Universidade do Minho
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Development of a Single-Phase Modular Multilevel Converter for Electrical Power Systems

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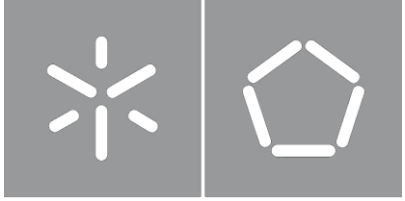

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Development of a Single-Phase Modular Multilevel Converter for Electrical Power Systems

Master Thesis
Master in Industrial Electronics and Computers Engineering

Work developed under the supervision of

Professor Vítor Duarte Fernandes Monteiro

Professor João Luiz Afonso

October 2022

To the star that shines the brightest.

Acknowledgement

The development of this dissertation counted with important contributions from many people, to whom I direct my most sincere thanks.

To my supervisors, Doctor Vítor Monteiro, and Doctor João Luís Afonso, for the constant motivation and availability displayed throughout all the stages of the work, both in professional and personal aspects.

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To my girlfriend for all the emotional support and company provided over the past year, without whom it would be much harder to keep the focus.

STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

Resumo

Com especial enfase nos últimos anos, tem-se verificado um aumento, tanto na demanda quanto no preço da energia elétrica, surgindo a necessidade de desenvolvimento de sistemas de conversão de energia elétrica mais eficientes. Neste contexto, esta Dissertação de Mestrado foca-se no estudo, simulação e desenvolvimento de um conversor modular multinível (*modular multilevel converter*, MMC) baseado na utilização de submódulos em meia ponte. O MMC tem como fator chave a modularidade, que permite atingir níveis de potência mais elevados, melhorar os sinais de saída de tensão e de corrente do conversor, e resultar numa uma solução mais compacta. O conceito de modularidade permite o aumento da tensão de operação do conversor utilizando submódulos em série, e o aumento da corrente de operação utilizando submódulos em paralelo. Adicionalmente, em caso de mau funcionamento de um submódulo, o conversor pode ser reconfigurado e continuar a operar, embora com um nível de potência inferior. Devido à versatilidade que o MMC permite, este pode ser utilizado em diversas aplicações, tais como sistemas de transmissão de energia em HVDC, sistemas ferroviários, transformadores de estado sólido e interface de energias renováveis.

No âmbito desta dissertação foi desenvolvido um modelo de simulação com o software vocacionado para a eletrónica de potência PSIM, incorporando o sistema de potência e o sistema de controlo, com o objetivo de permitir uma análise completa do MMC proposto. No modelo PSIM foram considerados vários detalhes do circuito de potência, nomeadamente, os semicondutores utilizados e os filtros de acoplamento, e vários detalhes do circuito de controlo, concretamente o controlo digital com programação em linguagem C, bem como as funções a serem implementadas no protótipo experimental.

Posteriormente à validação computacional em PSIM, foi desenvolvido um protótipo laboratorial (500 W, 230 V - 50 Hz, 200 VDC), agregando dois submódulos superiores ligados em série e dois submódulos inferiores também ligados em série, os respetivos circuitos de comando e de interface com o circuito de potência, circuitos de sensorização, circuitos de condicionamento de sinal, assim como a plataforma de controlo digital utilizando o DSP TMS320F28379D. Inicialmente, os resultados experimentais foram obtidos de forma independente para validar cada submódulo e, depois, mais relevante, foram obtidos resultados experimentais com o MMC a operar com o conjunto dos quatro submódulos.

Palavras-Chave: Conversor Modular Multinível (*Modular Multilevel Converter*, MMC), Eletrónica de Potência, Controlo Digital.

Abstract

With special emphasis in recent years, an increase has been verified not only demand, but also in the price of electric energy, emerging the need to develop more efficient electric energy conversion systems. In this context, this Master Dissertation focuses on the study, simulation, and development of a modular multilevel converter (MMC) based on the use of half-bridge submodules. The key to the MMC is the modularity, which allows the converter to reach higher efficiency levels, improving the voltage and current output signals of the converter, resulting in a compact solution. The modularity concept allows the increase of the operation voltage of the converter using submodules in series, and the increase the operating current using submodules in parallel. Additionally, in the event of a submodule malfunction, the converter can be reconfigured and continue the operation, albeit at a lower power level. Due to its versatility, the MMC can be used in a variety of applications such as HVDC power transmission systems, railway systems, solid state transformers and renewable energy interface.

Within the scope of this dissertation, a simulation model was developed recurring to PSIM power electronics software, incorporating the power and control systems, in order to allow both low-level and high-level analysis of the MMC. In the PSIM model, several details of the power circuit were considered, namely, about the semiconductors used and the coupling filters, as well as several details of the control circuit, especially the digital control in C programming language with functions to be implemented in the experimental prototype.

After the computational validation in PSIM, a laboratory prototype was implemented (500 W, 230 V - 50 Hz, 200 VDC), connecting two submodules in the upper arm in series, two submodules in the lower arm in series as well, the respective driver and command circuits, sensing and signal conditioning circuits, was well as a digital control platform recurring to the DSP TMS320F28379D. Initially, experimental results were obtained independently to experimentally validate each sub-module and, later, more relevantly, experimental results were obtained with the MMC operating with the set of four sub-modules.

Keywords: Modular Multilevel Converter (MMC), Power Electronics, Digital Control.

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Acronyms and Abbreviations

Acronym	Significance
AC	Alternating Current
ANPC	Active Neutral-Point Clamped
CHB	Cascaded H-bridge
CNPC	Cascaded Neutral-Point Clamped
CSC	Current Source Converter
CSI	Current Source Inverter
DC	Direct Current
DSP	Digital Signal Processor
FB	Full-Bridge
FC	Flying Capacitor
GaN	Gallium Nitride
GTO	Gate Turn-off Thyristor
HB	Half-Bridge
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
IGCT	Integrated Gate-Commutated Thyristor

LCI	Load-Commutated Inverters
MMC	Modular Multilevel Converter
NNPC	Nested Neutral-Point Clamped
NPC	Neutral-Point Clamped
PLL	Phase Locked Loop
PV	Photovoltaic
PWM	Pulse-Width Modulation
SiC	Silicon Carbide
SST	Solid-State Transformer
STATCOM	Static Synchronous Compensator
VCO	Voltage Controlled Oscillator
VSC	Voltage Source Converter
VSI	Voltage Source Inverter
ZOH	Zero Order Holder

Chapter 1

Introduction

1.1 Context

Power electronics is contemplated as the conversion and control of electrical power. Switching devices are used to achieve such purpose, due to the high efficiency to them associated. Power electronics is a popular topic of research, being in constant evolution since its beginning [1].

Over the past few years, with the constant evolution of new and improved power devices, many kinds of power converters have been developed for wide power applications. Regarding high power applications, the efficiency of power converters is of paramount importance since the stress of the components is higher due to the magnitude of voltage and current. As such, to overcome such limitations, a new family of power converters was introduced, the multilevel converters, with special focus in three-phase applications.

The multilevel converters appeared in 1974 [2] and have raised in popularity due to their characteristics and advantages, which include [3]:

- Reduction in power loss leading to better efficiency;
- Simple redundancy due to the modular structure;
- Low dv/dt in the switching power devices;
- Superior harmonic performances in the controlled variables;
- Low common mode voltages;
- Scalability to superior voltage and current levels due to the modular structure.

The previous advantages lead to the compactness of the power converter, i.e., design of power converters with high power density, and to the reduction of the coupling filters, as well as to the reduction of the production costs.

Within the multilevel the family, the modular multilevel converter (MMC) has been one of the most promising power converters for medium/high voltage applications compared to the conventional converters. The MMC can reach voltage values up to 400 kV, with power rating of 1000 MW [4], which makes this kind of converter very attractive from an industrial and academic point of view. In addition to the multilevel advantages, the MMC possesses some unique characteristics of its own [5]:

- Modular construction;
- Voltage and power scalability;
- Fault-tolerant operation.

However, the MMC also presents some disadvantages when compared to other power converters, such as:

- Extra controller required for balancing the capacitors voltage;
- Existence of a circulating current that needs to be suppressed, otherwise there will be an increase of device losses. These advantages result in a much more complex control system, due to the number of variables being monitored.

The first MMC available commercially was installed in Transbay, a Siemens project in San Francisco in 2010 [6] and has extended to a wide array of applications ever since, such as variable speed drives, power quality applications, renewable energy interface, Railway power systems, solid state transformers and HVDC systems [7].

There are several MMC topologies regarding the different structures of submodules and their integration, each presenting their own advantages and disadvantages, which will be discussed and presented further.

In Figure 1.1, is presented a high-level diagram of the proposed MMC topology to be developed in the scope of the present dissertation.

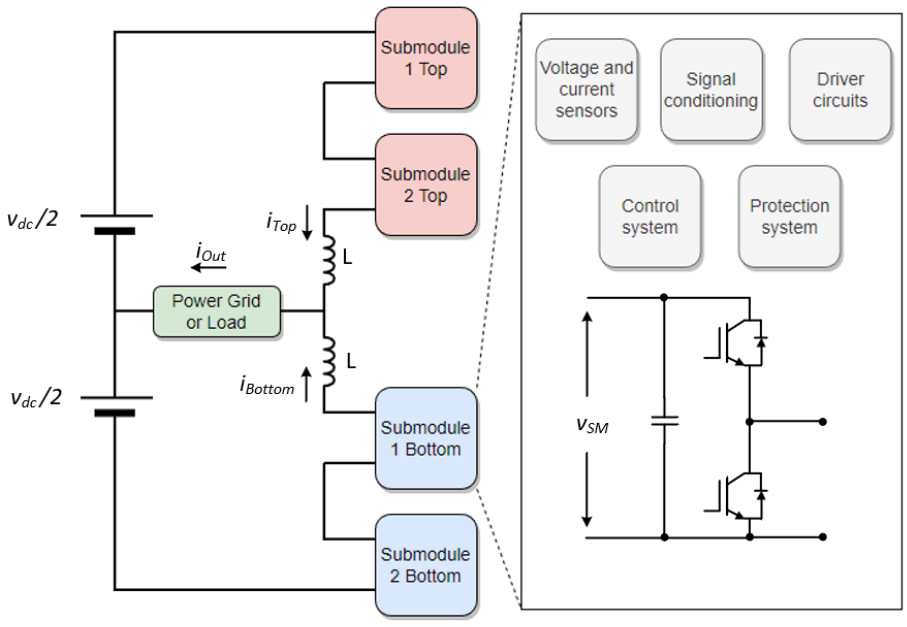


Figure 1.1 High-level block diagram of the MMC topology proposed in the present dissertation.

As it can be seen, the converter is composed by a split DC-link and four half-bridge submodules. Each submodule is equipped with a driver circuit, voltage and current sensors and respective signal conditioning. Recurring to these sensors, it is implemented a protection system in both hardware and software, which is essential to ensure the good functioning of the submodule, as well as keeping the DC-link capacitors balanced.

1.2 Motivation

Throughout the development of this dissertation in the Group of Energy and Power Electronics (GEPE) in the University of Minho the main goal is to learn as much as possible as well as contribute to the literature, with the research and implementation of a power converter in an MMC topology.

MMC topologies have been studied and improved over the past few years and are a very interesting research topic due its versatility, especially for medium/high power applications. The focus of the present dissertation is to study and develop a generic MMC that can be applied in different types of applications. In the scope of present dissertation, after a strong simulation component, it will be carried out the development of both software and hardware for the MMC submodules, as well as their integration. The software will be implemented recurring to digital control based on DSP and the power hardware will be developed using discrete IGBT as switching devices. The work is concluded with an experimental validation in laboratory.

From a personal perspective, this dissertation allows me to explore the field of academic research with active contributes through the publication of scientific articles, enriching my academic path as well as enabling new opportunities.

1.3 Objectives and Description

The goal of this dissertation is to develop a single-phase MMC capable of interfacing with loads and with the electrical power grid, dividing the total power of the converter through all the submodules. The implementation of the auxiliary control and power circuits aims for the modularity concept, making it easier for an eventual expansion of the number of submodules of the MMC. To be able to fully accomplish such objective, the following steps must be contemplated.

Computational Simulations

- Development of a complete high-level simulation model, regarding the power circuit for each submodule;
- Integration of the submodules resulting in the MMC;
- Close-loop control;
- Balancing of the DC-link capacitors of the submodules.

Submodule Implementation

- Development of sensing and instrumentation and respective signal conditioning;
- Development of the driver circuits;
- Development of the power circuit;
- Integration of the above-mentioned points making up a submodule;
- Control of the submodule in both open-loop and close-loop.

Integrated Implementation

- Integration of the submodules;
- Close-loop control;
- Balancing of the DC-link capacitors of the submodules;
- Interface with different load;
- Interface with the electric power grid;

1.4 List of Publications

Published Technical Articles:

1. **N. Rodrigues**, J. Cunha, V. Monteiro, Joao L. Afonso, "*Technical and Economical Evaluation of Modular Multilevel Converters for the Electrical Power Grid Interface*" in ICEE International Conference on Energy and Environment: Bringing Together Engineering and Economics, Porto, Portugal, 2022, https://hdl.handle.net/1822/81237[8].
2. **N. Rodrigues**, J. Cunha, V. Monteiro, Joao L. Afonso, "*Railway Auxiliary Power Supply System: A Modular Multilevel Converter Approach*" in Research Arena TRA 2022, Lisbon, Portugal, 2022, https://hdl.handle.net/1822/81242[9].
3. **N. Rodrigues**, J. Cunha, V. Monteiro, Joao L. Afonso, "Modular Multilevel Converter: A Comparison of Pulse-Width Modulation and Current Control Techniques" in SESC 2022 - 4th EAI International

Conference on Sustainable Energy for Smart Cities, Novembe, 2022, Braga, Portugal, https://hdl.handle.net/1822/81241[10].

Submitted Technical Articles:

1. **N. Rodrigues**, J. Cunha, V. Monteiro, Joao L. Afonso, "Development and Experimental Validation of a Reduced-Scale Single-Phase Modular Multilevel Converter" in MDPI Electronics 2022.

1.5 Dissertation Organization

The layout of the present dissertation assembles seven chapters.

The first chapter is the introduction, which presents an overall framework of the dissertation, the motivations which drove the development of the dissertation, the objectives with a detailed description, the list of publications and the dissertation organization.

The second chapter focus on the study and presentation of the different applications on which MMC is used, recurring to the literature to present both final products and ongoing investigation prototypes.

The third chapter details different topologies of multilevel converters, with especial focus on the MMC, also presenting different types of submodules for such type of converter. Then, different modulation, and control techniques for the MMC that allow the control of the chosen converter topology are presented. The second and third chapter refers to the state of the art.

The fourth chapter refers to computational simulations of the MMC and the associated circuits, recurring to software PSIM to allow the validation of the topology as well as the tunning of the controllers. The simulation aims to create and environment as close as possible to the real-world conditions, despite of the non-linearity of the components used in practice.

The fifth chapter presents the implementation of both hardware and software.

The sixth chapter carries out the experimental tests and results obtained in the laboratory.

The seventh chapter presents the conclusions and critic analysis about the dissertation as a whole and the prospects for future works.

Chapter 2

Applications of Modular Multilevel Converters

2.1 Introduction

Due to the unique advantages presented by the MMC [11], it has been a common topic of research and development for medium/high power and high voltage applications. The main and first application of the MMC is related with HVDC applications [12], however, over the past few years, the research associated to the operation and control of the MMC have allowed the broadening of its possible applications to several others, which are presented in this chapter.

2.2 High Voltage Direct Current

Due to the low conduction and switching losses and, voltage-source converters (VSC) using MMC are an interesting solution for the connection of AC grids through HVDC. The modularity and scalability it offers, allows the use of low voltage and low-cost semiconductors with a higher DC-link voltage [13]. The MMC equivalent switching frequency is high since it is the sum of the switching frequency of each submodule in an arm, even though each submodule can be switched at a very low frequency (50 to 150 Hz) [4].

The connection of AC grids through HVDC can occur in various circumstances [5]:

- Connecting different frequency grids (50 Hz and 60 Hz);
- Connecting asynchronous grids;
- Connecting islands to the mainland;
- Connecting weak grids, using the power converters to inject reactive power supporting the power grid;
- Connecting offshore wind power to the mainland;
- Long distance power transmission greater than 800 km – 1000 km.

Monopolar and bipolar systems in the symmetrical and asymmetrical layouts are examples of MMC-HVDC configurations, regarding two-terminal and multi-terminal HVDC systems [14]. Monopolar and bipolar systems possess several differences in terms of power rating and cost associated: the bipolar configuration is more complex, possessing two converters in each end, making it possible to reach higher power ratings and more suitable for fault- tolerant operation. Despite such advantages, the cost is higher due to the amount of extra hardware required comparing to the monopolar configuration [15].

2.2.1 Two-Terminal HVDC Systems

Two-terminal MMC-HVDC systems, or symmetrical monopolar MMC systems possess one converter at the receiving station, and another at the sending station [16]. There are many different topologies in which MMC can be implemented, although the only commercially available is Half-Bridge, due to high efficiency and low-cost. The different topologies will be presented in further on.

Aside from the power converters, the HVDC systems use isolation transformers, star-point reactor with ground impedance and DC cables. Regarding the isolation transformer, it is common for the star winding to be connected on the AC grid, while the delta winding is connected to the MMC AC signal, therefore blocking the zero-sequence currents, and preventing their entrance in the systems during faults in the AC-side [17]. A two-terminal HVDC system based on MMC is presented in Figure 2.1.

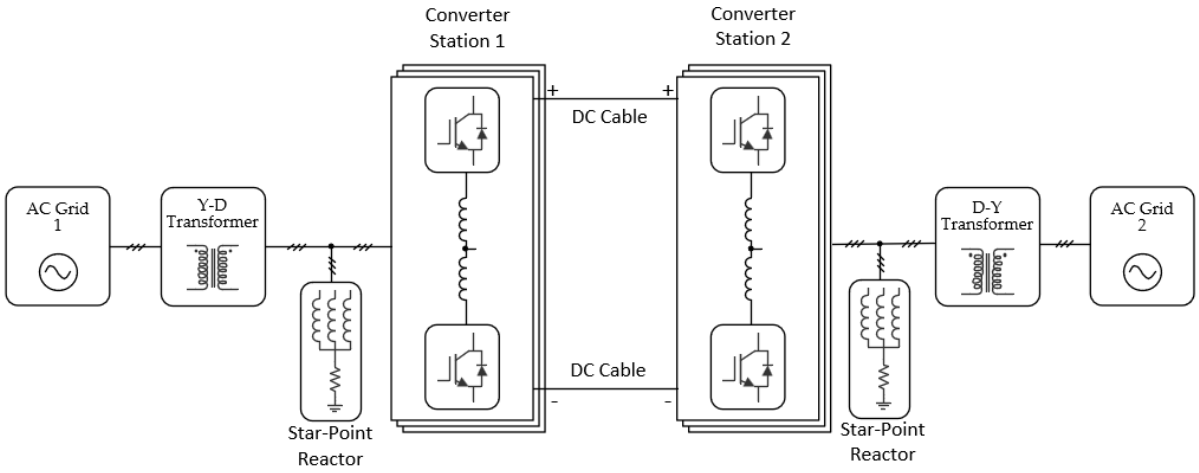


Figure 2.1 Two terminal HVDC system based on MMC.

MMC are currently in use and being installed by major corporations, such as Siemens, ABB, and Alstom. The first ever project in which MMC was implemented was Trans Bay Cable, which is a HVDC underwater transmission cable interconnecting San Francisco and Pittsburg in California, USA with a length of 85 km, and with power rated at 400 MW, at a DC voltage of ±200 kV [6].

Another major project where MMC was used in HVDC is DolWin1 by ABB which is a link to transmit offshore wind power to the power grid of the German mainland. This project has a particularity when compared to others, since one of the two converter stations are built on a platform in the sea, converting AC to DC. The second converter station is placed in the mainland and converts DC to AC. The MMC in each end of the DC link use cascaded half-bridge submodules with a DC voltage of ±320 kV at 800 MW over 165 km [18].

2.2.2 Multi-Terminal HVDC Systems

While two-terminal HVDC systems use one converter in each end, multi-terminal systems use two or more converter stations in each end, either in series or parallel. In parallel systems, the converters share the DC voltage, while in series systems, the same DC current flows through both converters. Regarding reliability, parallel systems are more advantageous since in permanent faults in the system, only the converter where the fault is caused is interrupted, while in series systems, the whole complete system is interrupted [19]. A multi-terminal HVDC system based on MMC is presented in Figure 2.2.

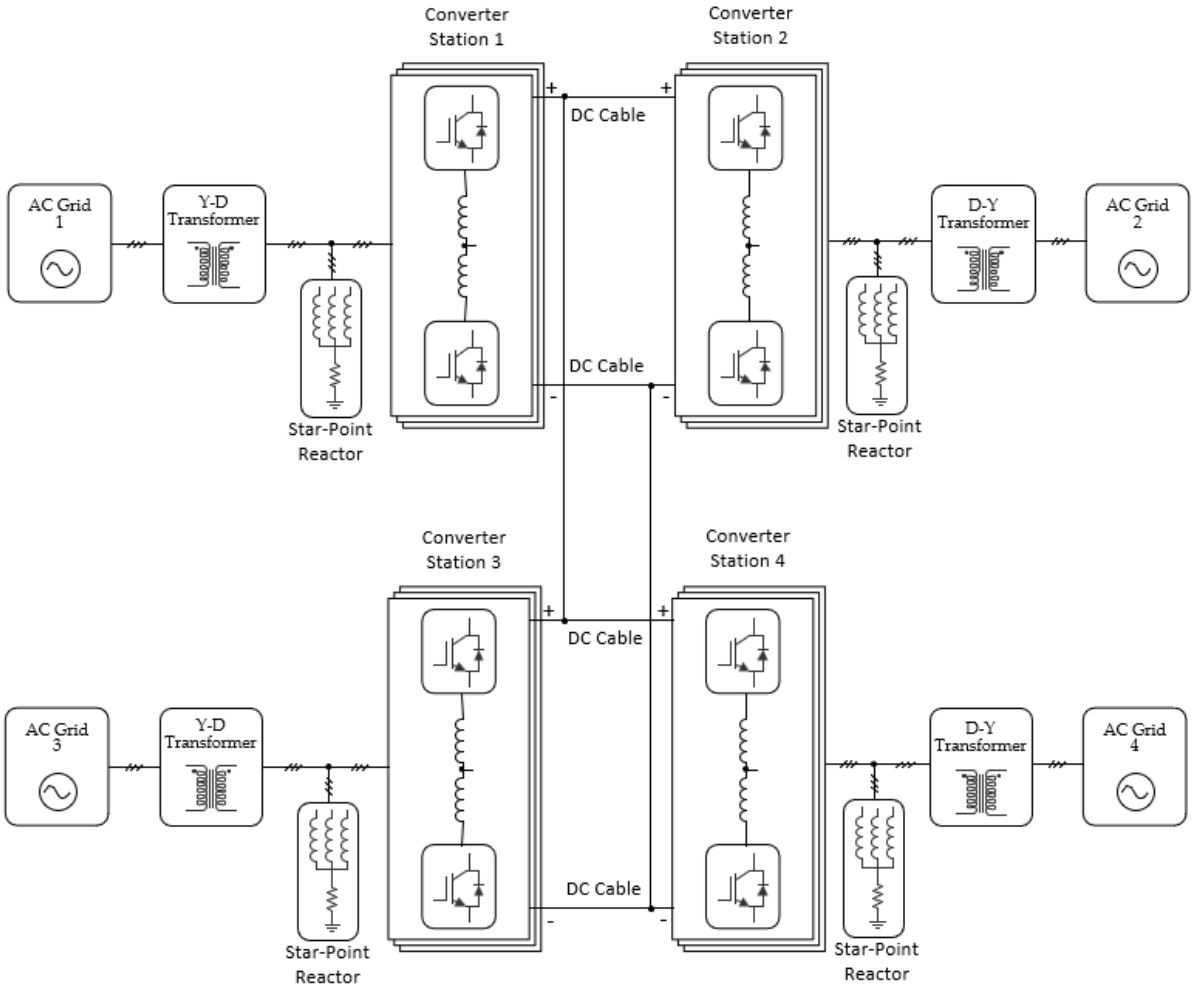


Figure 2.2 Multi-terminal HVDC system based on MMC.

Both VSC and CSC can be used in HVDC multi-terminal systems, with special focus on VSC-HVDC converter technology, which allows the control of both active and reactive power. MMC is currently used in many VSC-HVDC multi-terminal systems, with two major projects in China, Nanao project [20] and Zhoushan project [21].

When it comes to DC-side short-circuit faults, the vulnerability of the multi-terminal systems must be considered. To implement DC-side short-circuit protection, two different methods can be used: incorporate fault-blocking in the converters control which adds complexity in a software level [22][23], or use HVDC circuit breakers, based on semiconductor technology, adding more complexity in a hardware level [13].

2.3 Medium Voltage Motor Drivers

Due to the performance and high efficiency, medium voltage motor drivers have been widely utilized with an important role in industry in a wide array of applications, such as pumps, fans, compressors, metal rolling, mine hoists, refineries and grinding mills, resulting in very high availability requirements, due to the financial consequences that follow a possible failure in the motor [24]. As such, the reliability of the power converters used as drives is a key factor for the choice of the converter topology [25][26].

In Figure 2.3, it is presented a diagram for the drive of a medium voltage motor. It includes a power transformer, two conversion stages and a DC-link.

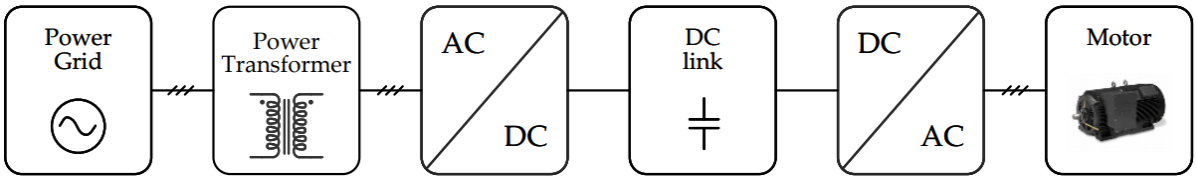


Figure 2.3 Medium voltage motor drive diagram.

The first conversion stage, an AC-DC converter works as a rectifier, converting the AC grid voltage into a DC voltage. There are many possibilities for the topology of this converter, from multi-pulse rectifiers using phase shifting transformer to eliminate low-order harmonics, to active rectifiers using MMC, which is more suitable for regenerative applications. The second conversion stage refers to the conversion of the DC voltage in the DC-link to a three-phase voltage in the motor [27].

The power transformer on the AC grid side allows the blocking of the common mode voltage that is generated by the grid-side and will not appear in the motor. Despite being very advantageous due to the effectiveness of the solution, the transformer increases both the size and the cost of the motor drive, as well as decreasing the efficiency of the system itself due to the power losses on the transformer.

Due to the possibility of large amount of submodules in MMC, the common mode voltage generated is much smaller, fading away the need of multi-winding transformers [28], if used on both conversion stages,

which can allow the achievement of a reliable and compact motor drive at a lower cost [29], as presented in Figure 2.4.

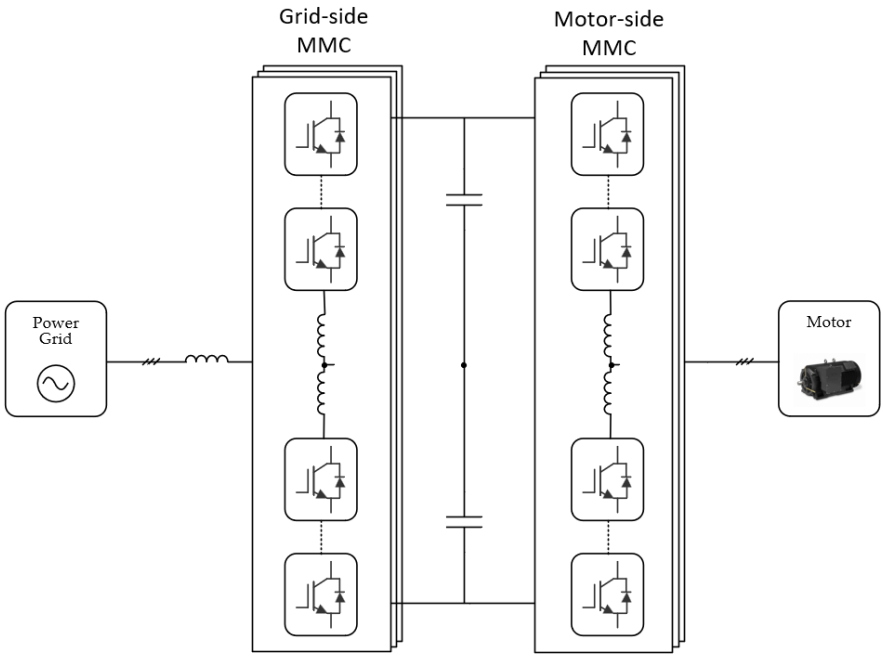


Figure 2.4 Transformer-less medium voltage motor drives based on MMC.

In the article presented in [30], it is proposed and studied an MMC with a flying-capacitor topology, validating both in simulation and experimentally the feasibility of the MMC in medium voltage motors. In the article presented in [31] it is proposed a half-bridge MMC using medium voltage SiC power devices.

2.4 Static Synchronous Compensator

It is frequent for medium voltage distribution lines to have problems related to reactive compensation due to voltage variations, unbalances, and harmonics. The voltage variations appear mostly due to start or cease of functioning of a major load or motor. The unbalances are caused by single-phase applications and asymmetric faults. Harmonics appear due to nonlinear loads, as well as the saturation of transformers.

At first, thyristor-based line-commutated converters were used to improve the power quality, having later migrated to power converters based on self-commutated devices, such as GTO and IGBTs. The STATCOM included in this group of power converters, and it is used to mitigate all the referred problems through its capacity for reactive compensation and voltage regulation [32].

Usually, it is used a H-bridge topology with a large DC-link capacitor to implement the STATCOM, but it is a solution with several limitations when it comes to situations of grid unbalances since the output voltage

of the converter only is limited to three levels [33]. MMC STATCOM solutions have been proposed due to offering more output voltage levels, which leads to having more degrees of freedom in the control. Using an MMC with a high number of submodules also allows coupling to the power grid without recurring to transformers, as demonstrated in Figure 2.5 [34]. Furthermore, there is no need for an external capacitor to store energy since that function is carried out by the capacitor present in each submodule of the MMC [35]. A recent STATCOM technology using MMC is commercially available under the trade name of SVC-PLUS [36][37].

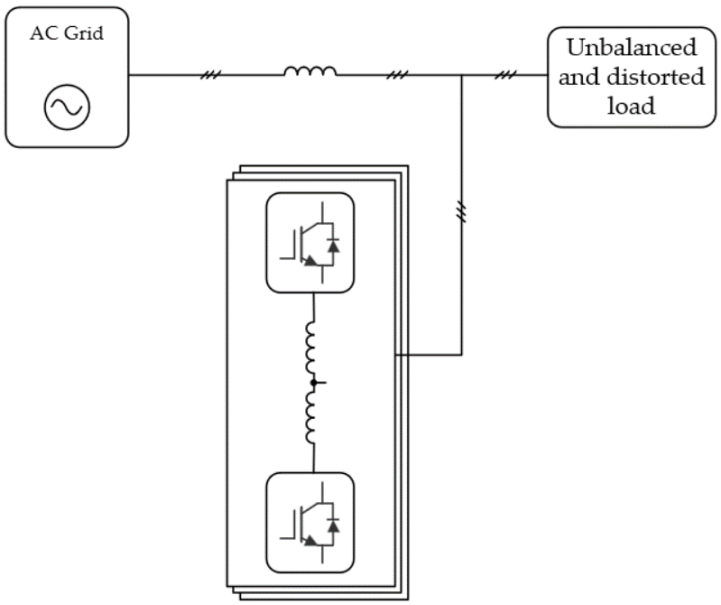


Figure 2.5 STATCOM based on MMC topology.

2.5 Solid-State Transformers

Over the last two decades, solid-state-transformers (SST) have risen in popularity amongst the high-power converters, being extensively investigated in diverse areas, with special focus on distribution systems due to its capability of electrical isolation, voltage transformation and power quality management [9].

The purpose of an SST is to perform power conversion recurring to medium to high frequency isolation, thus reducing the volume, weight and cost of the transformer required.

In Figure 2.6, it is presented a high-level diagram of a common SST topology, consisting in the use an AC-AC converter with an input of 50 Hz or 60 Hz voltage signal which is transformed to higher frequency to seize the advantages of the high frequency transformer. This is called the input stage of the SST. After the transformer, another AC-AC converter is used to shape back the high frequency signal to 50 Hz or 60 Hz to power the loads it is intended to, while maintaining galvanic isolation. This is called the output stage of the SST [39].

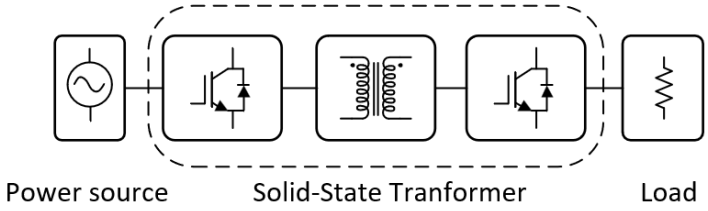


Figure 2.6 SST high-level diagram.

There are two kinds of SST in use, being the traditional two or three-level voltage source converter (VSC) type and the cascaded H-bridge type. However, as SST are commonly used in middle/high voltage systems, the input stage needs power electronics devices in series or parallel, causing voltage or current balancing problems. In article [40] it is proposed an SST topology recurring to an MMC.

The MMC is used as the grid-connected converter at the input stage. Increasing the number of sub-modules in each arm, the withstand voltage of the input stage converter is enhanced, which enables SST to be applied to medium or high voltage systems [41]. Using carrier phase-shift pulse width modulation (PWM), although each submodule has a low switching frequency, the equivalent switching frequency of the MMC is higher, reducing the harmonic component injected in the power grid and the switching loss of the power electronic devices.

2.6 Renewable Energy Interface

Renewable energy sources became very attractive regarding electric energy generation and have experienced an exponential growth over the past decades, with a tendency to grow each year [42]. Wind and photovoltaic are the most used renewable energy sources in terms of installed power due to the advantages provided when it comes to accessibility, capability, and cost of energy. Even though these technologies share the same purpose, there is several differences between them, especially in high power applications. While wind energy systems can be connected to medium voltage networks in both onshore and offshore plants without isolation issues [43], PV panels do not permit operating with more than 1500 V, so the PV systems are always connected to low-voltage networks [44].

The modularity offered by the multilevel converters, as well as the other advantages favor their use in large PV plant applications, however, the PV panels are unable to operate at medium and high voltage levels, therefore the number of cells of the multilevel converters in use industrially is reduced and operate at low-voltage and low-power levels [45].

In the article [46] it is proposed a novel multilevel converter that provides multiple isolated modules connected in series through low-frequency transformers to operate at medium voltage levels., as presented in Figure 2.7.

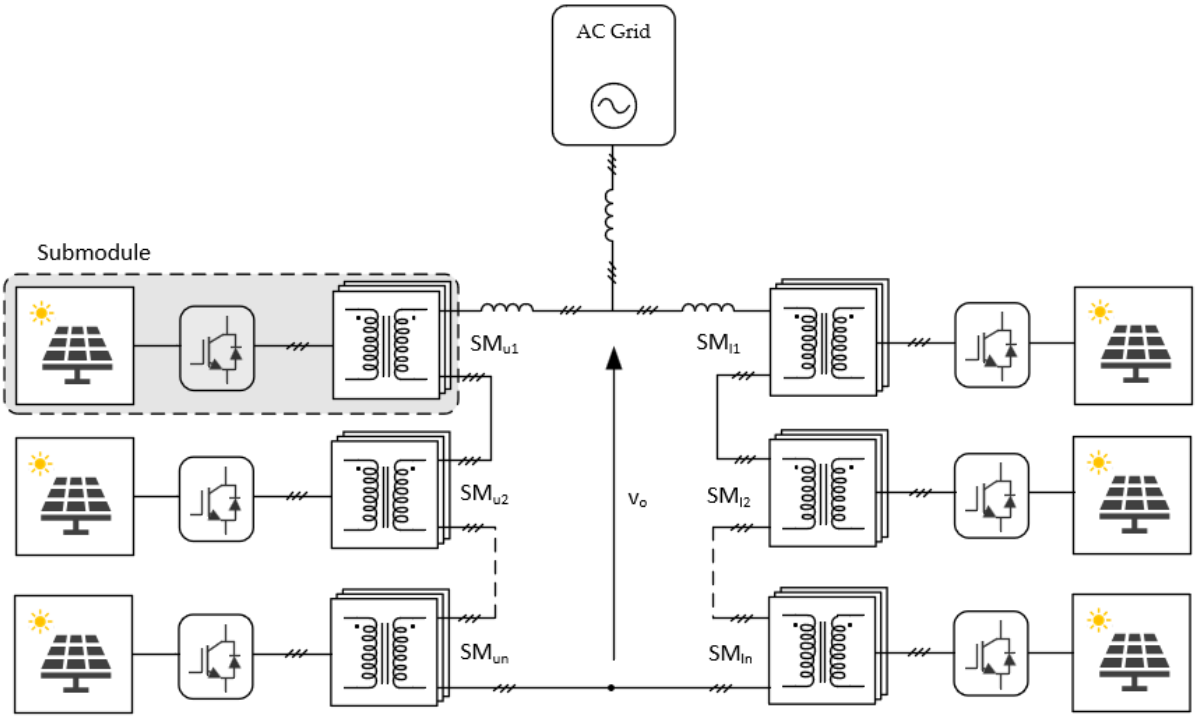


Figure 2.7 Isolated MMC for PV integration.

2.7 Railway Power Systems

The electrification of a train goes through some power conversion stages, from the power lines to the powering of the traction electrical motors and the auxiliary services. The power is supplied through a pantograph from the power lines. In Figure 2.8 is presented a generic diagram of the power of a train, consisting in an AC power line (15 kV or 25 kV), a pantograph, a circuit breaker, a high-power transformer and three power converters. The same concept is used to trains powered in DC, without using the power transformer and the main converter presented.

The main converter is responsible for creating a DC link from which the propulsion inverter and the static inverter use as input voltage. The referred DC link is shared by both, as such, due to the power required for the traction motors, the DC link suffers very high fluctuations. The propulsion inverter is a powerful power converter responsible for controlling the traction electrical motors.

The static inverter is responsible for supplying the necessary power for the auxiliary services, which can be achieved in a vast array of possibilities. In Figure 2.8 is presented the usual topology, consisting in a DC-AC converter followed by a single-phase 50 Hz transformer. There are also solutions for this inverter using medium frequency transformers, with a rectifier and an inverter at the secondary-side of the

transformer, creating the same output in a more compact solution. The static inverter can also incorporate AC-DC converters for battery interface.

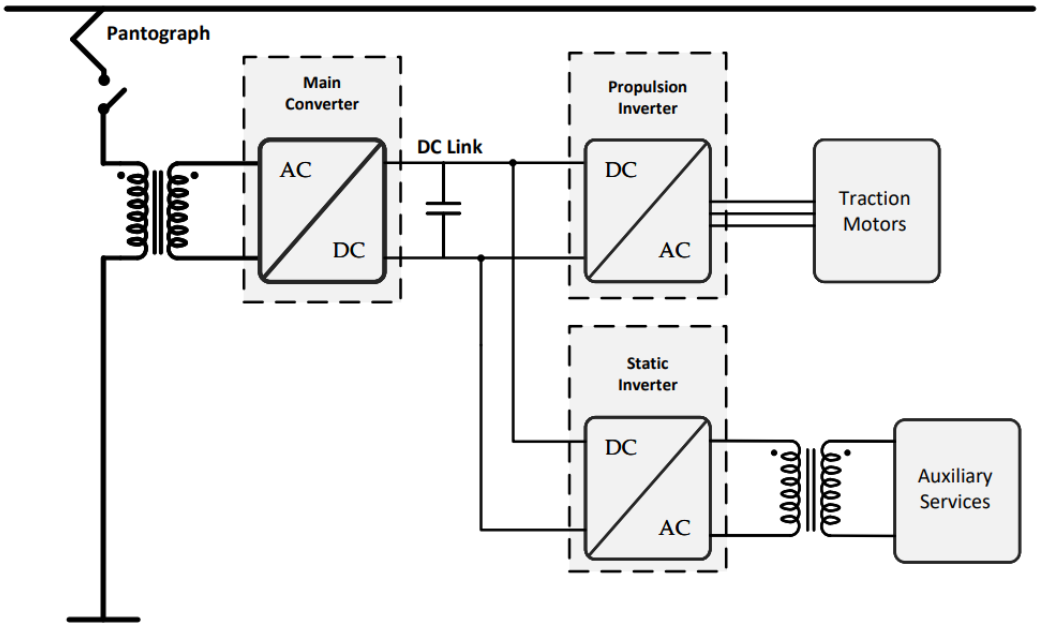


Figure 2.8 Generic diagram of the power system of a train.

A paper where I am first author proposes a new topology for a single-phase static converter, with the purpose of powering the auxiliary services of the train, such as AVAC, power plugs and illumination steadily, using an MMC, a high-frequency transformer, an active rectifier, and a power inverter. The proposed topology is presented in Figure 2.9.

With the proposed topology it is possible to split the voltage by the submodules which allows use components of lower voltage. This results in less power dissipated and lower temperature spots which facilitates the management of the heat. Furthermore, it promotes the possibility to use discrete semiconductors (with better switching performance) instead of modules.

Another topic in constant investigation regarding the railway power systems are the railway power conditioners based on MMC [47][48] The railway power conditioners aim to suppress negative sequence components that result is current unbalances in the three-phase system that powers the locomotives, decreasing the power quality, hence increasing the power losses, resulting in higher operating costs due to the reduced efficiency.

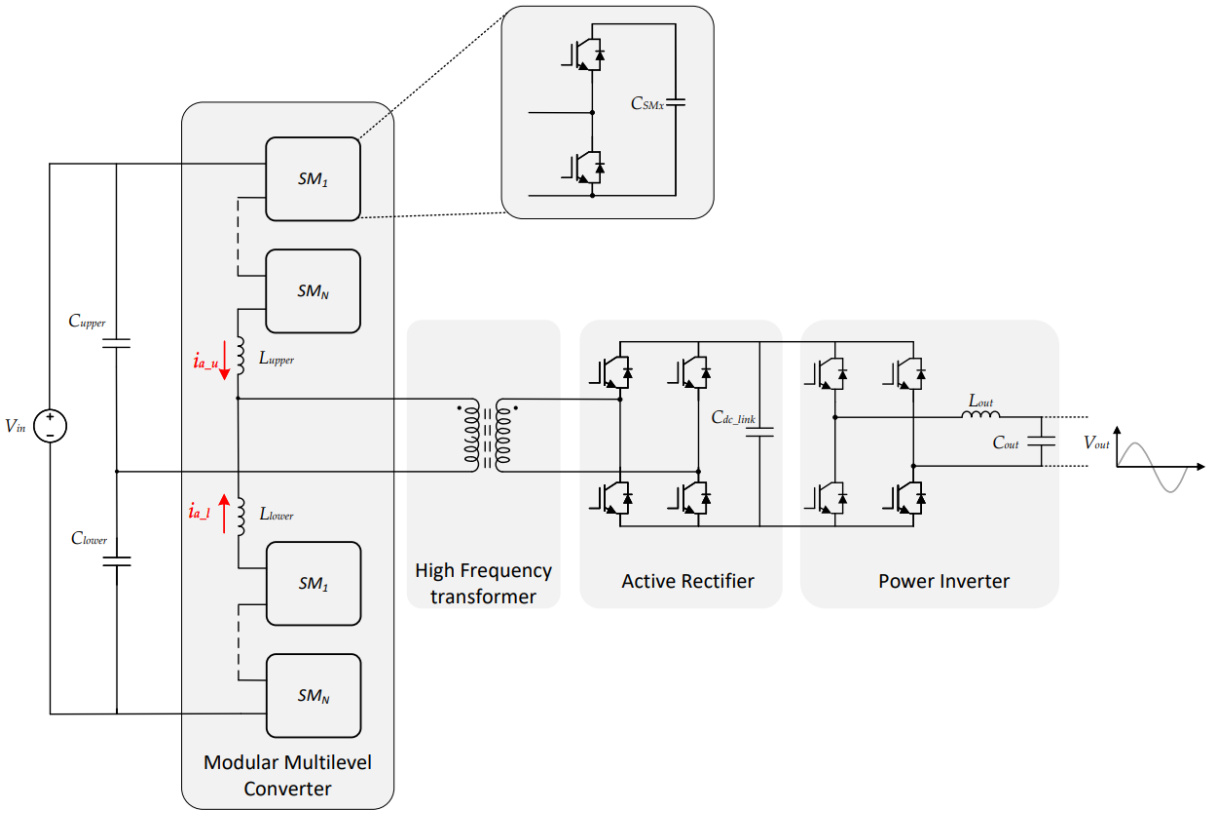


Figure 2.9 Topology for railway auxiliary power supply based on MMC.

2.8 Conclusion

This chapter presents the different applications where multilevel converters are used, with special focus on the MMC as is the topic of this dissertation. The most common usage of the MMC is on HVDC systems, namely on the interface of renewable energies to the power grids in DC current at a very high voltage, using MMC in both ends of the system. More and more investigation is being made and the literature is growing when it comes to MMC is the application of that are referred to in this section, from medium voltage motors and static compensators, due to the possibility of transformer-less operation, to railway power conditioners for an improvement of the power quality in the railway system.

Chapter 3

DC-AC Multilevel Topologies and Control Techniques

3.1 Introduction

Commonly referred as “power electronics inverters”, DC-AC power electronics converters are capable of synthesizing AC output waveforms controlling its magnitude and frequency, from a DC input on the DC-link. Usually, it is used PWM control techniques to synthesize the desired waveform with a switching frequency equal or multiple of the switching frequency of each semiconductor [49]. With the mentioned PWM techniques, the desired waveform is obtained through the output of the converters followed by a filter between the converter and the load, which can be inductive of capacitive, based on the classification of the converter. This type of converters can be classified as voltage source inverter (VSI) or current source inverter (CSI), according to the DC-link configuration.

In industry, CSI were also known as load-commutated inverters (LCI) and use mainly GTO and IGCT as switching devices. This type of converters is usually operated under short-circuit conditions with current-controlled switching devices, therefore requiring a low switching frequency. In CSI the output has high discrete values of di/dt, so the filter applied between the load and the converter is capacitive [50].

With the forthcoming of the IGBT in the market, a semiconductor designed for fast switching, VSI became more popular due to the advantages brought by the IGBT, especially the lower switching losses, resulting in a high efficiency and high reliability. Furthermore, the VSI is usually operated at a higher switching frequency, thus resulting in a low current harmonic distortion. In VSI, the output presents high discrete values of dv/dt, and, as such, to smooth the current waveform, the filter applied between the load and the converter is inductive [50]. The MMC fits in the VSI category, being the focus of this dissertation.

3.2 Multilevel Topologies

Multilevel converters are in general developed for high-power applications recurring to an array of low-cost semiconductors and DC capacitive voltage sources, presenting several advantages in comparison with high-power two-level converters, such as:

- Low dv/dt;
- Near-sinusoidal currents;

- Smaller filters;
- Low voltage harmonic distortion;
- High efficiency;
- Low common-mode voltage.

Some multilevel topologies also allow fault-tolerant operation. Among the multilevel converters there are two main types: Integrated multilevel converters and multi-cell multilevel converters [4].

3.2.1 Integrated Multilevel Converters

In this section are presented the most relevant topologies of integrated multilevel converters that are in use in industry. For each topology, it is presented a switching state table, which is crucial for the voltage balancing of the capacitors. Even though this type of converters possesses the advantages above mentioned, there are also some disadvantages associated, such as:

- The number of voltage levels of the converter is static, requiring modifications in the converter itself to increase the number of voltage levels, which is not cost-efficient;
- No fault-tolerant operation, meaning that if any failure occurs on the converter, it must be shut down.

3.2.1.1 Neutral-Point Clamped Converter (NPC)

First introduced by Akagi et al. in 1981[51], the NPC was one of the first topologies of multilevel converters to appear in the literature. In Figure 3.1 is presented a three-phase three-level neutral-point clamped inverter, a power converter usually found in high-power medium voltage drives.

This converter uses a DC-link composed by two split capacitors, resulting in a neutral reference point with two clamping diodes in each phase. The voltage on the DC-link capacitors is intended to be half of Vdc, and the capacitors can be charged and discharged by neutral current, which causes neutral-point deviation. This neutral-point deviation can also be caused by the real difference between components, such as manufacturing tolerances of the capacitors, inconsistency in semiconductors characteristics or unbalanced three-phase operation and can cause failure on the switching devices in use, leading to malfunction of the converter [52]. So, these factors must be considered when projecting the converter and the voltage across the DC-link capacitors needs to be monitored.

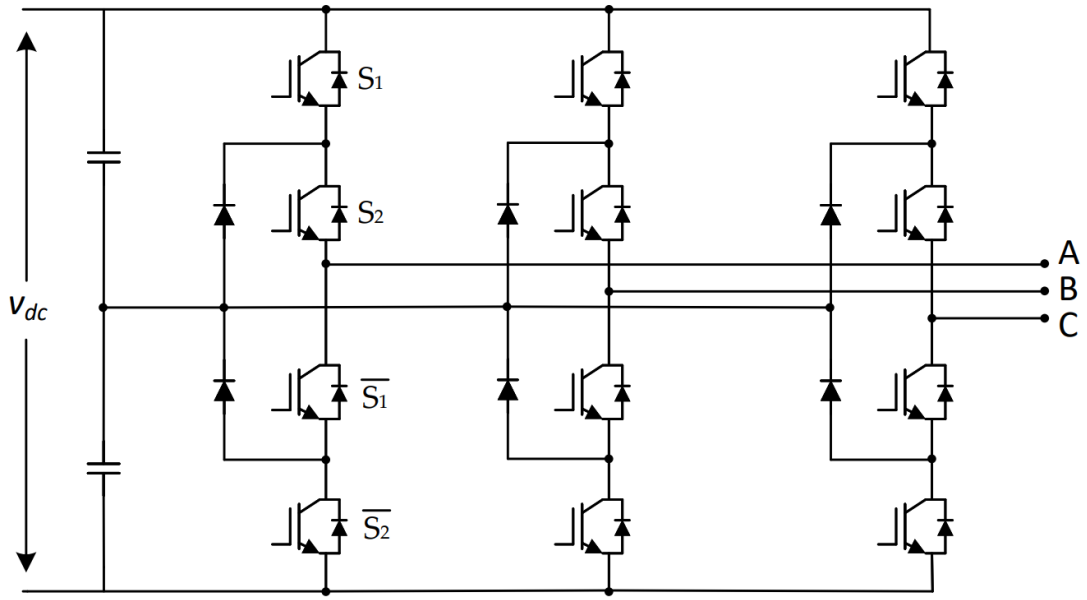


Figure 3.1 Three-level neutral-point clamped converter.

Furthermore, this topology has an issue with unequal power losses in the switching devices, leading to uneven temperature distribution in the semiconductor-junction. The switching states of a three-level NPC inverter are displayed in Table 3-1.

Table 3-1 Switching states of a three-level NPC inverter.

Switching State	Switching States (per phase)		Inverter Phase Voltage
	S_1	S_2	
Positive	1	1	$V_{dc}/2$
0	0	1	0
Negative	0	0	$-V_{dc}/2$

3.2.1.2 Active Neutral-Point Clamped Converter (ANPC)

In Figure 3.2, is presented a three-phase three-level active neutral-point clamped inverter, a topology derived from the three-level NPC inverter, replacing the clamping diodes by active clamping switches.

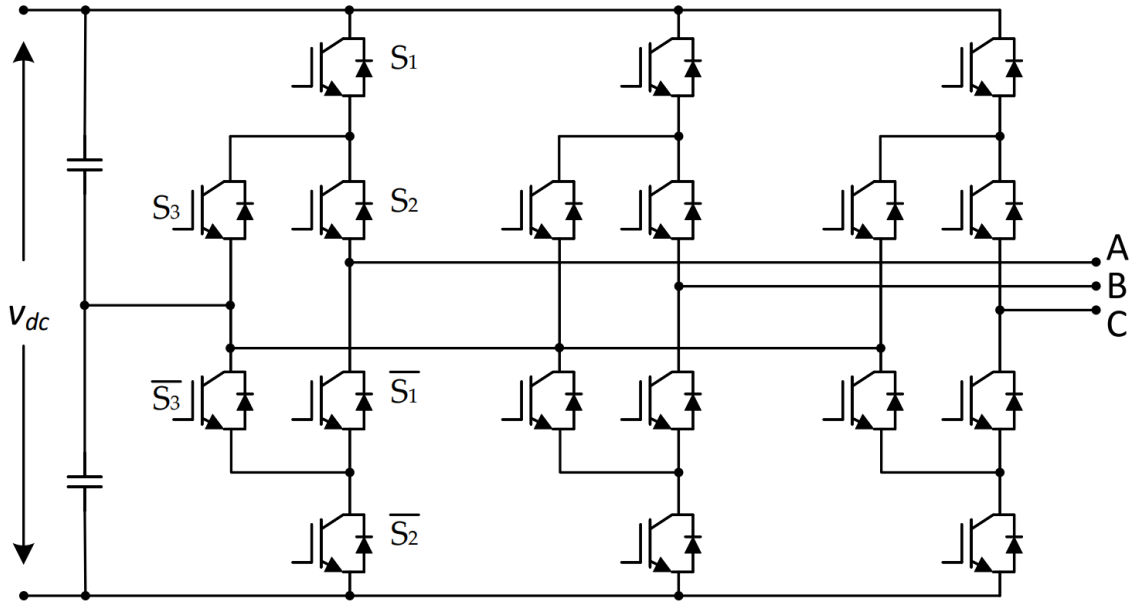


Figure 3.2 Three-level active neutral-point clamped converter.

This allows the control of the power loss distribution and even distribution in the semiconductor-junction temperature. This way, the ANPC overcomes some of the drawbacks of the NPC inverter, however the use of the active clamping switches increases not only the cost but the complexity of the converter. The switching states of a three-level ANPC inverter are displayed in Table 3-2.

Table 3-2 Switching States of a three-level ANPC.

Switching State	Switching States (per phase)			Inverter Phase Voltage
	S_1	S_2	S_3	
Positive	1	1	0	$V_{dc}/2$
0	0	1	0	0
	0	1	0	
	0	0	1	
	1	0	1	
Negative	0	0	1	$-V_{dc}/2$

3.2.1.3 Flying Capacitor (FC) Converter

In Figure 3.3, it is presented a three-phase four-level flying capacitor inverter [53]. This topology allows modularity within a certain degree of freedom as more levels are obtained by adding DC capacitors to the cascaded switching devices, which raises the complexity of the design and control of the converter.

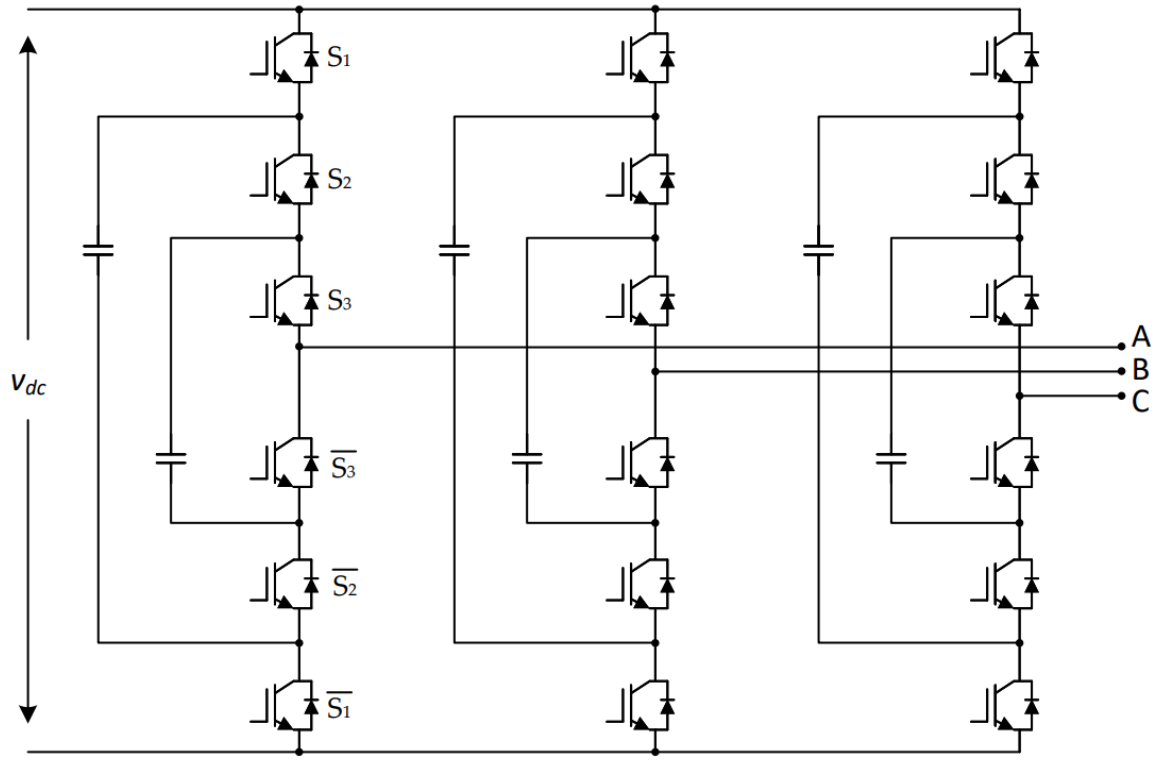


Figure 3.3 Four-level flying capacitor inverter.

Furthermore, the flying capacitors present in this topology have different voltage ratings, and each one requires a pre-charging circuit [50]. Still regarding the capacitors, the voltage on the flying capacitors needs to be monitored and controlled to avoid problems caused by the dc deviation, increasing even more the control of the converter. The switching states for each phase of the inverter are presented in Table 3-3, presenting some redundant switching states, which are crucial to the control and balancing of the flying capacitors.

Table 3-3 Switching states of a four-level FC inverter.

Level	Switching States (per phase)			Inverter Phase Voltage
	S_1	S_2	S_3	
3	1	1	1	V_{dc}
2	1	1	0	$2V_{dc}/3$
	1	0	1	
	0	1	1	
1	0	0	1	$V_{dc}/3$
	0	1	0	
	1	0	0	
0	0	0	0	0

3.2.1.4 Nested Neutral-Point Clamped Converter (NNPC)

In Figure 3.4, is presented a three-phase four-level nest neutral-point clamped inverter, which is a combination of the FC and NPC inverter.

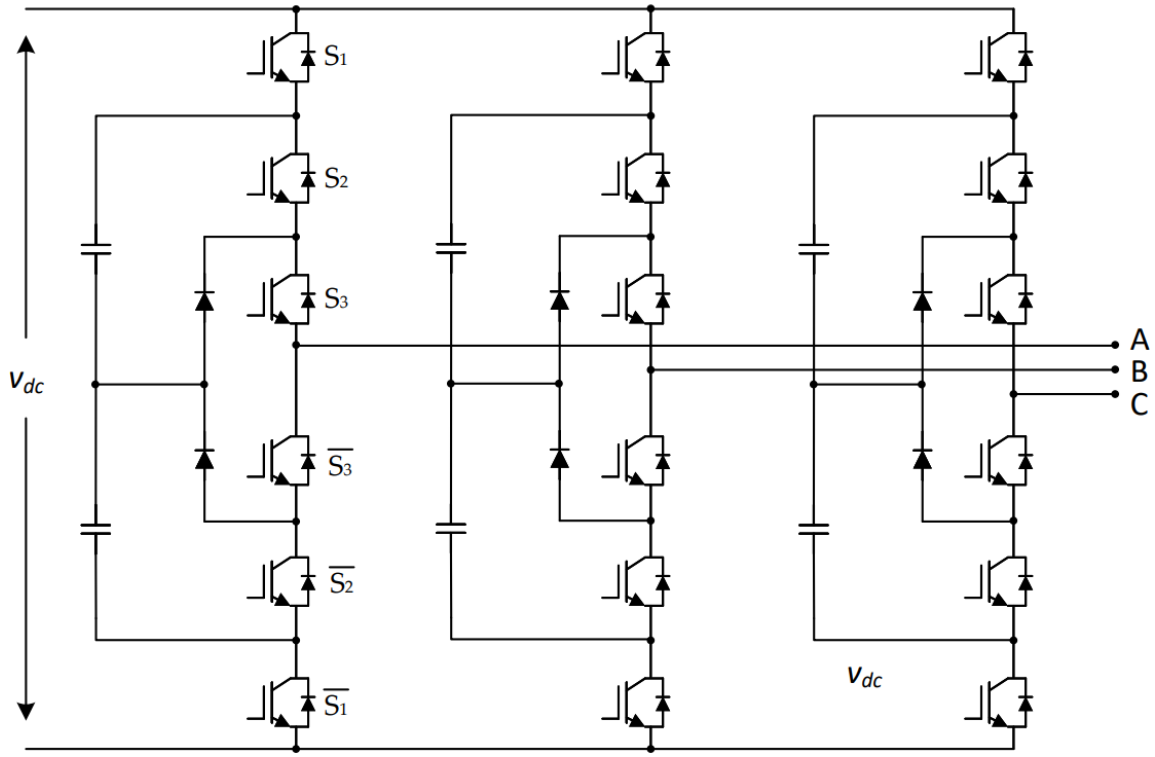


Figure 3.4 Four-level nested neutral-point clamped converter.

In this configuration, the voltage rating of each switching device is $V_{dc}/3$ and gets lower as more voltage levels are added to the inverter, resulting in low stress on the semiconductors. Unlike the NPC inverter, the clamping diodes in each phase are not connected to a dc-link midpoint, and comparing to the NPC topology, for the same purpose and voltage levels, the NNPC inverter requires fewer switching devices. However, a three-phase four-level NNPC topology required six flying capacitors which voltages need to be monitored and controlled, while in NPC the NPC only two dc-link capacitors need such control, thus resulting in a more complex control system for the NNPC topology. The switching states of a four-level NNPC inverter are displayed in Table 3-4.

Table 3-4 Switching States of a four-level NNPC.

Switching State	Switching States (per phase)			Inverter Phase Voltage
	S_1	S_2	S_3	
Positive 1	1	1	1	$v_{dc}/2$
Positive 2	1	0	1	$v_{dc}/6$
Positive 2	0	1	1	
Negative 2	0	0	1	$-v_{dc}/6$
Negative 2	1	0	0	
Negative 1	0	0	0	$-v_{dc}/2$

3.2.2 Multi-Cell Converters

In this section are presented the most relevant topologies of multi-cell converters, also known as cascaded converters. The multi-cell converters address the mentioned problems in section 3.2.1, since these topologies have a modular construction, allowing an easy scalability to higher values of voltage and current with the addition of submodules being able to handle greater voltage values using low-voltage switching devices, i.e., IGBT. Furthermore, as these converters are composed by separate submodules, in case of submodule malfunction, the converter can still operate at reduced capacity.

3.2.2.1 Cascaded H-bridge Converter (CHB)

The cascaded H-bridge converter is the most popular cascaded topology and consists in H-bridge power modules in cascade, each capable of outputting three voltage levels. In

Figure 3.5, is presented a three-phase five-level cascaded H-bridge.

Each module of the converter requires an isolated DC source, usually obtained from phase-shifting transformer with multiple secondary windings followed by a diode rectifier [4]. Connecting H-bridge with similar DC source modules increases the overall converter voltage, also increasing the power rating with a voltage rating of $2N+1$, being N the number of power modules in each phase. This topology is also referred as symmetrical CHB. However, the number of isolated power sources also increases, requiring a much more complex, expensive, and larger transformer [54].

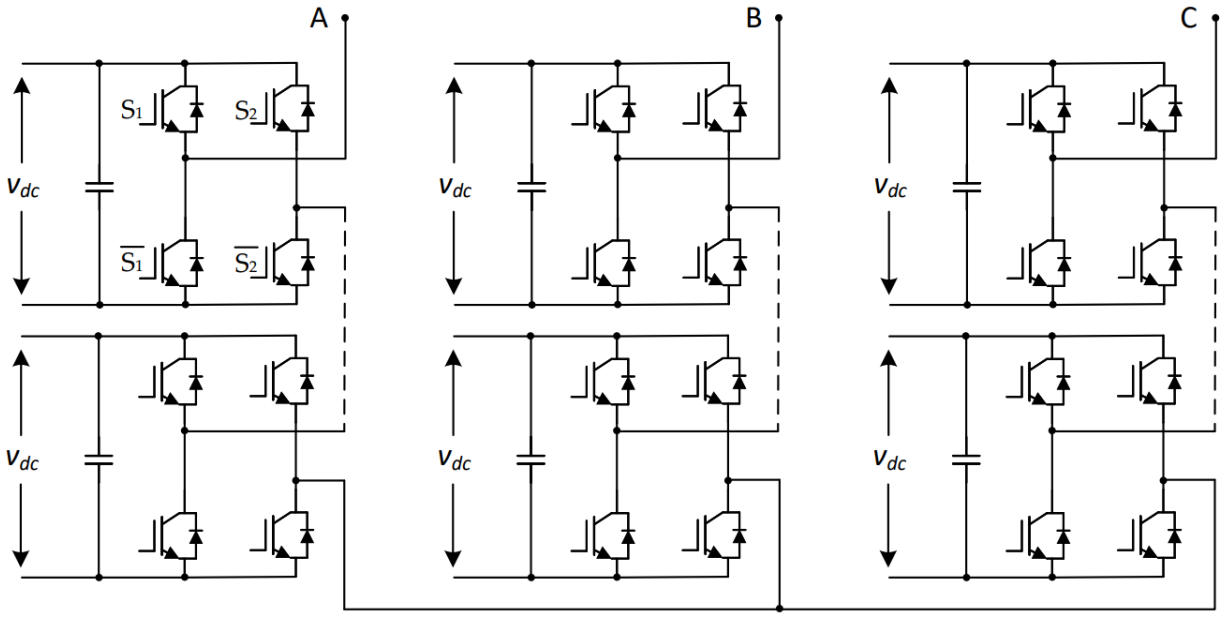


Figure 3.5 Cascaded H-bridge converter.

Still regarding the CHB, it is possible to obtain a higher number of voltage level using the same number of modules, which is obtained by maintaining a DC voltage ratio between the H-bridge power modules. This topology is referred as asymmetrical CHB. This topology minimizes the switching losses, thus improving the efficiency [55]. However, the modularity feature of the symmetrical CHB fades in the asymmetrical CHB due to requiring devices with different voltage ratings and thermal designs [56].

3.2.2.2 Cascaded Neutral-Point Clamped Converter (CNPC)

In Figure 3.6, is presented a three-phase cascaded neutral-point clamped converter. This topology was designed to overcome the loss of the modularity feature of the asymmetrical CHB and uses two three-level neutral-point clamped converter legs, forming H-bridge structures in each phase.

The voltage output in each phase is limited to five-level due to control complexity. The CNPC requires an isolated DC source for each phase, which can be obtained by a phase-shifting transformer with a diode rectifier. When in comparison with the CHB, for a five-level output, the CNPC only requires a DC source per phase, while the CHB requires two, however, the CHB possesses fewer devices, since the CNPC required two capacitors and four diodes in each phase.

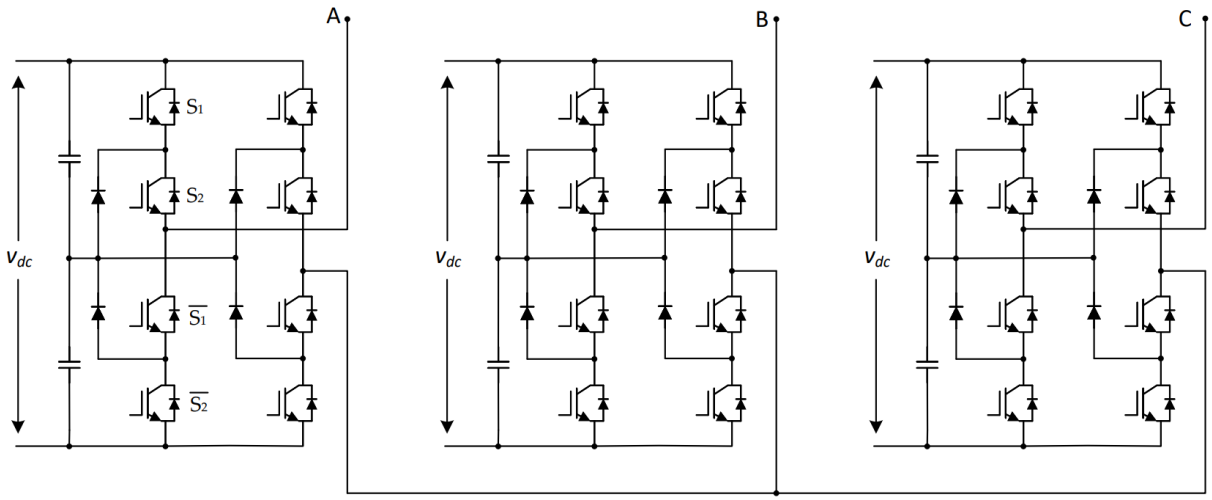


Figure 3.6 Cascaded neutral-point clamped converter.

3.2.2.3 Modular Multilevel converter (MMC)

As presented previously, cascaded topologies possess some features that integrated multilevel topologies do not, such as:

- Modular construction;
- Voltage and power scalability;
- Fault-tolerant operation.

As such, with these topologies it is possible for the converter to have higher rated voltage and power values without the series connection of semiconductors. However, as the DC-link of each module is composed by an isolated DC source obtained by complex transformers, with the raise of number of submodules also raises the number of DC sources necessary, the size and cost of the converter also increases.

For medium/high power systems, this becomes a major drawback, as the number of levels of the converter must be higher, so another multi-cell converter appeared, the modular multilevel converter (MMC). The MMC preserves the cascaded topologies features without the need of isolated DC-sources and phase shifting transformers, as the submodules are equipped with a DC-link capacitor.

In Figure 3.7, is presented a configuration of a MMC with the common nomenclature associated to this type of converter.

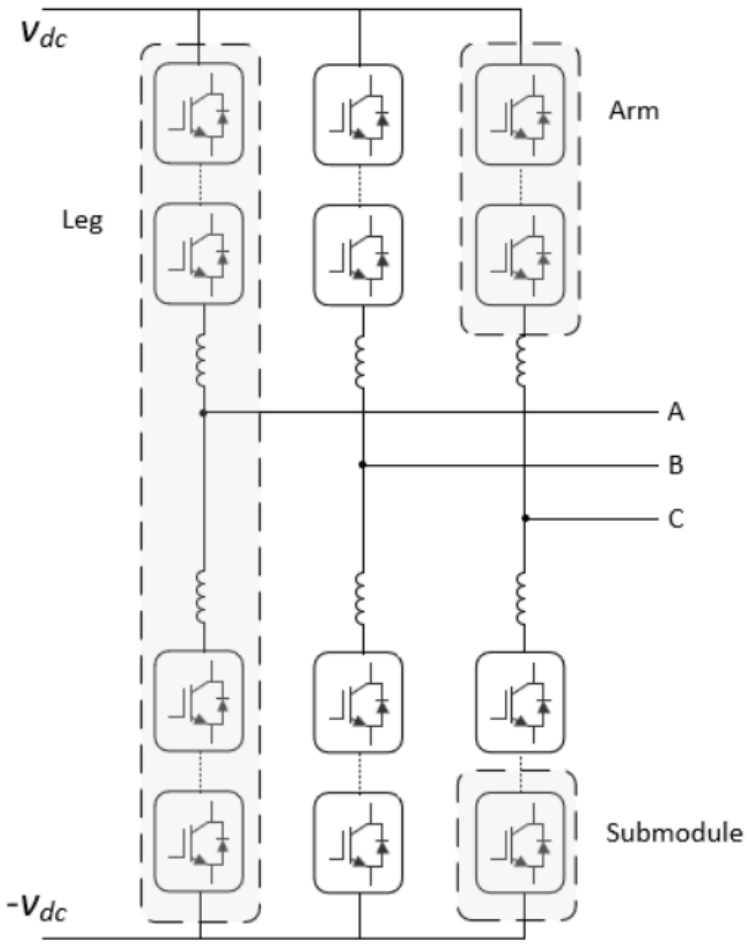


Figure 3.7 Configuration of a modular multilevel converter.

MMCs submodules are DC-AC power converters with capacitors on the DC-link. As such, there are many different topologies that can be used as submodules in MMC. In this section, the three main topologies will be discussed. In Figure 3.8, the schematic of a half-bridge submodule is presented.

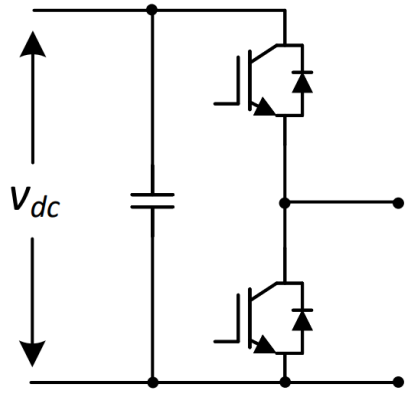


Figure 3.8 Half-bridge submodule schematic.

The half-bridge submodule is composed by two switching devices with antiparallel diodes and a DC capacitor. The output voltage is composed by two levels: 0 and V_{dc}. In Figure 3.9, the schematic of a full-bridge submodule is presented.

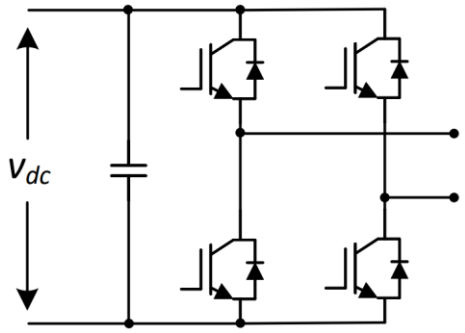


Figure 3.9 Full-bridge submodule schematic.

The full-bridge submodule is composed by four switching devices with antiparallel diodes and a DC capacitor. The output voltage is composed by three levels: - V_{dc}, 0 and V_{dc}. In Figure 3.10, the schematic of a flying capacitor submodule is presented.

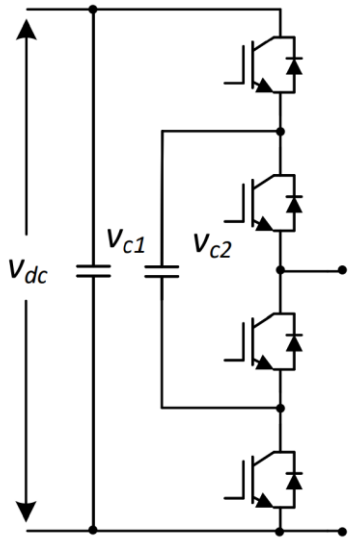


Figure 3.10 Flying capacitor submodule schematic.

The flying capacitor submodule is composed by four switching devices with antiparallel diodes and two DC capacitors with different voltage ratings. The output voltage is composed by three levels: 0, V_{c2}, and V_{c1}.

Among all the submodules topologies, HB is the most popular and commonly used in commercial products due to its simple construction, with a straightforward design and control. Furthermore, in operation, only one switching device is in conduction at the time, resulting in low power losses and high efficiency. However, due to its simplicity and reduced number of semiconductors, the output value only takes positive values, so it cannot support DC fault blocking.

The FB submodule possesses a similar complexity in the design and control to the HB, however, possesses two more switching devices, which lead to higher losses since there are two switching devices

in conduction at the same time, thus reducing the efficiency of the submodule. Due to the capacity of outputting both positive negative values, HB can limit the current during eventual DC faults.

The FC submodule possesses a more complex design and control than the HB and FB, requiring two DC capacitors with different rated voltages. In operation, a maximum of two devices are in conduction, thus the efficiency and power losses are like the FB. Similarly to HB, as the FC cannot output negative values, it has no DC-fault blocking. Table 3-5 presents a summary of the differences between the diverse types of submodules.

Table 3-5: MMC Submodule comparison.

	Half-Bridge	Full-bridge	Flying capacitor
Number of output levels	2	3	3
Number of switching devices	2	4	4
Number of DC capacitors	1	1	2
DC-link voltage	$2V_{dc}$	V_{dc}	$2V_{dc}$
Output frequency	f_s	$2f_s$	f_s
Unipolar operation	No	Yes	No
DC fault blocking	No	Yes	No
Control complexity	Low	Low	High

3.3 Modulation Techniques for MMC

When it comes to PWM techniques for power electronics converters with 2 or 3 voltage levels, the options available in the literature are extensive. However, regarding in specific the PWM techniques for MMC, and since it requires distinct stages for each submodule, it results in more complex techniques for synthesizing the desired multilevel waveform [49]. The modulation consists of a comparison between a modulator waveform, which takes the form of the desired signal, and one or more triangular carrier waveforms, where their disposition varies depending on the technique. In this section, it is presented a comparison between the most conventional, namely the phase-shift carrier PWM and the level-shift carrier PWM.

3.3.1 Phase-Shift Carrier PWM

In phase-shit carrier PWM, all the triangular carrier signals have the same: frequency; peak-to-peak amplitude; and offset value. However, varies the phase disposition of the triangular carriers. The carrier signals are disposed with a $2\pi/N$ phase-shift between them, where N represents the number of

submodules in each arm of the MMC. Figure 3.11, illustrates the referred modulation technique for a MMC with two submodules in each arm, therefore with N = 2.

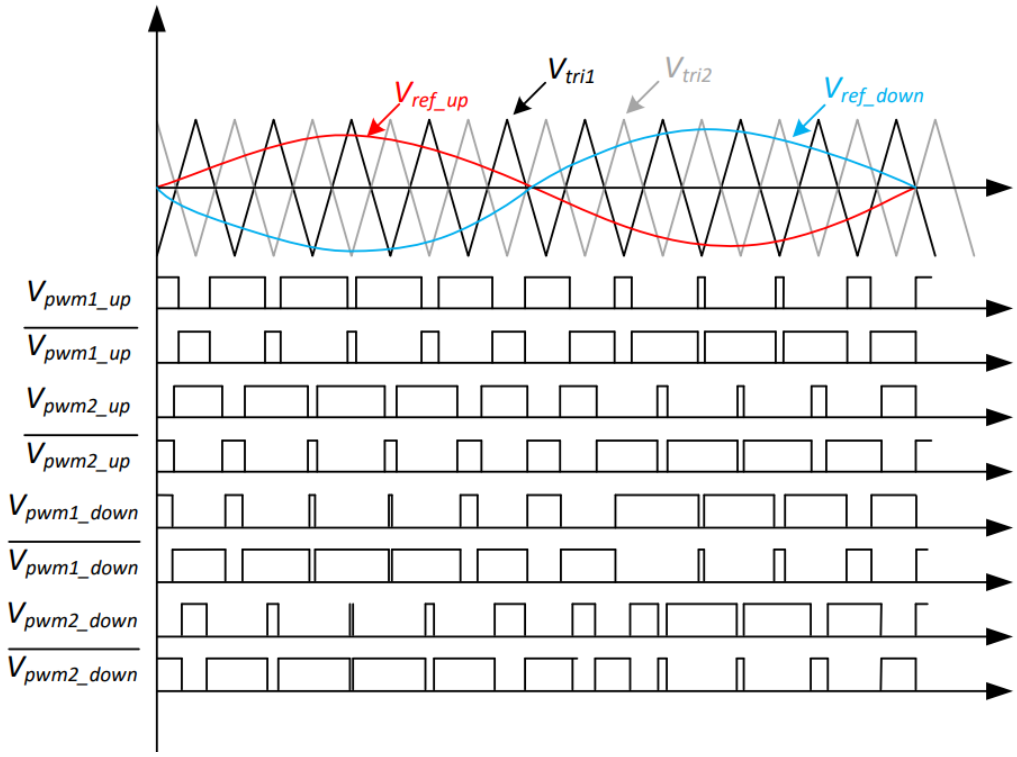


Figure 3.11 Phase Shift Carrier Modulation technique for a MMC with two submodules in each arm.

For a better understanding of the technique through visualization of the waveforms of the carrier signals and the modulator signals, the modulator signals were disposed with 50 Hz frequency and the carrier signals with 500 Hz frequency. In a practical implementation, typically, this frequency would be higher, in the order of kHz to a few tens of kHz. In this figure, V_{ref_up} corresponds to the reference of the up arm, V_{ref_down} to the corresponds to the reference of the down arm, while V_{tri1} and V_{tri2} corresponds to the reference of the necessary two carriers with a phase disposition of 180 degrees. The variables V_{pwm1_up}, V_{pwm2_up}, V_{pwm1_down}, V_{pwm1_down}, as well as the corresponding complementary values, corresponds to the gate pulse-pattern of the IGBTs that constitute the MMC with two submodules.

This technique is remarkably interesting for MMC, due to some unique characteristics [4]:

- Even power losses across the submodules of the converter;
- Minimizes DC-link ripple;
- Provides a natural balancing of submodule capacitors voltage at the carrier frequency.

Although being very advantageous for multilevel topologies, this technique does not possess sensibility to DC-link voltage fluctuations.

3.3.2 Level-Shift PWM

In level-shift PWM, the required number of triangular carriers is the same when compared with the phase-shift, with all the triangular carrier signals sharing the same frequency and peak-to-peak amplitude, however, varying in the offset value since they are vertically disposed. There are many variants of this technique, where the phase disposition of the triangular carries varies. Similar to the figure presented to the phase shift carrier technique, Figure 3.12 presents the level-shift modulation for a MMC with two submodules in each arm. Also in this technique, with the objective of facilitating the understanding, 50 Hz modulator signals and 500 Hz carrier signals were considered.

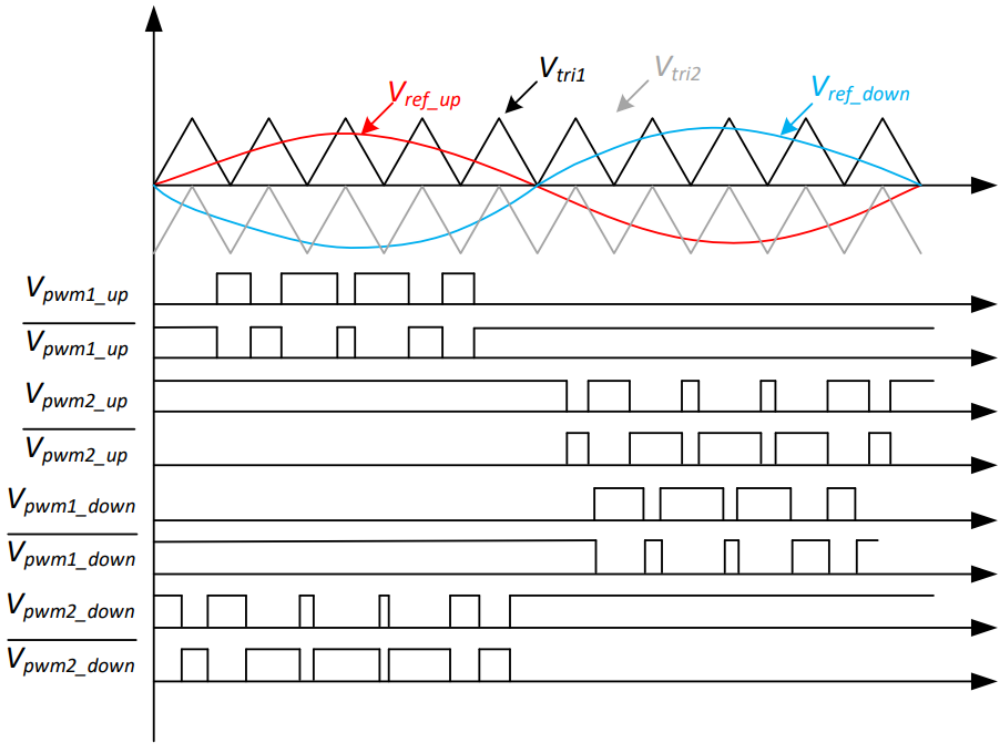


Figure 3.12 Level Shift Modulation technique for a MMC with two submodules in each arm.

This technique is very popular in conventional multilevel converters, not being very advantageous however for the MMC, since it causes uneven power losses across the submodules, resulting in voltage ripple in the submodule capacitors and high circulating currents [57].

3.4 Control Techniques

Regarding the control of power electronics converters, digital control schemes allow an efficient, safe, and reliable operation, with higher dynamic and steady-state performance. In Figure 3.13, is presented a block diagram where the different steps of controlling and MMC are shown.

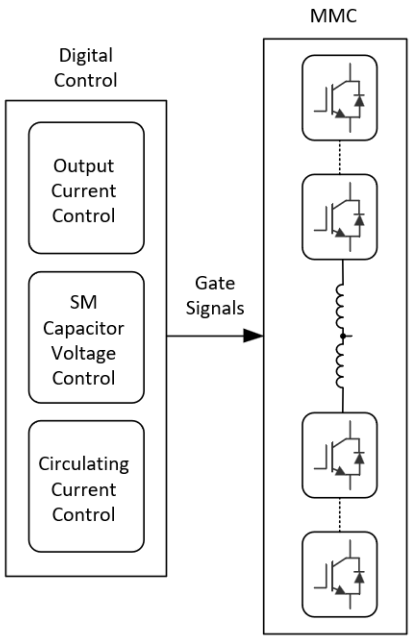


Figure 3.13 MMC control system block diagram.

The focus lies on the control of the output current, as well as the balancing of the capacitor voltage across every submodule since the functioning of the converter depends on these two controls. Regarding the circulating currents, it is considered a secondary control since the function of the converter does not depend on it. However, it is also important because the circuiting currents lead to higher RMS values on the arm currents, resulting in power losses and decrease of efficiency. Furthermore, they are more relevant in three phase systems, since they appear due to voltage difference across the capacitors of submodules in the different legs, thus not being one of the focuses of this dissertation.

3.4.1 PI Controller

The PI controller aims to control the MMC current according to a current reference. In a first stage, it is calculated the error between the reference current and the output current of the MMC and then, such error serves as input for the PI controller, which consists of a proportional and integral gains, and an integral parcel, presented in the equation (3.1) [58]:

$$V_{mod} = K_p\left(i_{ref} - i_{out}\right) + K_i \int_0^t \left(i_{ref} - i_{out}\right)dt \tag{3.1}$$

This technique requires the tuning of the proportional and integral gains for a better performance of the system, keeping in mind that the dynamic response is limited by the PI gains as well as the steady state error, which can be mitigated, but never fully extinguished [59]. The output of the PI controller corresponds to the input of the modulation block, V_{mod}, whose output results in the command signals for the switching power devices, as presented in Figure 3.14.

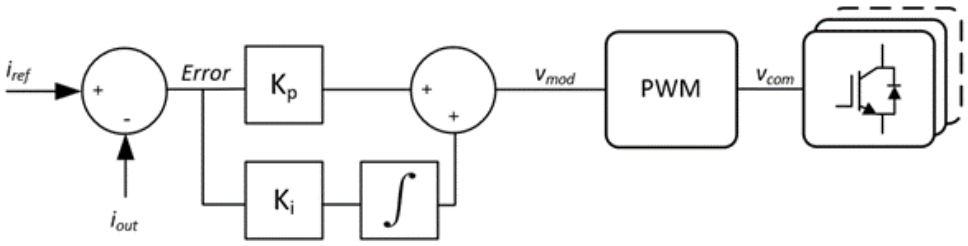


Figure 3.14 PI controller with SPWM modulation.

As the command signals, v_{com}, are generated by a modulation technique, the switching frequency of the semiconductors has a fix value, making it easier for the dimensioning of the passive filters of the converter.

3.4.2 Model Predictive Control

The model predictive control calculates the desired control variables based on an electrical model of the converter in study, without any integral error associated as appear in the PI controller [60]. This type of controller, typically, presents fast transient response, and small-steady state error, due to its fast dynamic response [61]. In order to be able to obtain the electrical model of the MMC, its equivalent circuit is presented in Figure 3.15. As mentioned before in this chapter, the circulating current will be neglected for a simplification of the model.

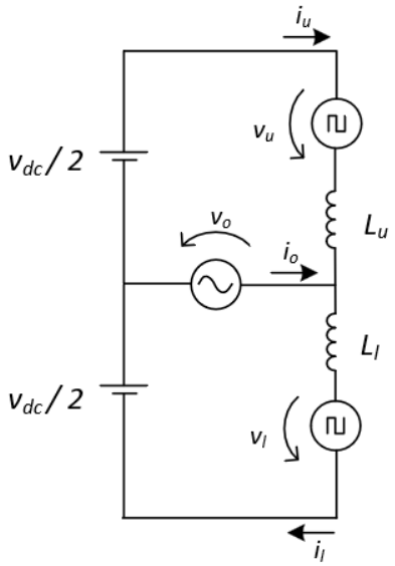


Figure 3.15 MMC equivalent circuit.

Applying Kirchhoff's voltage law on the equivalent circuit, disregarding the conduction and switching losses on the semiconductors, the equations obtained are the following:

$$v_o = -L_u \frac{di_u}{dt} - v_u - i_u R_u \tag{3.2}$$

$$v_o = L_l \frac{di_l}{dt} + v_l + i_l R_l \tag{3.3}$$

The predictive control is a current based controller, in which the variable in control in each equation is the current flowing in the arm.

$$i_{u_{error}} = i_{u_{ref}} - i_u \tag{3.4}$$

$$i_{l_{error}} = i_{l_{ref}} - i_l \tag{3.5}$$

The voltage drop in the internal resistors of the inductive filters of the arms of the MMC can be neglected ($i_l R_{Ll}$ and $i_u R_{Lu}$), due to the low value they have, thus resulting in a simplification of the equations without any significant error associated.

$$v_o = -L_u \frac{d\left(i_{u_{ref}} - i_{u_{error}}\right)}{dt} - v_u \tag{3.6}$$

$$v_o = L_l \frac{d\left(i_{l_{ref}} - i_{l_{error}}\right)}{dt} + v_l \tag{3.7}$$

Separating the differential part in the previous equations:

$$v_o = -L_u \frac{di_{u_{ref}}}{dt} + L_u \frac{i_{u_{error}}}{dt} - v_u \tag{3.8}$$

$$v_o = L_l \frac{di_{l_{ref}}}{dt} - L_l \frac{i_{l_{error}}}{dt} + v_l \tag{3.9}$$

Since the control is performed by a microcontroller, the equations need to be in discrete time, instead of linear time. The discretization of the derivative can be done using Euler's method:

$$\frac{dx}{dt} \cong \frac{x(K) - x(K-1)}{\Delta t} \tag{3.10}$$

Where K indicates the present sample and K-1 the previous sample. By substitution the in the previous equations:

$$v_u[K] = -\frac{L_u}{\Delta t}\left(i_{u_{ref}}[K] - i_{u_{ref}}[K-1] - i_{u_{error}}[K]\right) - v_o[K] \tag{3.11}$$

$$v_l[K] = -\frac{L_l}{\Delta t}\left(i_{l_{ref}}[K] - i_{l_{ref}}[K-1] - i_{l_{error}}[K]\right) + v_o[K] \tag{3.12}$$

Simplifying the previous equations:

$$v_u[K] = -\frac{L_u}{\Delta t}\left(i_u[K] - i_{u_{ref}}[K-1]\right) - v_o[K] \tag{3.13}$$

$$v_l[K] = \frac{L_l}{\Delta t}\left(i_{l_{ref}}[K-1] - i_l[K]\right) + v_o[K] \tag{3.14}$$

Disregarding the circulating currents, according to the current direction arbitrated in the equivalent circuit, the current in each arm are described by the following equations:

$$i_u = -\frac{i_o}{2}, \quad i_l = \frac{i_o}{2} \tag{3.15}$$

Substituting in the previous equations, and introducing T_s as the sampling period, the final equations are obtained:

$$v_u[K] = -\frac{L_u}{T_s}\left(\frac{i_{u_{ref}}[K-1]}{2} + i_u[K]\right) - v_o[K] \tag{3.16}$$

$$v_l[K] = \frac{L_l}{T_s}\left(\frac{i_{l_{ref}}[K-1]}{2} - i_l[K]\right) + v_o[K] \tag{3.17}$$

The final equations for the reference voltage across each arm in each sampling period are used as the modulator signals for the PWM signals generation, adding the necessary offsets for the capacitor balancing in each submodule, which is discussed in Section 3.4.3.

3.4.3 Capacitor Balancing

Regarding the control of the voltage balancing across the capacitor of the submodules for a single phase MMC with only one arm, as is the case of study, two different steps must be contemplated: the individual voltage control across each submodule presented in Figure 3.16, and the arm voltage control presented in Figure 3.17 [62].

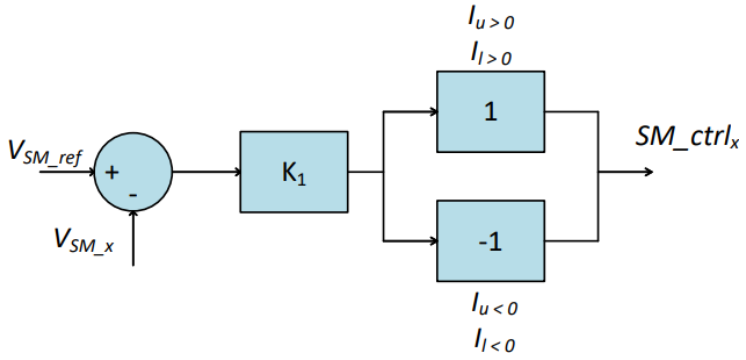


Figure 3.16 Individual voltage control of the capacitor in each submodule.

The individual voltage control consists of a proportional control of the voltage of each submodule to follow the voltage reference. Depending on the current direction, the output of the controller is multiplied by one if the current in the arm in which the submodule is integrated is positive, or -1 if the current is the arm is negative. As such, there is a controller unit for every submodule of the MMC.

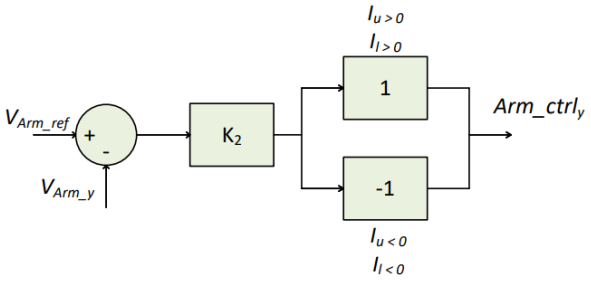


Figure 3.17 Voltage control across each arm.

Regarding the arm voltage control, it is similar and works as a complement to the individual voltage control, as it consists of a proportional control of the sum of the submodule voltages across each arm to keep the voltage in each arm balanced. Identical to the individual voltage control, the output of the controller is multiplied by -1 if the current in the arm is negative. Regardless the number of submodules per arm, there are two controller units for arm voltage control. For the control of the output of the MMC, two different approaches are discussed in this chapter: using a PI controller for the current control presented in Figure 3.18, and using the predictive model control Figure 3.19.

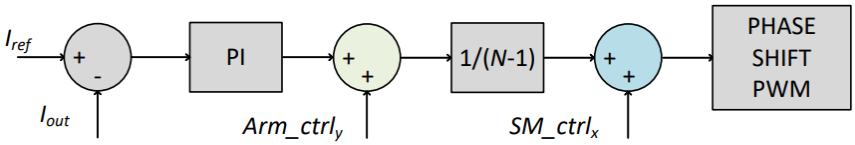


Figure 3.18 Gate signal generation for each submodule using a PI controller.

Regarding the PI controller, as mentioned earlier in chapter 3.4.1, the value of the actual current is subtracted to the reference current value and goes through the proportional and integral gains. Using model predictive control, the final equations are used instead, thus generating the reference signals in both approaches. Then it is summed the output of the arm voltage controllers, followed by a gain of $1/(N-1)$, where N relates to the number of submodules in each arm. Finally, the output of the controller of the voltage of each submodule is summed to the reference signal, having created the modulators for the phase shift PWM. This technique consists of the phase shift of the triangular carriers of each arm in $360/(N-1)$ degrees, as discussed in chapter 3.3.1 [49].

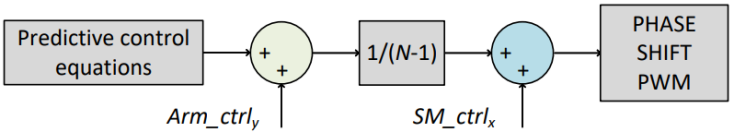


Figure 3.19 Gate signal generation for each submodule using model predictive control.

3.5 Conclusion

This chapter relates to a more practical approach of the project since it is focused on convertor topologies and methods to control them. At first, the multilevel topologies were discussed, presenting the advantages and disadvantages of this family of power converters, when comparing to the conventional. Many different topologies were approached, and it was possible to see that although each possessing their own characteristics, they all share some features among them.

Inside the multilevel family, a special converter topology was presented, the MMC. This converter possesses modular construction, being made by submodules. Three different topologies for the submodule were discussed, each presenting advantages and disadvantages from each other. The selected topology for the submodules of this dissertation was Half-Bridge due to the simplicity of the control of each submodule, since the system itself is already very complex.

After presenting the topologies for the power converters, two main modulation techniques used were presented, phase shift carrier and level shift carrier, since are the more used in multilevel topologies. Phase shift carrier modulation was the technique selected for the development of the project.

Finally, two control techniques were presented, PI controller and model predictive control. Regarding the advantages and disadvantages presented, the model predictive control will be carried out in the development of the converter in study of this dissertation. Although being very advantageous in many aspects in comparison with the traditional power converters, the MMC presents some technical challenges that result in a complex control system. Such challenges include:

- Control of the voltage across the submodule, including pre-charging processes, voltage balancing and voltage ripple control.
- Circulating currents in the legs, which appear from the difference in the voltage between the arms and only flows in the converter legs, increasing power loss in the converters and the ripple in the capacitors of the submodules.
- Submodule fault tolerance.
- Design constraints when it comes to the values of the arm inductance and the submodule capacitor. The arm inductance is responsible for filtering the switching frequency harmonics in the arm, as well as limiting the DC short-circuit current. The submodule capacitor is usually projected from the tradeoff between the capacitor voltage ripple and the cost of the capacitor itself.

Chapter 4

Operation Principle and Computational Simulations of the Proposed Topology

4.1 Introduction

Once having selected the topology for the power converter, it is of paramount importance to conceive its validation recurring to computational simulations to assess the functioning of the power converter as a whole. Computer simulation is a powerful resource, which is crucial for the understanding of the behavior of the system in the various stages, either initial response, transitory events, or steady state response. Furthermore, the simulation is also a crucial tool to test the control algorithms, as well as tuning its parameters in order to provide the better performance for the system. As such, the simulation software must be highly explored to be able to make the most of it in order to develop a simulation model as close as possible to a real implementation, regarding the non-linear components present in the system.

Regarding power electronics, computational simulations also allow a safe environment for the users, since in this area there are high values on power and energy at stake, which can be harmful for human in case of a failure. Furthermore, it also prevents damage in the electronic components, which would lead to an additional economic cost and possible waiting time from the component distributors. As such, the simulation environment provides a safe and interactive way to study the converter and all the algorithms associated prior to their implementation in practice.

Along the course of this chapter, an explanation of the selected topology is presented in detail in order to better understand the functioning of the power converter in an intuitive way, recurring to the electrical schematic. Then two major simulations with MMC are presented with different number of submodules per arm, and different power ratings, to understand the functioning of the power converter in both cases. Results are presented for diverse types of loads in a first interaction, followed by grid interface where the grid synchronization algorithms are explored. At last, the capacitor voltage across each submodule will be presented for both converters.

4.2 Operation Principle

The selected topology for the present dissertation was an MMC with two half-bridge submodules in each arm. In Figure 4.1, it is presented the electrical diagram of the chosen topology, followed by the output voltage levels of this power converter. This section intends to intuitively explain the functioning of this topology, recurring to the electrical diagram.

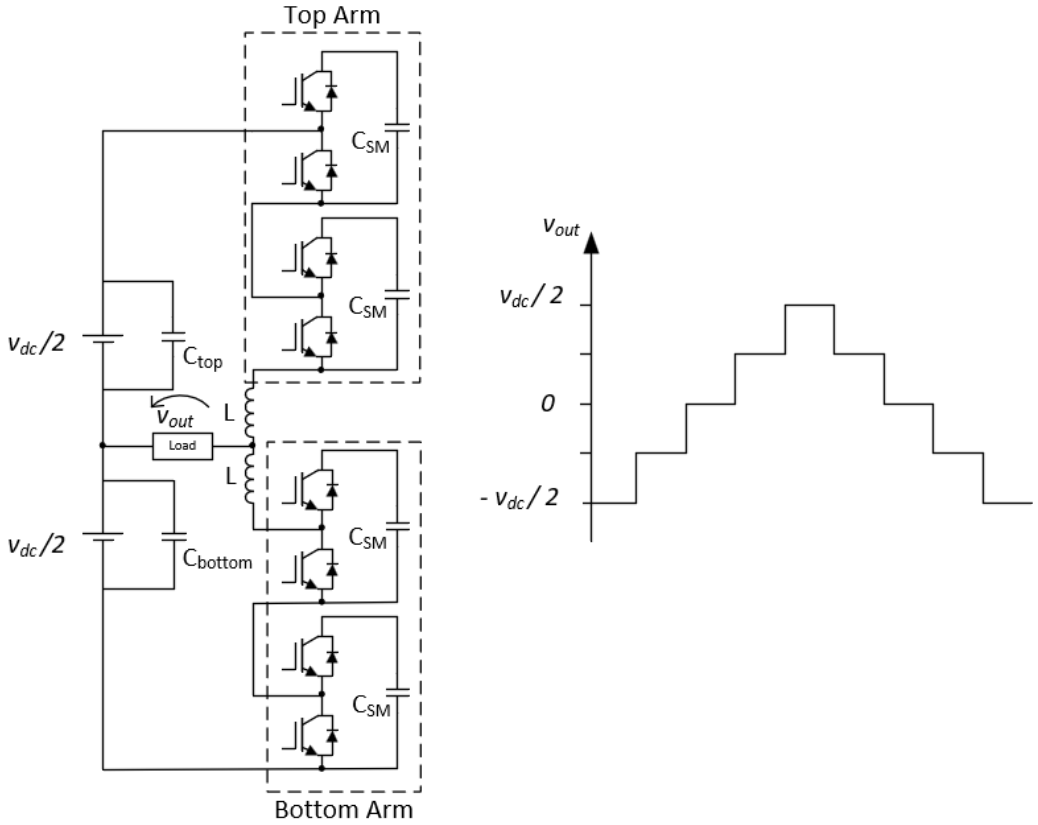


Figure 4.1 Electrical diagram of the MMC with two submodules in each arm and output voltage levels generated.

Each submodule in composed by two IGBTs, only one conducting at a time. When the upper IGBT conducts, the submodule is considered active and when the lower IGBT conducts, the submodule is considered bypassed. The activation of the upper submodules results in a positive voltage, while the activation of the lower submodules results in a negative voltage. The output voltage of the MMC is the sum of both arm voltages, considering the voltage division in the coupling coils. The number of voltage levels in the output of the MMC using this topology is equal to $N+1$, where N refers to the number of submodules. As such, there are five voltage levels possible on the output of the converter: $-v_{dc}/2$, $-v_{dc}/4$, 0, $v_{dc}/4$ and $v_{dc}/2$. The production of some levels can be made using different combination of submodules active and bypassed, which created redundant states, which are useful for the balancing of the voltages across the capacitors of the submodules.

For the synthesis of level -$v_{dc}/2$ both upper arm submodules must be bypassed, while both lower arm submodules are active. As such, there are no redundant states for this level. Figure 4.2, presents the synthesis of this level.

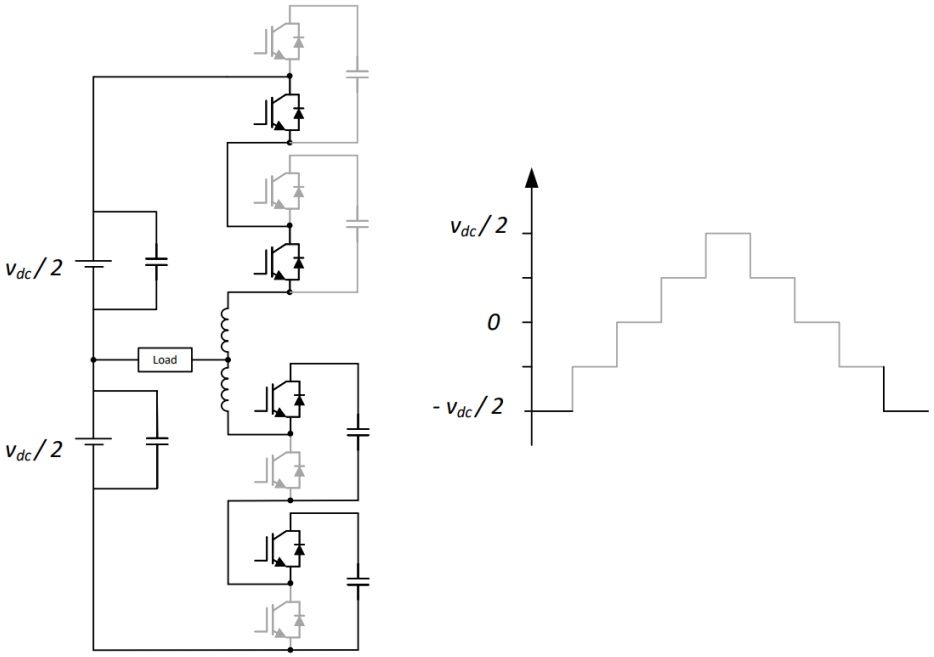


Figure 4.2 MMC switching devices state for the synthesis of level -$v_{dc}/2$.

For the synthesis of level -$v_{dc}/4$, both lower arm submodules must be active and in the upper arm one submodule must be active while the other is bypassed. This results in two redundant states. In Figure 4.3, it is presented one of such states for the synthesis of level -$v_{dc}/4$.

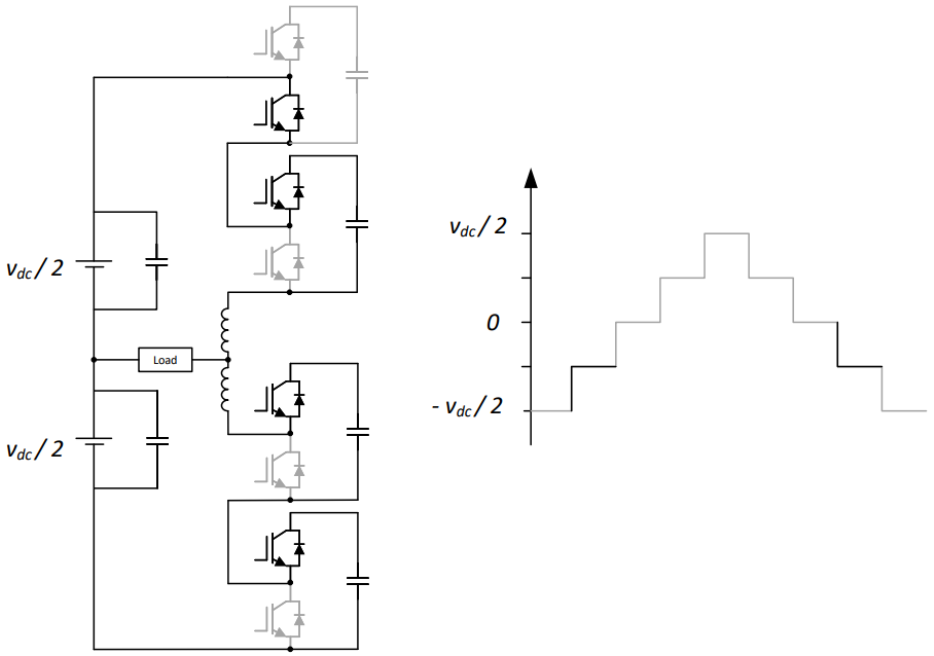


Figure 4.3 MMC switching devices state for the synthesis of level -$v_{dc}/4$.

For the synthesis of level 0 it is necessary to have the same number of submodules active in the upper and lower arm. As such, there are six redundant states in the generation of this level. In Figure 4.4, it is presented the synthesis of the level 0 with one active submodule in each arm.

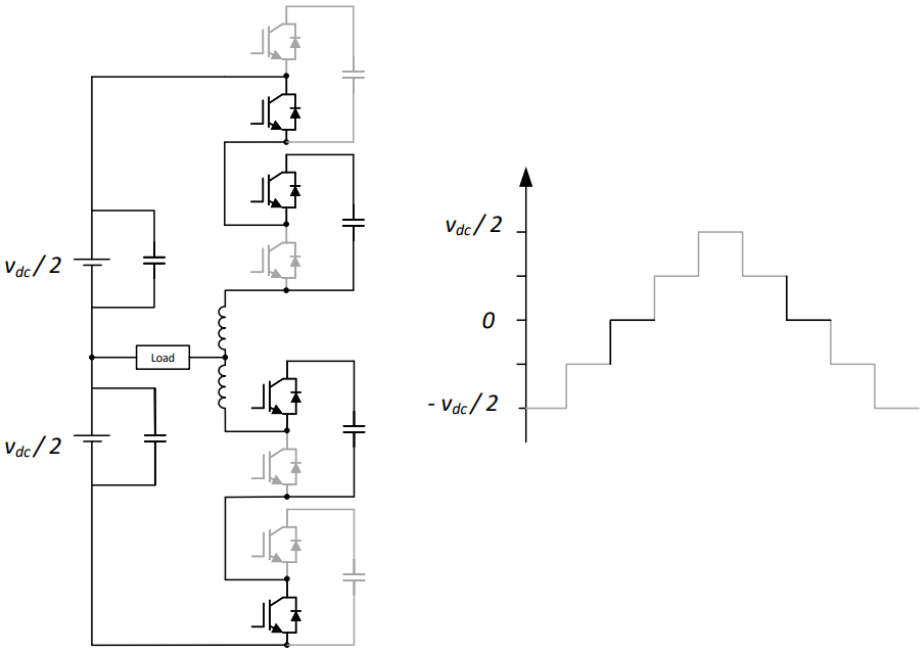


Figure 4.4 MMC switching devices state for the synthesis of level 0.

For the synthesis of level $v_{dc}/4$, both upper arm submodules must be active and in the lower arm one submodule must be active while the other is bypassed. This results in two redundant states. In Figure 4.5, it is presented one of such states for the synthesis of level $v_{dc}/4$.

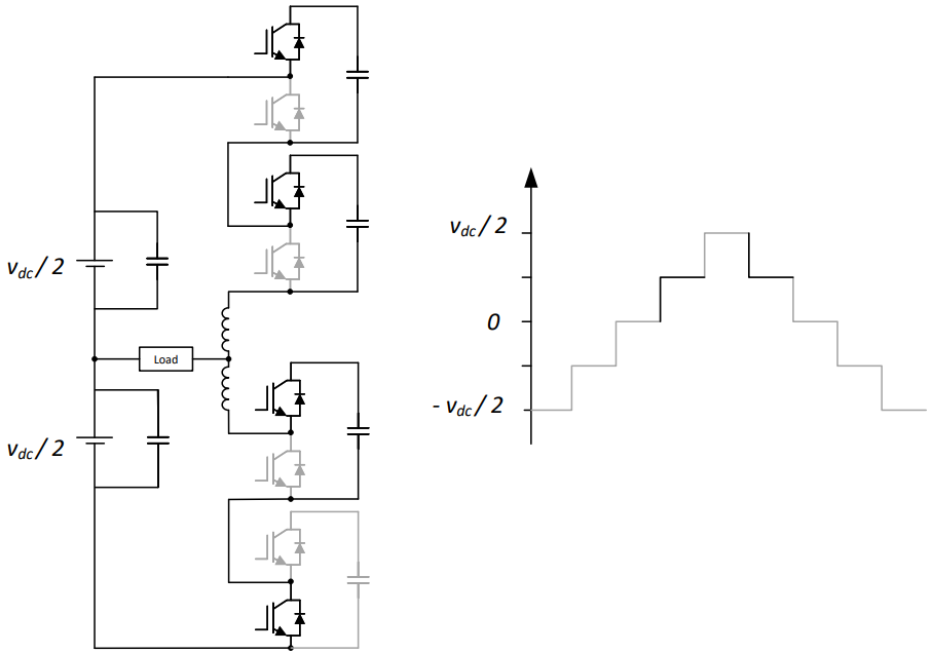


Figure 4.5 MMC switching devices state for the synthesis of level $v_{dc}/4$.

For the synthesis of level $v_{dc}/2$ both lower arm submodules must be bypassed, while both upper arm submodules are active. As such, there are no redundant states for this level. Figure 4.6 presents the synthesis of this level.

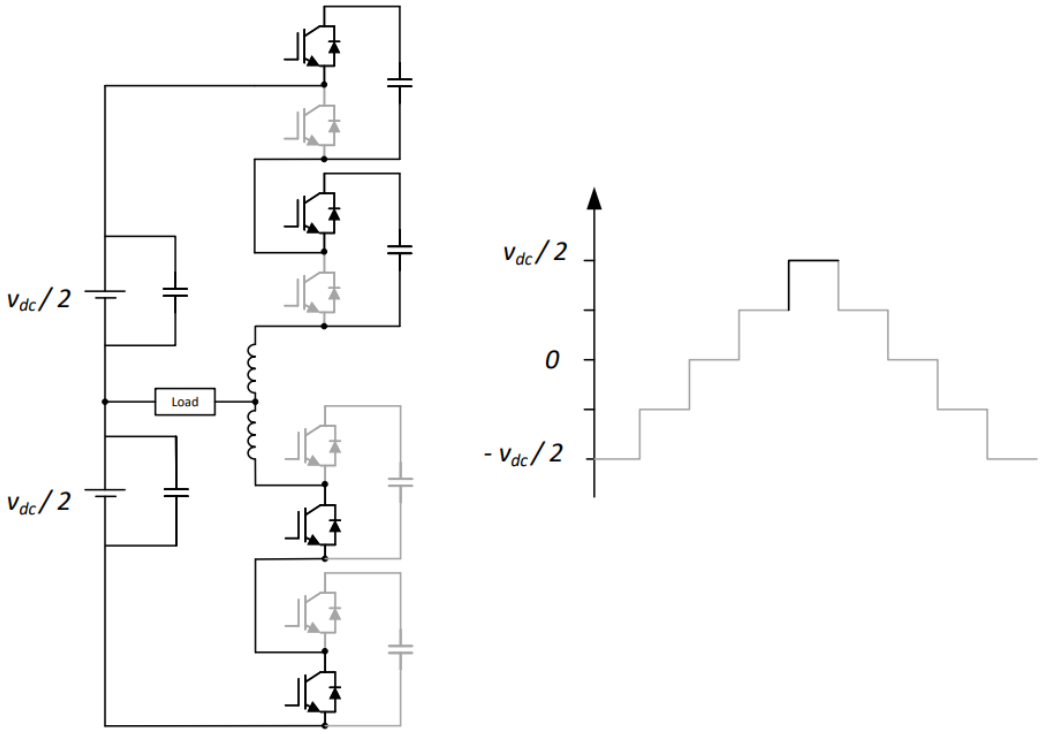


Figure 4.6 MMC switching devices state for the synthesis of level $v_{dc}/2$.

4.3 Simulation Model

The simulation model was developed recurring to PSIM software and in order for a better visualization concerning the size of the model, it is presented in the following two figures. In Figure 4.7, is presented the power stage of the converter, containing a total of eight half-bridges converters, four in each arm, properly connected with the inductive filters and with the electrical power grid. To approach the simulation to the real conditions, the components used in each submodule possess some real non-idealities, allowed by the software: the IGBTs used in the simulation model were designed to match with the ones used in practice, IKZA50N65RH5 [63] and the possibility to input the internal resistance of the passive components, such as capacitors and inductors. The model also possesses two capacitors with different values of capacity to better simulate the dynamic behavior of the converters. Finally, each submodule is equipped with a voltage sensor to monitor the voltage across the capacitors.

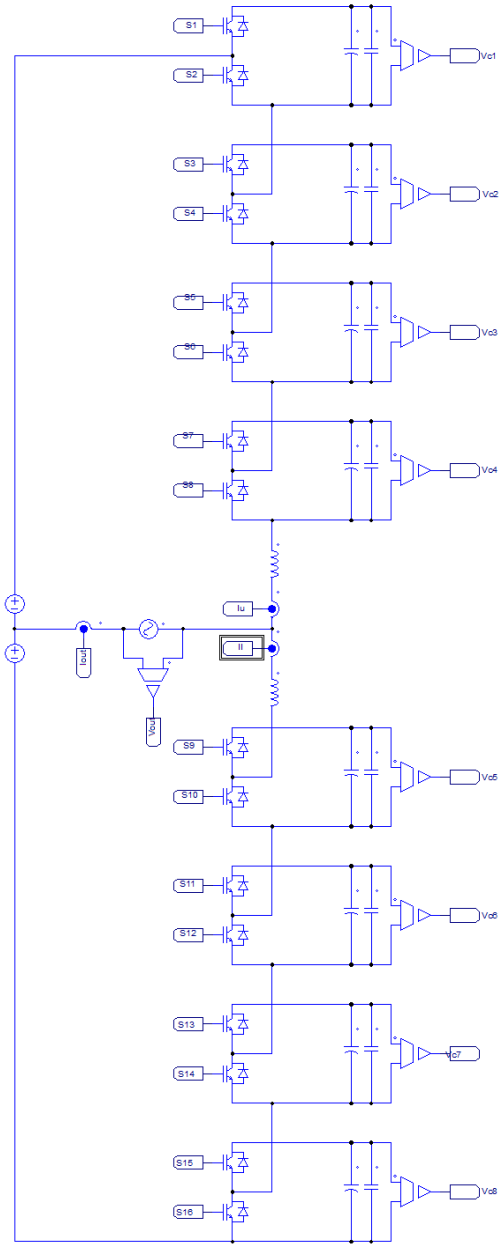


Figure 4.7 Simulation Model of the MMC with four submodules in each arm in software PSIM.

Regarding the system itself, it is equipped with a split DC-link made by DC power supplies, an AC sinusoidal voltage supply to simulate the electrical power grid, and sensors for voltage and current.

In Figure 4.8, is presented the control and modulation necessary for the functioning of the power converter. In the left it is possible to observe the C block, a block available in the PSIM software that allows the simulation of a digital signal processor (DSP), due to the similarities they share, i.e. coding of the control of power circuits in C programming language, and the possibility to read inputs and generate outputs. Another interesting feature in this software is the possibility of selecting the sampling frequency of the C block to better simulate the reality with the processing limitations of the DSPs. This is made using a zero-order holder (ZOH) in the input of the C block. This block is a big advantage when it comes to

stepping up from simulation to implementations, since a big part of the code is portable. In the right it is presented the modulation technique phase shift carrier that is responsible for the generation of the PWM signals for all IGBTs. As introduced in Section 3.4.3, the balancing of the capacitor voltage of the submodules is made by the sum or subtraction of calculated offsets to the modulator wave, which is also presented in this diagram. The sampling frequency was set to 50 kHz, and the switching frequency to 20 kHz. Using a flipflop D and AND gates, it is possible to simulate the deadtime of the semiconductors, which was set to 1 µs.

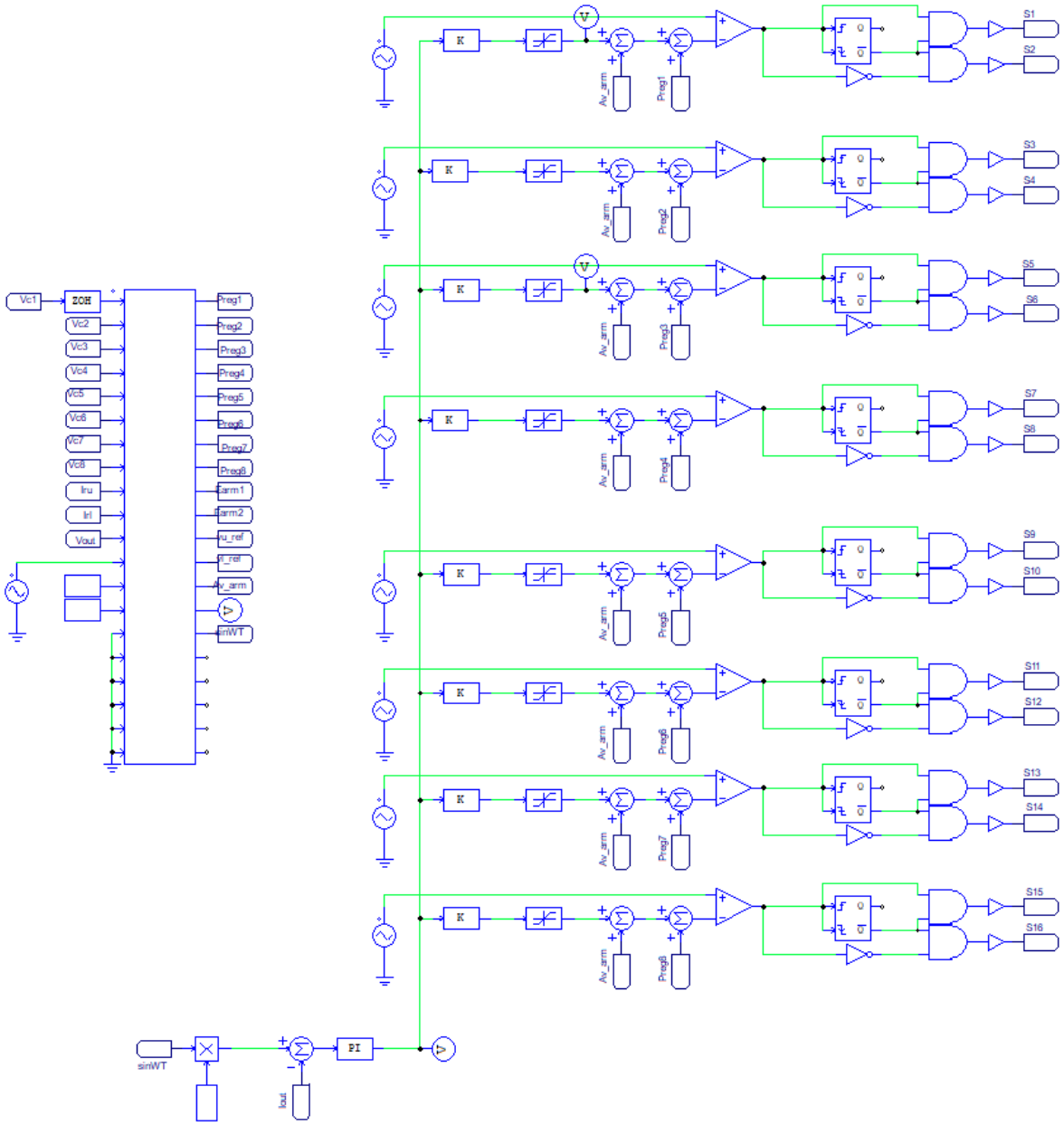


Figure 4.8 Simulation Model of the control and modulation for a MMC with four submodules in each arm in software PSIM.

4.4 Electrical Grid Synchronization Techniques

When the goal is to interface with the electrical power grid, one of the mandatory requirements is the synchronization of the control algorithms with the electrical power grid. This is due to power quality issues, namely high frequency noise in the voltage, and mostly the fact that the voltage signal in the electrical power grids suffers from harmonic distortion provoked by the influence of the connection of non-linear loads which creates harmonic distorted currents in the line impedance, thus creating the referred distortion in the voltage signal. With the existence of such problems the synchronization to the electrical power grid though a steady signal is of paramount importance for the interface of power converters.

There are many different techniques in the literature to address such issue, being two of the most common the zero-crossing method and the phase locked loop (PLL). The zero-crossing method, as the name proposes, consists of detecting the moment where the fundamental voltage passes through zero. As this phenomenon only happens two times per fundamental signal, this technique results in a slow dynamic response for the system [64]. Regarding the PLL, is consists of the synchronization in both phase and amplitude with the electrical power grid voltage signal to create a stable sinusoidal signal which can serve as reference for the control of the power converters [65]. In Figure 4.9, it is presented a block diagram for a PLL algorithm. It is composed by three distinct parts: a phase detector, a low pass filter and a voltage-controlled oscillator (VCO).

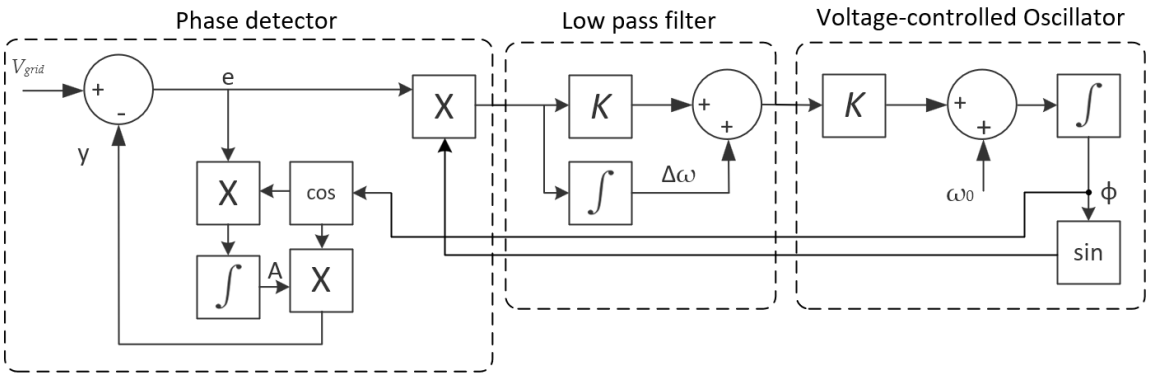


Figure 4.9 Block diagram of a PLL algorithm.

The phase detector measures the phase shift between the input and output signal, which is denominated as error. The error goes throw the low pass filter to a voltage-controlled oscillator which generates the output signal. Adjusting the proportional and integrative gains in the phase detector, low pass filter and oscillator, this loop allows not only the synchronization with the phase of the input signal, but also with its amplitude.

As presented is Figure 4.10, the phase synchronism occurs after the first cycle, while the amplitude takes two cycles for stablishing. It is possible to contemplate that the PLL generates a sinusoidal signal (0.4% $THD_{\%f}$) from a distorted signal (4.5% $THD_{\%f}$).

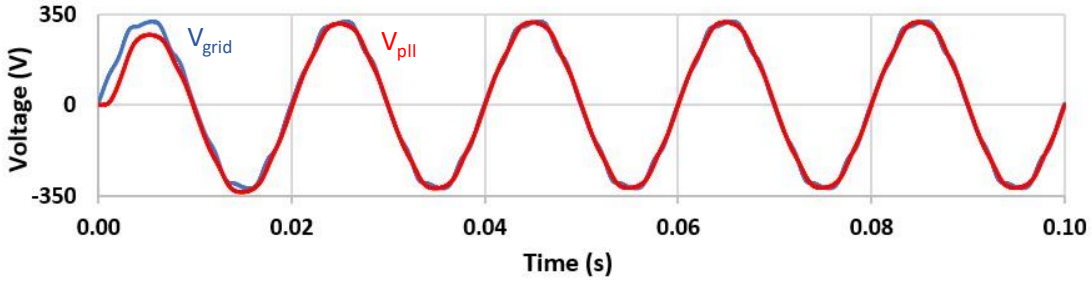


Figure 4.10 PLL synchronization with electrical power grid.

The central frequency (ω_0) of the VCO is defined by the user to match the frequency of the electric power grid, which in the Portuguese electrical system corresponds to 50 Hz. The PLL synchronizes the output signal with the frequency value indicated, allowing slight variations in the input signal. In Portugal, the norm NP EN 50160 dictates that during 99 % of time, the maximum value for medium frequency variation every 10 seconds of the power grid voltage is ±1 % of the nominal value [66], [67]. Hence, the PLL algorithm was tested in extreme conditions to access its behavior in such cases.

In Figure 4.11, it is presented the algorithm response to the referred frequency variations. Figure 4.11(a) regards the results for the PLL synchronism with a fundamental frequency of a power grid of 50.5%, while Figure 4.11(b) presents the same results for a fundamental frequency of 49.5%, thus validating the PLL algorithm.

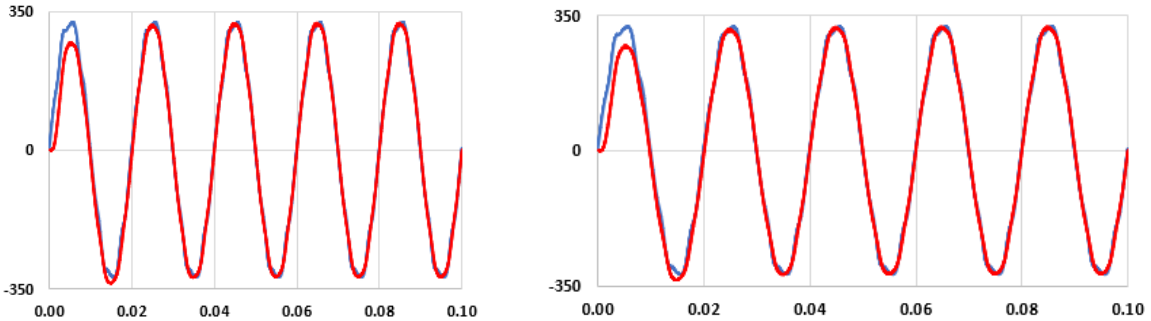


Figure 4.11 Power grid voltage and output PLL signal at a fundamental frequency of: (a) 50.5 Hz, (b) 49.5 Hz.

The PLL also generates a unitary sine wave which is extremely helpful for the generation of sinusoidal reference values, which is of paramount importance to synthesize a sinusoidal current waveform in the output of the converter, to inject energy in the electrical power grid.

4.5 Simulation Results

In Table 4-1, the electrical parameters introduced in the simulation presented in Figure 4.7, are summarized. The aim is to interface with the electrical power grid, as such, the DC-link voltage must be higher than the peak voltage of the electrical grid voltage (325 V). The DC link voltage was arbitrated to 400 V, resulting in a DC voltage across the submodules of 200 V, as there are four submodules in each arm.

Table 4-1: Electrical parameters introduced in the simulation model for an MMC with four submodules in each arm.

Power Rating	P	5 kW
DC-Link Voltage	v_{dc}	400 V
Submodule DC Voltage	V_{SM}	200 V
Inductive filters	L_u, L_l	5 mH
Submodule capacitors	C_{SM}	5 mF
Output Voltage (Electrical Power Grid)	v_{out}	230 V
Output Frequency	f	50 Hz
Switching Frequency	f_{sw}	20 kHz
Sampling Frequency	f_s	50 kHz
Semiconductor deadtime	d	1 µs
Modulation index	m	81.25 %

The modulation index equation is presented in (4.1), where A_m regards the maximum amplitude of the modulator signal, and A_c represents the amplitude of the carrier signals, hence resulting in a modulation index of 81.25 %, since the carrier signals peak amplitude is the same as the DC link voltage.

$$m_a = \frac{A_m}{A_c} \tag{4.1}$$

The first simulation performed intended to access the behavior of the MMC while injecting energy in the electrical power grid. To do so, an initial analysis and discussion of the simulation results was approached with the system operating in steady state conditions, at constant 5 kW output power. The output voltage of the converter is imposed by the voltage in the grid, and, in order to simulate the system in a more realistic environment, several harmonics were added in the electrical power grid voltage signal in the simulation model. As the power converter is injecting energy in the grid, it is notorious that the output current of the MMC (represented in color red in Figure 4.12) is in phase opposition with the grid voltage (represented in color blue).

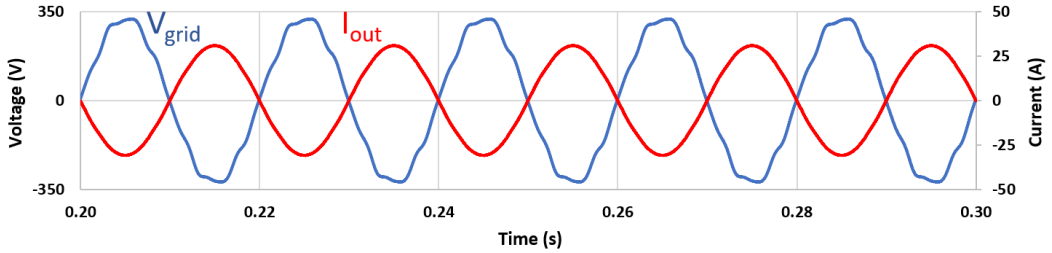


Figure 4.12 Simulation results for an MMC with 4 submodules in each arm at a rated power of 5 kW in steady state in electrical power grid interface operation: Output Voltage and Output Current.

Despite the distortion presented in the voltage signal, with a $THD_{\%f}$ of 4.07%, such phenomena does not appear in the output current of the converter, presenting a $THD_{\%f}$ of 0.43% at 21.78 A RMS, which results in a power rating of the expected 5 kW. As the converter in study is modular, the power is distributed throughout the different submodules, each contributing for the output voltage, and consequently current of the converter. In Figure 4.13, it is presented the voltage across the inductive filters of the MMC.

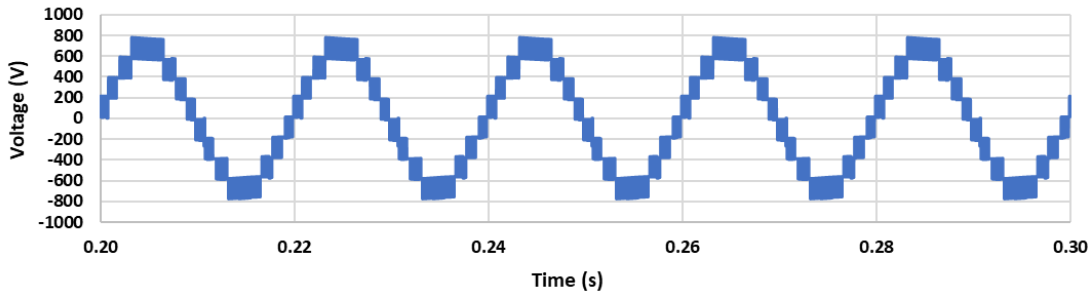


Figure 4.13 Simulation results for an MMC with 4 submodules in each arm at a rated power of 5 kW in steady state in electrical power grid interface operation: Voltage levels generated by the power converter measured between the inductive filters.

This waveform is of paramount importance since it represents both the waveform being synthesized and voltage levels in the output of the converter, created by the operation of the different submodules in all stages of functioning. It is possible to visualize nine voltage levels, which is equal to the total number of submodules present in the MMC, plus the level 0, where all submodules are bypassed. To ensure a power even power distribution among the submodules, the voltage across each submodule must remain as steady as possible. This is made by monitoring and balancing the submodules capacitors, as is demonstrated in Figure 4.14.

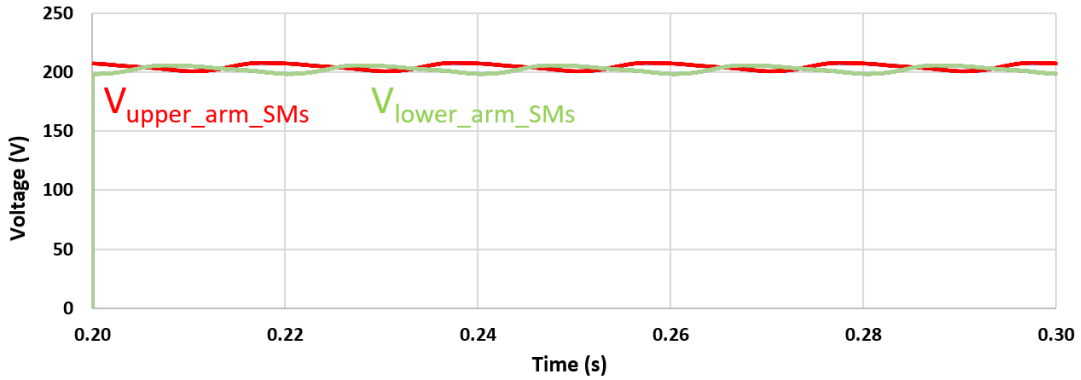


Figure 4.14 Simulation results for an MMC with 4 submodules in each arm at a rated power of 5 kW in steady state in electrical power grid interface operation: Voltage across each submodule capacitors.

As there are four submodules in each arm, the voltage across each capacitor was referenced to 200 V, and it is possible to observe that both the upper arm capacitors and the lower arm capacitors converge to the reference. The red signal refers to the submodules in the upper arm, while the green signal refers to the submodules in the lower arm. Each signal visible in Figure 4.14, represents the four submodules of the referent arm, since the signals are overlayed, and only one is visible for each arm. As previously explained, the balancing of the submodules capacitors is made using the medium voltage value across each of them, thus allowing the voltage to oscillate at 100 Hz between controlled parameters, thus appearing the ripple. To better access the voltage behavior in each submodule, a detailed result is presented in Figure 4.15, where it is possible to observe the ripple of the capacitors voltage, which is approximately 7 V, representing 3.5% of the steady state value.

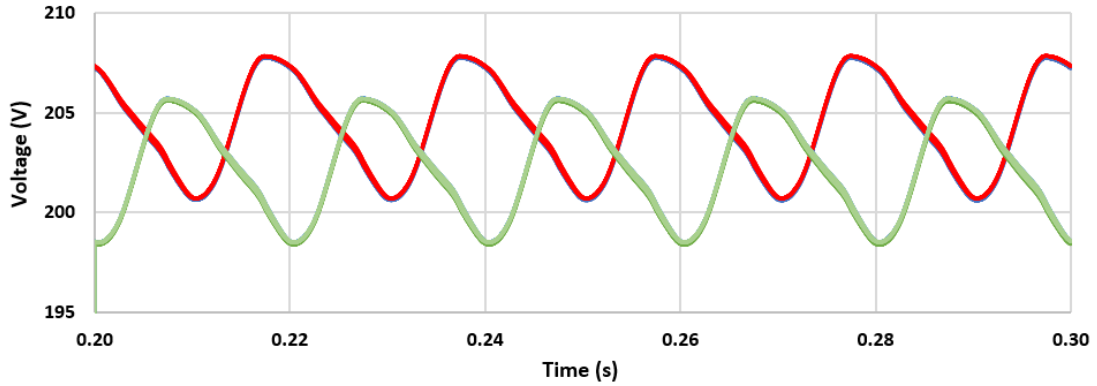


Figure 4.15 Simulation results for an MMC with four submodules in each arm at a rated power of 5 kW in steady state in electrical power grid interface operation: Ripple voltage across each submodule capacitors.

The results demonstrated thus far allow the validation of the power converter in steady state in terms of power circuit and control algorithms. However, as different loads with different power ratings can be connected in different time instances, it is necessary to study the behavior of the MMC in transition stages. Hence, a second simulation was carried out where all the parameters of the converter were maintained,

changing however the power rating in the time instant $t = 0.3$ s from 5 kW to 10 kW, which allows the simulation of more loads being connected to the power converter.

In Figure 4.16, it is presented the grid voltage (represented in blue) and the output current (represented in red) of the MMC while injecting energy in the electrical power grid, with a reference power rating changing to double in $t = 0.3$ s.

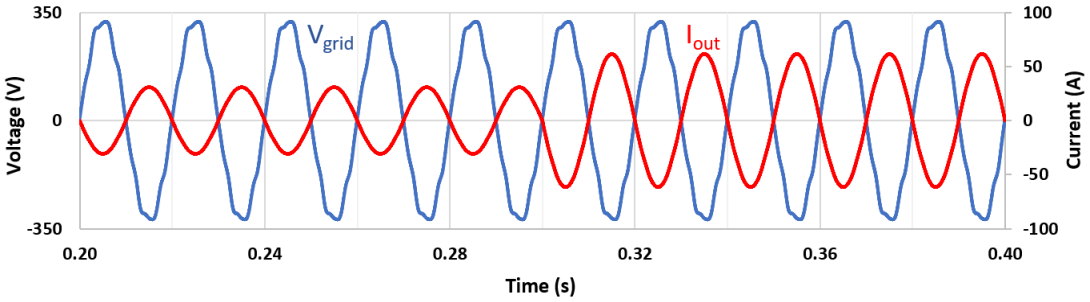


Figure 4.16 Simulation results for the response of an MMC with 4 submodules in each arm transitioning from 5 kW rated power to 10 kW in electrical power grid interface operation: Output voltage and output current.

As observed, similar to steady state operation, as the MMC is injecting energy in the electrical power grid, the current and voltage output of the converter are placed in phase opposition. When the power reference changes, as the voltage remains the same, the current doubles its value. As the transition occurred in a moment where both the current and the voltage are crossing zero, the response of the current is smooth, and the current waveform remains sinusoidal in every cycle. The RMS value of the current changed from 21.78 A to 43.56 A. Regarding the voltages across the submodules, in Figure 4.17, it is possible to observe that the medium value follows the reference value after the transitory event, with an increase in the ripple, as the power raises.

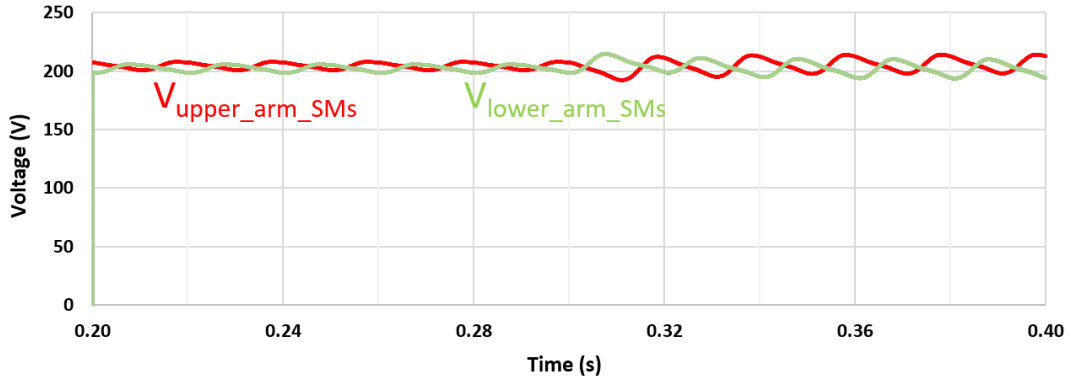


Figure 4.17 Simulation results for the response of an MMC with 4 submodules in each arm transitioning from 5 kW rated power to 10 kW in electrical power grid interface operation: Voltage across each submodule capacitors.

In Figure 4.18, it is presented the detail of the ripple voltage across the capacitors of all submodules. Analyzing such waveforms, the ripple after the transition raises from 7 V to approximately 15 V, denotating

a substantial percentual change of 3.5% to 7.5%. The ripple can be attenuated recurring to the use of larger capacitors.

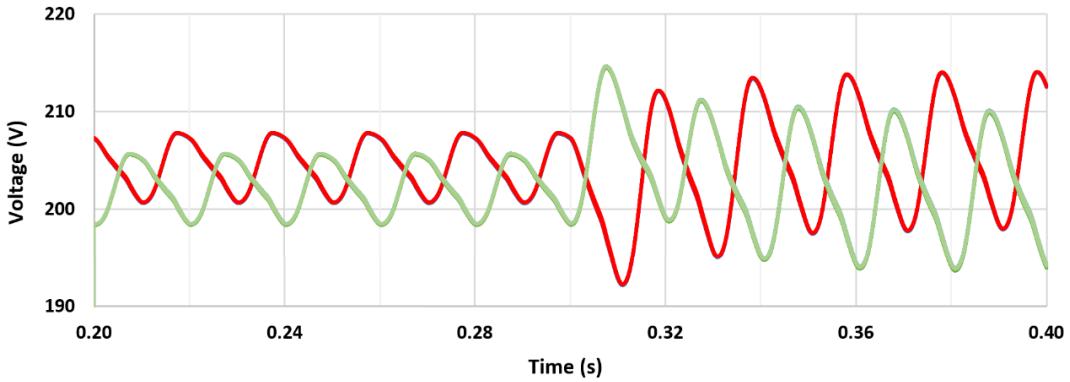


Figure 4.18 Simulation results for the response of an MMC with 4 submodules in each arm transitioning from 5 kW rated power to 10 kW in electrical power grid interface operation: Ripple voltage across each submodule capacitors.

The demonstrated simulated results allow the comprehension and validation for a single phase MMC with four submodules in each arm when interfacing with the electrical power grid, controlling the rated power of the converter with an even distribution of the power among all the submodules since their voltage remains balanced.

4.6 Reduced Scale Simulation

The previous results related to a simulation of a high scale single phase MMC with four submodules in each arm, operating with high power ratings. However, the prototype developed in the scope of the present dissertation is equipped with two submodules in each arm and it is not intended to operate at such power ratings. Hence, a second simulation model was developed in order to analyze the behavior of the power converter that was projected in this dissertation. In Table 4-2, are presented the parameters introduced in the simulation model in order to make it closer to the prototype implementation.

Table 4-2: Electrical Parameters introduced in the simulation model for an MMC with two submodules in each arm.

Power Rating	P	300 W
DC-Link Voltage	V_{dc}	120 V
Submodule DC Voltage	V_{SM}	120 V
Inductive filters	L_u, L_l	5 mH
Submodule capacitors	C_{SM}	1.6 mF
Output Voltage (Electrical Power Grid)	V_{out}	50 V
Switching Frequency	f_{sw}	20 kHz
Sampling Frequency	f_s	50 kHz
Semiconductor deadtime	d	1 µs
Modulation index	m	81.25%

As the converter possesses two submodules in each arm, the voltage across each submodule must be the same as the DC-link voltage [68], 120 V. Using such DC-link voltage, the output voltage of the converter must be comprehended between the -120 V and 120 V, requiring a stepdown transformer for 50 V to the electrical power grid. Similar to the MMC with 4 submodules in each arm, the output voltage of the MMC with 2 submodules in each arm measured between the inductive filters demonstrates the different voltage levels that the converter produces, as presented in Figure 4.19. As foreseen, the output voltage of the converter is composed by five different levels.

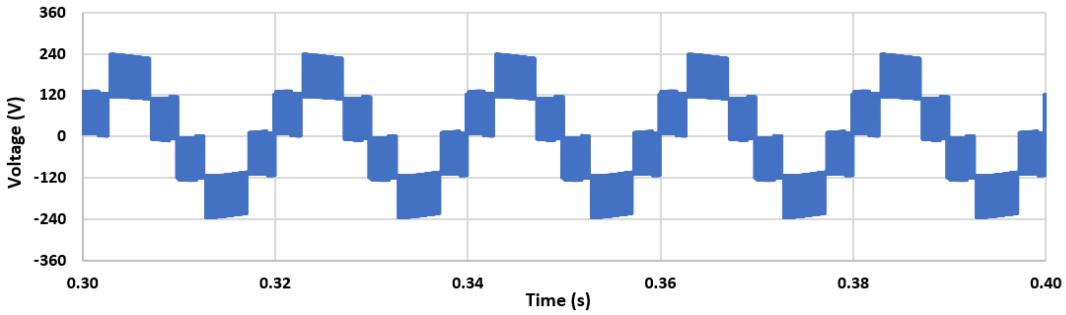


Figure 4.19 Simulation results for an MMC with 2 submodules in each arm at a rated power of 300 W in steady state in electrical power grid interface operation though a step-down transformer to 50 V: Voltage levels generated by the power converter measured between the inductive filters.

In Figure 4.20, two signals are presented: the grid voltage through a step-down transformer to 50 V at blue and the output current of the power converter injecting 300 W in the electrical power grid. Even though the number of submodules of the converter is smaller to the previously presented, the output current possesses a clean sinusoidal waveshape with a $THD_{\%}$ of 0.6%, while the electrical power grid remains distorted. The current possesses an RMS value of 6.1 A.

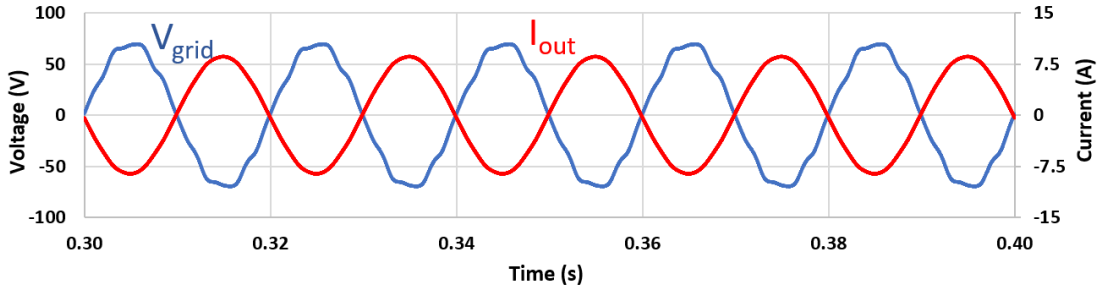


Figure 4.20 Simulation results for an MMC with 2 submodules in each arm at a rated power of 300 W in steady state in electrical power grid interface operation though a step-down transformer to 50 V: Output voltage and output current.

In order for the current to follow its reference with a reduced distortion, as well as evenly distributing the power among all the submodules, the voltage across all the submodules must be the same. In Figure 4.21, the voltage across every submodule is presented.

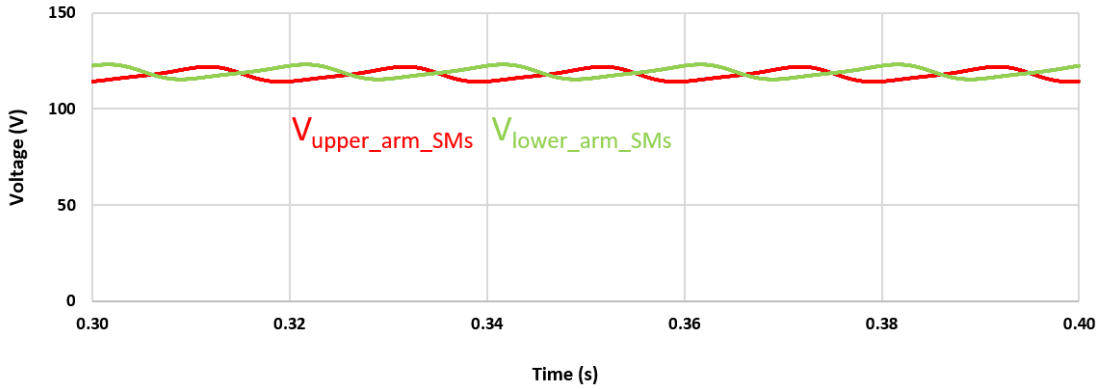


Figure 4.21 Simulation results for an MMC with 2 submodules in each arm at a rated power of 300 W in steady state in electrical power grid interface operation though a step-down transformer to 50 V: Voltage across each submodule capacitors.

The red waveform represents the upper arm submodules voltage, while the green waveform represents the lower arm submodules. Even though only two waveforms appear to be presented, for each arm, the capacitor voltage is the same, hence the signals are overlaid. As foreseen, the voltage across all the submodules follow the reference with natural 100 Hz oscillation.

4.7 Conclusion

In this chapter, after an explanation of the functioning of the proposed topology, it was presented a simulation model that has proven to be crucial for the validation of the power converter in terms of both power and control. In a first stage it was presented the algorithm of the PLL used, that allows the synchronization with the electrical power grid, in order to generate a reference current signal in phase opposition with the grid voltage, for the injection of energy in the electrical power grid.

Regarding the simulations of the converter itself, two distinct stages were approached. Starting with a single phase MMC with four submodules in each arm, operating at 5 kW in steady state, and introducing a transitory event for double the power to study the behavior of the converter to tune and validate the control algorithm of current output, as well as voltage balancing control across the submodules. Besides the functioning itself of the converters, with the computational simulations it was possible to understand how the submodules influence the output, and the 100 Hz oscillation in the voltage of the capacitors of each submodule.

In a final stage, it was developed a simulation model for a reduced scale MMC, using two submodules in each arm, same as the prototype that was developed in the scope of the present dissertation. This allowed the comprehension of the system itself, as well as providing a forecast of the results that are expected in the practical implementation.

Chapter 5

MMC Prototype Implementation

5.1 Introduction

Throughout the present chapter it is presented the development and implementation of the prototype in the laboratory of the Group of Power Electronics and Energy (GEPE) for the chosen topology of power converter, a MMC with two submodules in each arm, to interface with the electrical power grid.

For an organization purpose, this chapter is divided into two different sections. In a first section, the power stage will be approached, where it is discussed the driver implementation, the submodules PCBs, and their integration in the power converter. Furthermore, the main components utilized are displayed and described in terms of functionality and justification for its choice. In a second section, the control circuitry and software are briefly discussed.

The main focus of this dissertation is to study and learn about the MMC, a converter that is in vogue in research in the field of power electronics, with potential to expand to further applications. As such, the hardware developed in the GEPE laboratory in the scope of this dissertation was delineated to be as modular as possible, as well as portable to other projects in the laboratory. This means that each submodule is equipped in a single PCB, a generic half-bridge converter, and the control part possesses PCB separately as well, as is further discussed in this chapter.

5.2 Power Stage

This section focuses on the implementation of the power stage of the MMC, with a detailed characterization of the components that contribute to the integration of the power converter. In terms of hardware development in this dissertation, the power stage is subdivided in three categories, the submodules, the drivers, and the passive elements. In order to develop the necessary hardware for the project, it was first necessary to establish the maximum ratings at which the prototype can operate. In Table 5-1, such parameters are established.

Table 5-1 Power converter maximum ratings.

Power	500 W
DC Voltage	200 V
Output current	10 A
Switching Frequency	20 kHz

5.2.1 Submodule Implementation

The first step to implement the submodules was the selection of components. The chosen topology dictates that the submodules are but simple half-bridge converters, as such, each submodule must be equipped with two semiconductors and one capacitor.

Regarding the selection of semiconductors, it is one of the most important decisions when it comes to power electronics projects since this is the main element responsible for the performance of the desired waveforms through its commutations. Over the last two decades a new type of semiconductor (SiC - Silicon Carbide) appeared to overcome some limitations presented by the MOSFETs and IGBTs, thus resulting in the significative raise of switching frequencies in power converters, lowering the power losses. This results in an increase of the system efficiency as well as providing a mechanical improvement of the encapsulation, allowing less parasitic and better thermal behavior. Nowadays, more and more it is recommended for the projects to use of small equipment with high power density, in order to ensure a better performance in a reduced encapsulation. On that note, with the developments in SiC technology, a new semiconductor appeared based on gallium nitride (GaN), focusing on applications with much higher frequencies, however possessing lower voltage ratings.

Keeping in mind the project requirements, after extensive research of semiconductors, the IGBT IKZA50N65RH5 [63] was selected for the power converter. This is an IGBT with a special particularity, since it possesses four pins, encapsulated in the PG-TO247-4-3 package as presented in Figure 5.1. The difference to normal encapsulation lies in the existence of a second emitter pin, the kelvin emitter. This pin allows the split of the current for each pin, one for the driver and the other for the power resulting in less ringing and eliminates the effect of parasitic inductance shared by the power circuit and gate driver circuits [69]. This effect is significantly increased at higher switching frequencies, and can create false triggers, increasing switching losses, thus diminishing the system efficiency, or in an extreme case can lead to the destruction of the IGBT by overload of the gate characteristics.

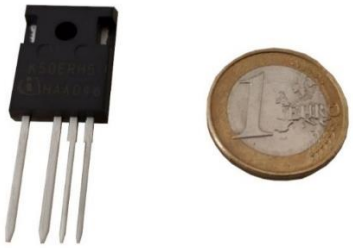


Figure 5.1 Selected IGBT for the development of the submodules: IKZA50N65RH5.

Regarding the maximum key parameters of the selected IGBT, the collector-emitter voltage (V_{CE}) is 650 V with saturation voltage of 1.65 V, the collector current (I_c) is 56 A. In the datasheet, all data is presented for a gate resistor of 12 Ω, with whom the sum of the turn-on, turn-off, rise time and fall time is equal to 225 ns. Furthermore, this IGBT possesses an attractive Safe Operation Area (SOAr) curve, which relates the operation voltage, current and the temperature.

Regarding heatsinks for the IGBT, the selected was CR201-50 [70], since it fits the purpose of the modularity concept while successfully allowing the heat to dissipate from both IGBTs of a submodule. The selected heatsink possesses a thermal resistance of 3.3 °C/W. Since the back of the IGBTs is connected to the drain and both share the same heatsink, it is of paramount importance to maintain the insulation between them. As such, even though the heatsink possesses an insulator film, a mica insulator was used in the backs of each IGBT.

In order to protect each submodule from overvoltage, high transient power surges and voltage transients when switch off and in the deadtime, each IGBT was connected with a transient voltage suppressor (TVS) in antiparallel. For this dissertation, the chosen TVS was 1.5KE100A[71], a 1500 W pulse peak TVS with fast response time and 100 V normal break voltage. As the voltage rating of the submodules were set to 200 V, two TVS were connected in in series in each IGBT because the voltage drop of each one is less than the internal diode), thus making a break voltage of 200 V. The TVS serve only as a protection, so current is not meant to flow through them in normal functioning, instead of going through the reverse diodes of the IGBT, thus the connection of series TVS being advantageous since it creates a path with higher impedance than the reverse diodes of the IGBT. Furthermore, the internal capacitance if reduced by half by the series connection.

Regarding the capacitor selection, the value was selected recurring to computational simulations in order to maintain the ripple below 10% of the DC-link voltage at all stages, including in transitory events. The simulation of the voltage balance across the capacitors proved to be quite complex, thus resulting in a selection of over dimensioned capacitors, since the raise of the capacitor value causes the voltage to

oscillate at a slower pace, thus resulting in in a decrease of ripple and allowing a better control of the system. As such, consulting the existent material in the laboratory in order to use components in stock, the chosen capacitor for the application was a 450 V, 820 µF United Chemi-Con capacitor [72]. It is highly advantageous the use of capacitors in parallel since not only does the equivalent capacity increase, but also results in a significant decrease in the equivalent series resistance (ESR) and equivalent series inductance (ESL), reducing the losses and the heat into the capacitor and the raising the self-resonance for higher frequency. The decrease in the ESR, allows a raise in the RMS value of the current in the DC-link, which enables the operation with fewer power losses. On the other hand, the decrease of the ESL causes an increase in the resonance frequency, thus resulting in a superior dynamic response for the capacitors. These factors are of paramount importance to electrolytic capacitors since they possess high values of ESR and ESL. However, the use of several electrolytic capacitors demands a large PCB, and increases not only the size, but only the cost of the prototype. Hence, in the scope of this dissertation, two electrolytic capacitors were used in parallel in each submodule, resulting an equivalent capacity of 1.64 mF.

The selected capacitors were electrolytic, so the dynamic response is slow for fast transients, which requires the use of faster capacitors. As such, two extra capacitors were selected. A 10 µF film capacitor and a 100 nF polypropylene capacitor [73]. In Figure 5.2, the three capacitors are presented in order of mention in the text.

Figure 5.2 Capacitors selected for the submodule development, 450 V 820 µF, 500 V 10 µF, 1000 V 100 nF, respectively.

At last, the submodule was equipped with sensors of both voltage and current presented in Figure 5.3. The current sensor present in the submodules intends to keep measure the current in the arm of the converter for the controller Each arm of the MMC is the junction of two submodules in series, so the current that flows through them is the same. As such, only one submodule per arm is equipped with a

current sensor. The sensor selected was LA-100P manufactured by LEM [74]. This is a hall effect sensor rated for a nominal current of 100 A equipped with 2000 turns in the secondary coil, possessing great linearity and accuracy, as well as low temperature drift, high bandwidth, and low delay. The number of turns in the primary depends on the application and on the maximum value of current to be read in order to optimize the scale to the maximum. In the application in use, eight turns were used in the primary. The output of the referred sensor is the current flowing on the secondary, with a maximum value of 50 mA in full scale reading. As such, a measure resistance must be used for the control system to get acquire the value read by the sensor. The resistance used was 120 Ω.

Figure 5.3 Sensors equipped in the submodules: Current sensor and Voltage sensor.

The voltage sensor aims to monitor the voltage across the capacitor in order for the control system to be able to balance the voltage across all the submodules, maintaining an even distribution of power through all submodules during the functioning of the converter. The voltage sensor selected for the application was CYHVS5/25A manufactured by ChenYang Technologies GmBH & Co. KG [75]. In similarity to above, the voltage sensor is a Hall Effect one, and can measure both AC and DC signals, ensuring insulation and a precision of ±0.8% full scale to a voltage value up to 2000 V.

According to the datasheet [75], both the input and the output of the sensor are made in current signals, possessing a transformation relation of the sensor is 1000:5000, with a maximum output current of 25 mA, hence it is necessary to use both resistors in the input and output of the sensor, as the electrical diagram presented in Figure 5.4 suggests.

The values of the resistors R_1 and R_2 define the maximum value of voltage that can be read by the sensor. Using 10 kΩ and 27 kΩ the sensor is able to measure values up to 259 V, enabling a safe margin for the voltage monitoring across the capacitors of the submodules. The resistors R_s is set to 0 Ω to function as a shunt, while the R_m is set to 120 Ω, same as in the current sensor.

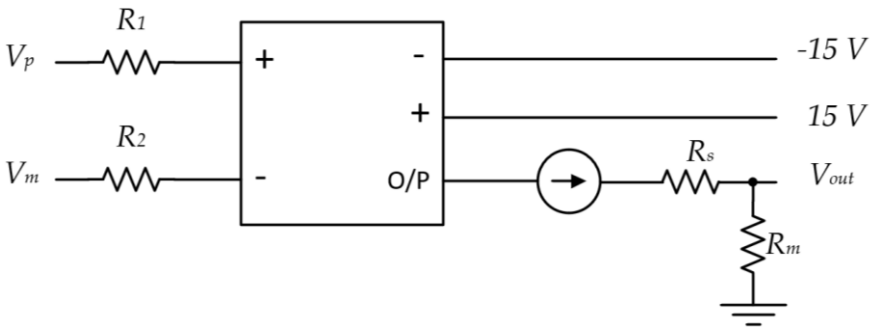


Figure 5.4 CYHV5/25A electric diagram.

Using the mentioned components discussed thus far in this section, it was possible to develop a complete submodule in a half-bridge topology presented in Figure 5.5, containing voltage surge protection, an array of capacitors in the DC-link of each submodule with different dynamic responses, and voltage and current sensors for the control of the submodule as an individual, and its integration in the converter as a whole.

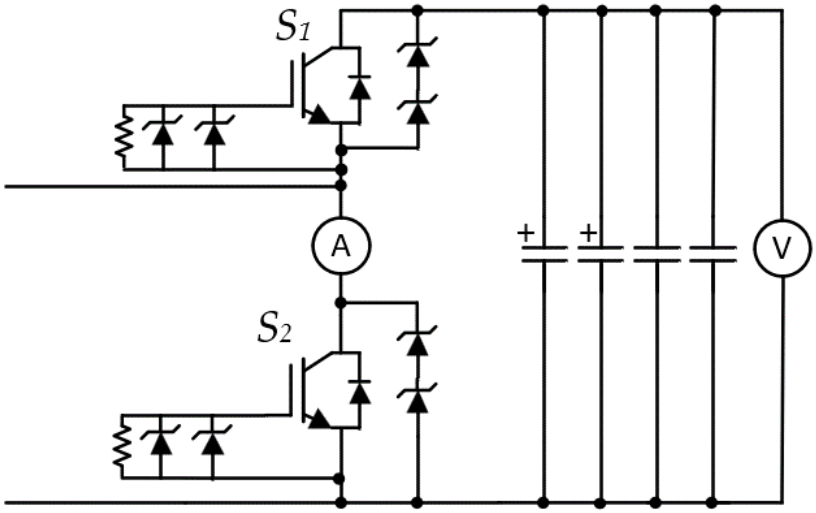


Figure 5.5 Submodule electric schematic.

Recurring to the software Altium Designer, a PCB was developed for each submodule. The board is equipped with the power stage of the submodule, containing all the components discussed earlier in this section. This PCB was developed simultaneously with the driver PCB, which is presented next in this chapter. Two connectors were placed for the connection of the driver board vertically, in order to create a generic submodule that can be tested with different drivers with the gate signals close to the IGBT. Regarding the gate protection, the submodule board counts with the gate-source resistor, as well as a Zener diode and a TVS [76]. The layout of the submodule PCB is presented in Figure 5.6 and in appendixc 2 in detail.

The position of the components was carefully delineated not only to optimize the size of the board, but also to improve the dynamic characteristics of the circuit. The most critical components to place were the

IGBTs, since for a good dynamic response they must be close to the submodule capacitors and for protection purposes they must be close to the TVSs and to the gate protection circuit.

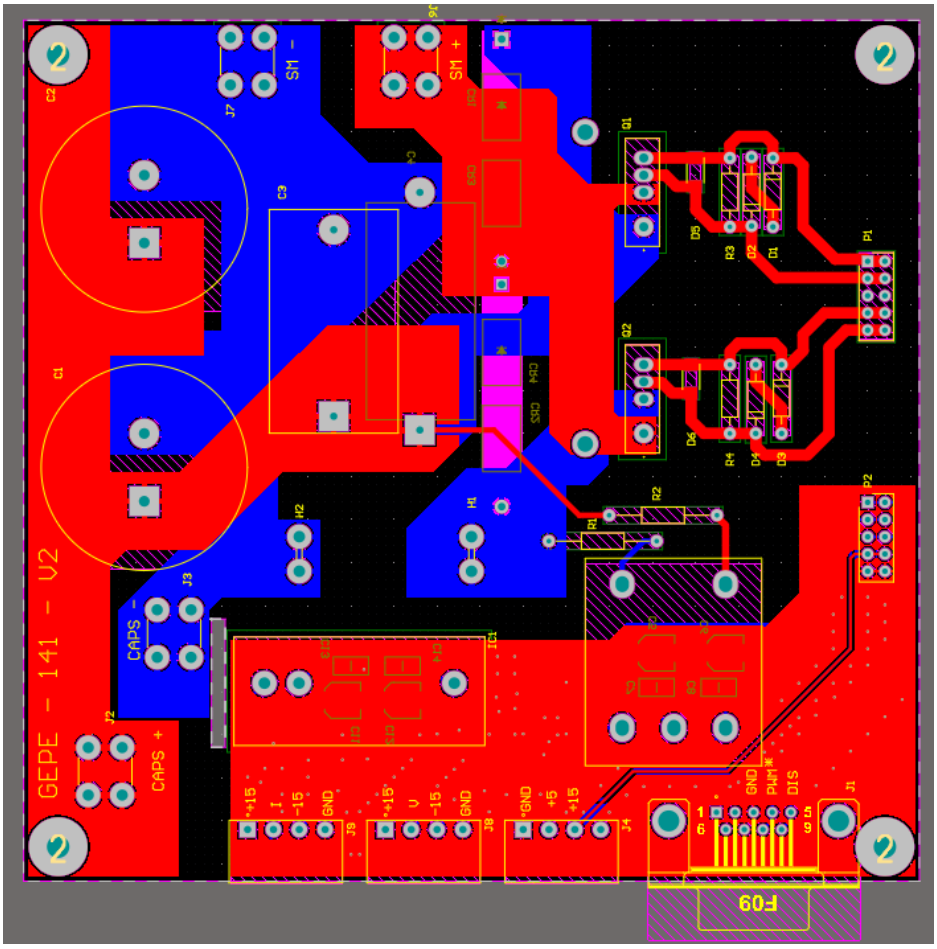


Figure 5.6 Layout of the submodule PCB in Altium Designer.

The IGBTs also require a heatsink on their backs, filling the space in the back of the IGBTs on the top layer. As such, the TVSs and the polypropylene capacitors were placed on the bottom layer of the board to be as close as possible to the IGBTs. On the other hand, the gate protection circuits are placed in the front of the IGBTs, next to the connectors to the driver board. It is important to notice that the all the power connections were made using copper planes to reduce the inductance of the connections, as well as allowing the better flow of the current.

In Figure 5.7, the Submodule board is presented in 3D view provided by the Altium Designer Software, a powerful feature that allows a prediction of the final layout of the board while in the final version with all the components placed in the correct positions, which is presented in Figure 5.8.

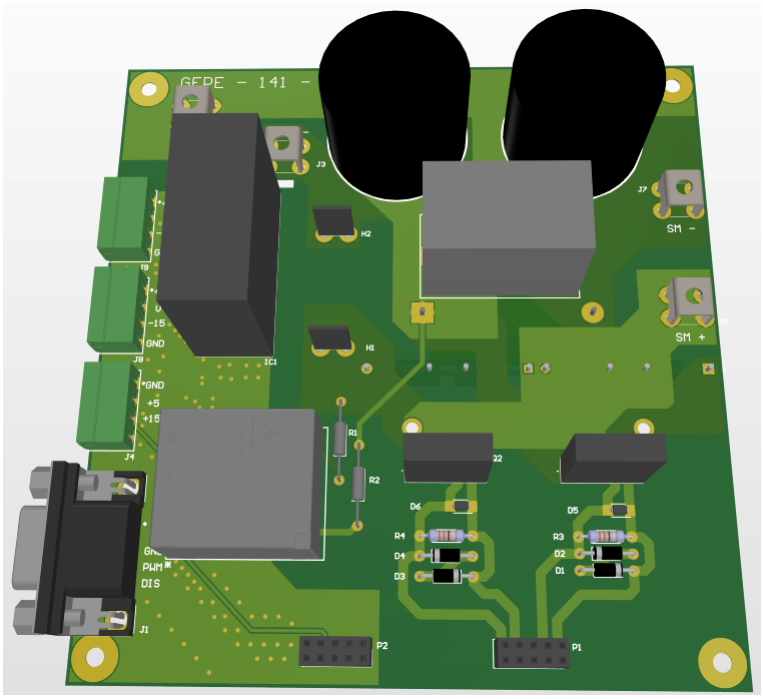


Figure 5.7 3D view in Altium Library of submodule PCB with components.

Figure 5.8 Final view of submodule board.

As foreseen, the resemblances between the 3D model and the final board are remarkable since it count with 3D models of the components used, with exception of the heatsink.

5.2.2 Driver Implementation

In order to command the IGBTs, a driver circuit is required. The driver consists of an integrated circuit with the functionality to output a signal to a capable of charging and discharging the gate capacitor of the IGBT in order for it to switch. After a careful assortment, the driver selected was SI8244-CB manufactured by SkyWorks [77]. This driver possesses very attractive characteristics for the drive of a half-bridge: it counts with a 4 A output, up to 8 MHz operation frequency, and most importantly, with one input signal, two outputs are generated complementary to each other, with a high-precision deadtime programmed by a resistor. Regarding the power of the driver, the input is powered with 5 V, while the output needs two separate DC-DC converters to ensure insulation. The selected converters were MEJ1S1515SC manufactured by Murata Manufacturing [78] presenting an insulation capacitance of 3 pF and isolation resistance of 1 GΩ. This DC-DC converters receives an input of 15 V and outputs insulated 15 V with short circuit protection up to 48 hours.

In Figure 5.9, it is presented a schematic of the electric diagram of driver circuit. Besides the power of the signal part of the driver, the inputs are controlled by the DSP, which is responsible for the PWM input, a 3.3 V peak square wave that is the result of the modulation. As the driver only possesses a PWM input signal, the deadtime is programed by the value of $R_{DT}$with a linear variation. The resistor selected was 75 kΩ that corresponds to a deadtime of 750 ns. As the switching frequency of the IGBTs is 20 kHz, this value corresponds to only 3% of the signal, considering deadtime in both turn On and Off transitions. The remaining components of the primary of the driver correspond to pull-down resistors and decoupling capacitors. At last, the driver possesses a *disable* input at 5 V responsible for turning off the outputs, resulting in no commutations in the power circuit.

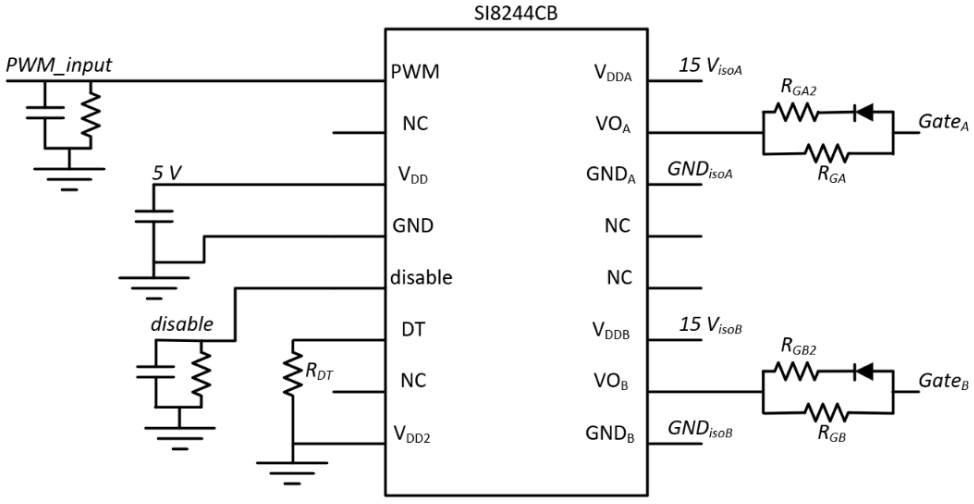


Figure 5.9 Electric schematic of the driver circuit.

Regarding the secondary of the driver, two outputs are generated based on the PWM input, complementary to each other. A DC-DC converter powers each output of the driver ensuring insulation for both signals that will drive each IGBT. Regarding the gate resistor, the value selected was 12 Ω as recommended by the datasheet of the IGBT. It can be noticed that in parallel with the gate resistor there is an inverted diode in series with another resistor. This ensures a smaller equivalent resistor in the turn off time of the IGBT, since it can provide more current for the discharge of the gate capacitor, to ensure a lower turn off time.

In Figure 5.10 and in Appendix 3 in detail, it is presented the layout of the driver PCB developed in Altium Designer. This PCB was designed simultaneously with the submodule PCB in order to combine with one the other.

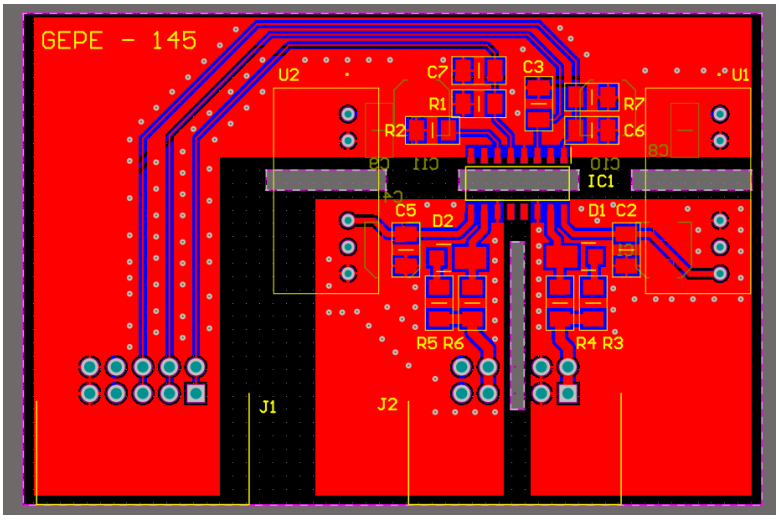


Figure 5.10 Driver PCB layout in Altium Designer.

The input and output connectors were dimensioned to match with the submodule PCB, in order to fit vertically to optimize the horizontal size of the submodule PCB. The insulation between the primary (DSP – control side) and the secondary (IGBT – power side) of the both the driver as well as the DC-DC converters was considered in the design of the PCB, adding rips beneath the components to ensure better insulation properties. To note that the outputs of the driver are separated in different copper planes with a rip in the middle, and the middle pins of the connector were removed also to improve the insulation.

After a prolonged process of verification, the PCB were sent to manufacture, and the results are the presented. In Figure 5.11, it is presented the 3D view in Altium library, a powerful tool that allows a good perspective of the visualization of the final aspect of the PCB, which is presented in Figure 5.12, after all the components were in place. Important to mention that in the bottom layer of the board there are decoupling capacitors in the primary and secondary of both DC-DC converters.

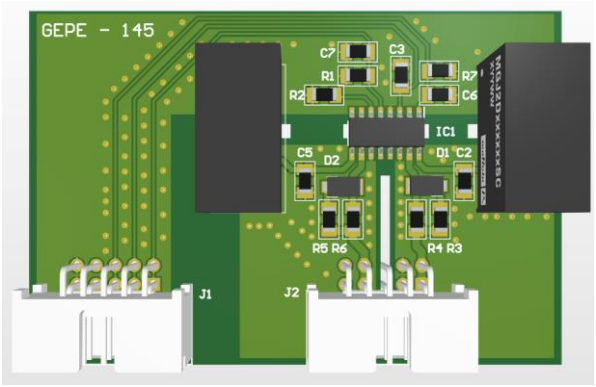


Figure 5.11 3D view in Altium Library of driver PCB with components.

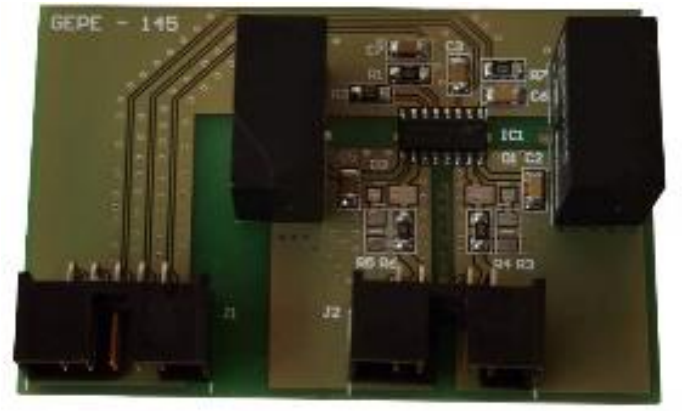


Figure 5.12 Final view of driver board.

Once both the submodule board and driver board were manufactured, soldered, and tested, they were assembled as one, and the result is as demonstrated in Figure 5.13.

Figure 5.13 Integration of the driver and submodule PCBs.

5.3 Control Stage

This section focuses on the implementation of the circuits responsible for the control of the power converter. Such circuits include signal conditioning, protection and a dock platform for the DSP used in this dissertation.

5.3.1 Signal Conditioning

In order to be able to control the power converter, it is necessary to acquire the voltage and current values across distinct locations of the MMC, thus recurring to the use of sensors. The DSP unit must be able to obtain such values to perform the necessary calculations and actuate on the power circuit accordingly. The obtention of these values is made using an analogic to digital converter (ADC), which can read values between 0 and 3.3 V. The output of the sensors, however, does not match this requirement hence being necessary the use of signal conditioning circuits.

In the power converter developed in this dissertation eight sensors were utilized. From these, five measure voltage while the other three measure current. The use of an external ADC was arbitrated, and the selected was AD7616 manufactured by analog devices, a 16 channel, 16 bits ADC [79].

In a first stage, as previously demonstrated in Figure 5.4, it is necessary to include a measure resistor in order to keep the values in the range of the ADC readings. Then, a second order low pass filter was developed in order to reduce the amount of noise in the digital processor, thus resulting in a steadier control. The referred circuits are presented in Figure 5.14.

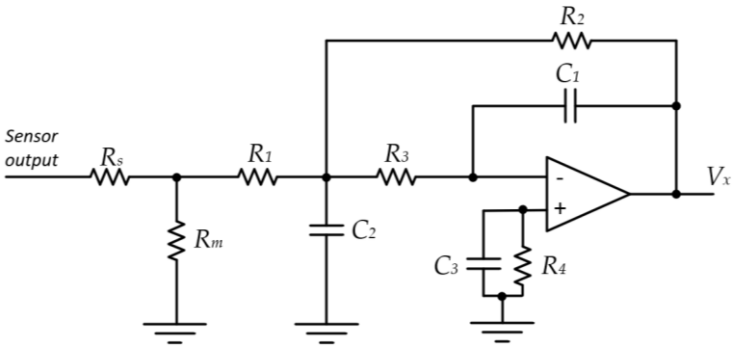


Figure 5.14 Signal conditioning and second order low pass filter schematic.

The dimensioning of the second order filters for each sensor was made recurring to the help of a filter design tool, designed by OKAWA [80]. The cut frequency of the filters was set to 2 kHz to all the signals, thus attenuating the switching noise in 40 dB, while maintaining a phase in the fundamental frequency

of approximately 180°, as intended, thus not creating a delay between the real value, and the value acquired by the ADC in the spectra of interest.

5.3.2 Hardware Protection

Following the second order filter, a window comparator was implemented in order to create a fast response hardware protection of the power converter. This circuit consists of the comparison of the signal read by a sensor after filtering with two reference values, a negative and a positive. Such reference signals are dictated by the resistors presented in the circuit in Figure 5.15, and refer to the possible interval of values that the given signal is allowed to vary. If the value is higher than the maximum positive value, or than the maximum negative value, the output of the comparator is set to a digital high, hence generation an error. This comparator was implemented recurring to the component LM339, manufactured by Texas Instruments [81], an integrated circuit that possesses four comparators with open collector output. As such, each component was used to implement two window comparators for different variables in order to optimize the component functionality to the maximum.

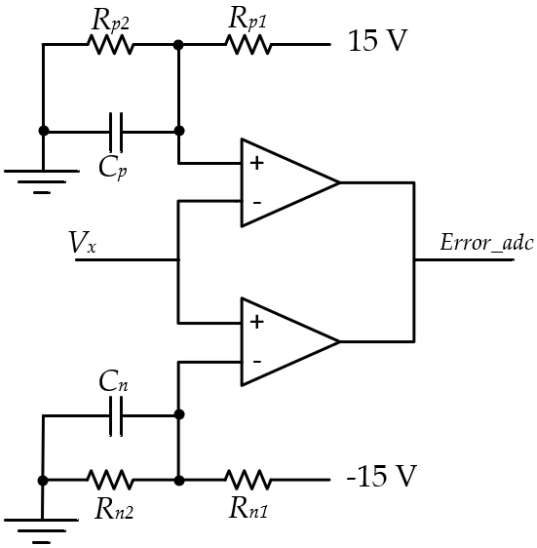


Figure 5.15 Hardware error detection circuit schematic.

In Table 5-2, all the controlled variables are presented, as well as the maximum reference values which they can reach before an error occurs in the hardware protection.

Table 5-2 Maximum values for the controlled variables in the MMC.

Controlled Variable	Nomenclature	Maximum negative value	Maximum positive value
Submodule 1 voltage	V_{SM1}	0 V	258 V
Submodule 2 voltage	V_{SM2}	0 V	258 V
Submodule 3 voltage	V_{SM3}	0 V	258 V
Submodule 4 voltage	V_{SM4}	0 V	258 V
Output voltage	V_{out}	-377 V	377 V
Output current	I_{out}	-13.2 A	13.2 A
Upper arm current	I_{up}	-13.2 A	13.2 A
Lower arm current	I_{down}	-13.2 A	13.2 A

Following the detection of the error, it was implemented a mechanism to memorize it since the comparator output would be set to a digital zero once the controlled variable returned to the established margin of values, which could result in damage on the electronic components of the power circuit. As such, a simple set and reset logic was implemented recurring to NE555, manufactured by Texas Instruments [82], working as bistable. It was also implemented a physical reset button to rearm the operation after removing the source of the error.

To ensure a safe operation in the power converter, the switching of the power semiconductors only occurs if three different enable signals are active. This was made using logic with two AND gates as demonstrated in Figure 5.16. The user inputs the first two signals. The signal *Enable_user* is made by a physical switch implemented in the prototype to prevent damage in the power converter components in case of failure. The signal *Enable_DSP* is sent via software by the DSP and can be used to implement software protections. Important to mention that the AND gates operate with 5 V inputs, and the DSP outputs the signals at 3.3 V TTL CMOS. As such, a boost converter was used to convert the 3.3 V output of the DSP to the 5 V input of the AND gate. Finally, the third enable signal, *Enable_ADC*, is set to digital high when no errors are detected in the ADC.

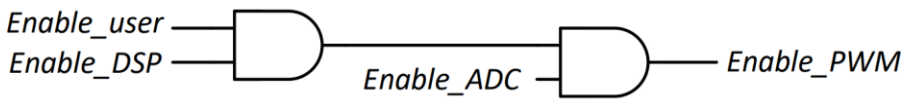


Figure 5.16 Logic to enable switching of the power semiconductors.

The signal conditioning and hardware protection regarding the eight controlled variables were included in a single board presented in Figure 5.17. This board is powered with 15 V and -15 V and possesses internal voltage regulators to 3.3 V and 5 V manufactured by Murata Power Solutions [83]. All the circuits in the are powered recurring to the local voltage regulators.

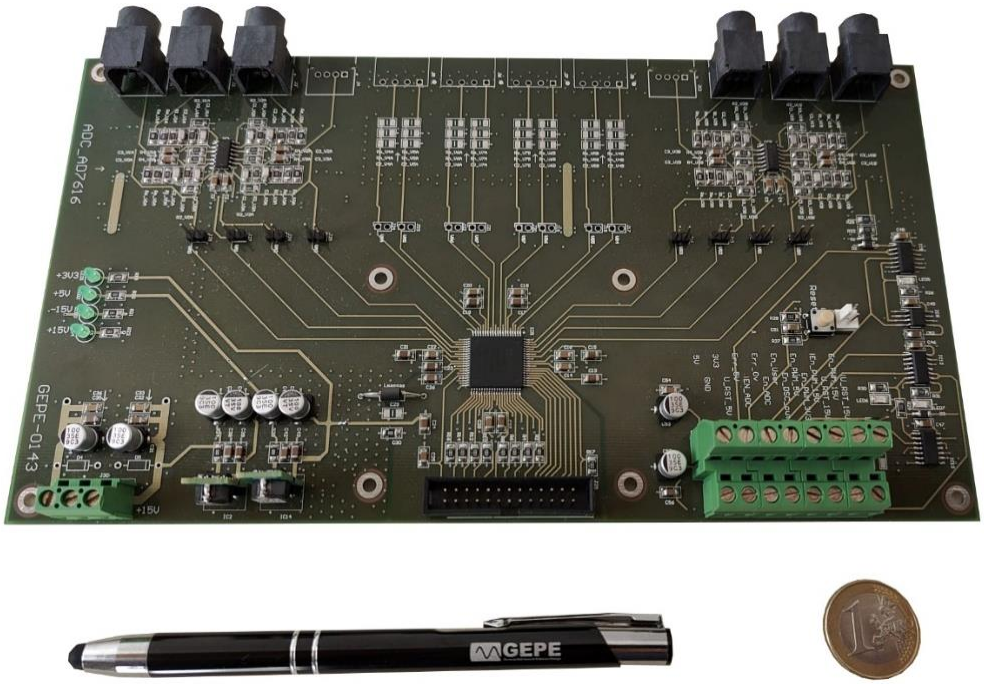


Figure 5.17 External ADC PCB with signal conditioning and hardware protection.

5.3.3 DSP Platform

Nowadays, digital control is necessary in all systems that require data acquisition and calculations. Power electronics is no exception. Digital control creates a friendly user interface with the power converters, with the capability of controlling the outcome of the converters by software. In the scope of this dissertation, for the control of the MMC, the DSP TMS320F28379D manufactured by Texas Instruments [84] was selected due to some attractive characteristics in terms of processing power, as well as the possession power electronics driven functionalities. Such characteristics include a dual-core architecture, 200 MHz clock frequency, up to 169 GPIO pins, 24 high resolution PWM channels with internal complementary generated with programable deadtime, and many others.

After an extensive study of the peripherals available on the DSP and a careful analysis of the necessary signals to control the power converter implemented, a dock station was developed with the organization in the layout of the desired pins optimized in terms of positioning and order of importance. The layout of the PCB is presented in Figure 5.18 and in Appendix 4. The first priority was the connection to the external ADC board. Such connection required GPIO pins. The second priority was the PWM signals. Even though only 4 PWM channels were necessary for to the drive of the IGBTs in the MMC, 6 PWM channels and corresponding complementary signals were displayed in the dock station in order to be used for other applications in the future. This station also counts with SPI connections for the interface with an external DAC, GPIOs dedicated for the connections of contactors and connectors to the internal ADCs and DACs

of the DSP. Similarly to the previous PCBs, it was developed in Altium Designer. This implementation required a careful mapping of the GPIO ports of the DSP.

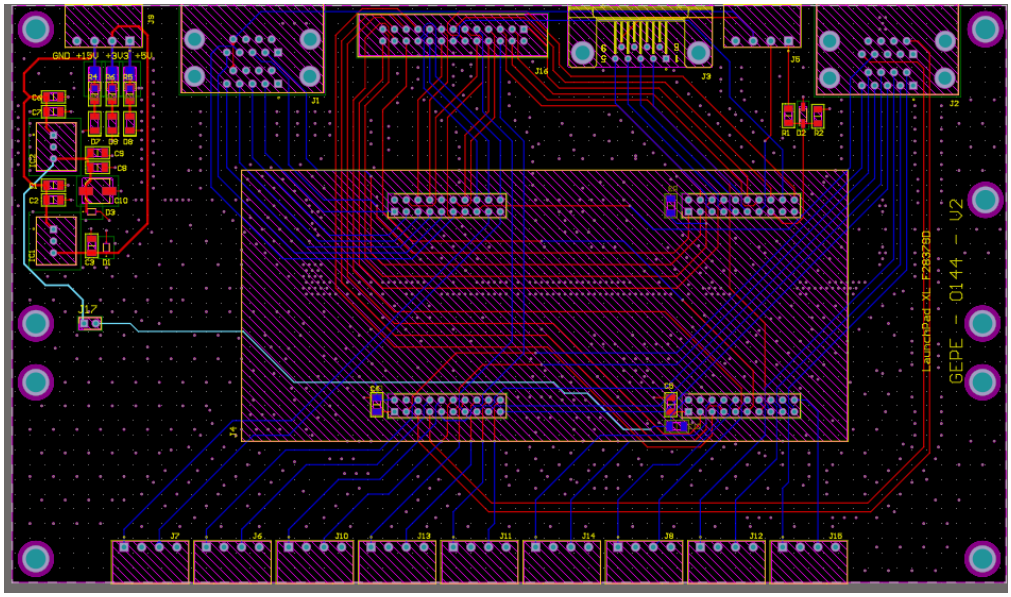


Figure 5.18 Layout of the DSP dock station in Altium Designer.

As the DSP is the center of the communication and control of the system, it is of paramount importance to ensure the quality of its signals. As such, the PCB was designed with four layers. Counting from bottom to top, the first layer corresponds to a copper plane connected to GND with several connections. The second layer contains the connection of the power signals provided by the voltage regulators. In the third layer it is made a reinforcement of the GND plane while the fourth layer (top layer) contains only tracks to make the necessary connections. It is also important to notice the existence of many vias to reinforce the GND copper planes along the entire board. In Figure 5.19, it is presented a 3D view of the PCB.

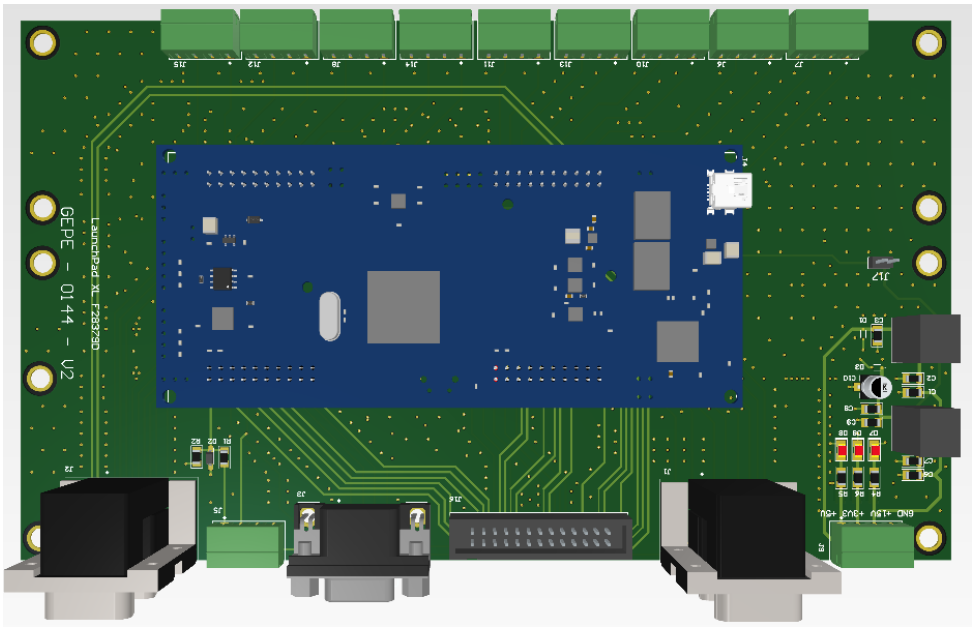


Figure 5.19 3D view of the DSP TMS320F28379D dock station PCB.

After manufacturing and a selection of the necessary components, the PCB was assembled and the result is as follows in Figure 5.20.

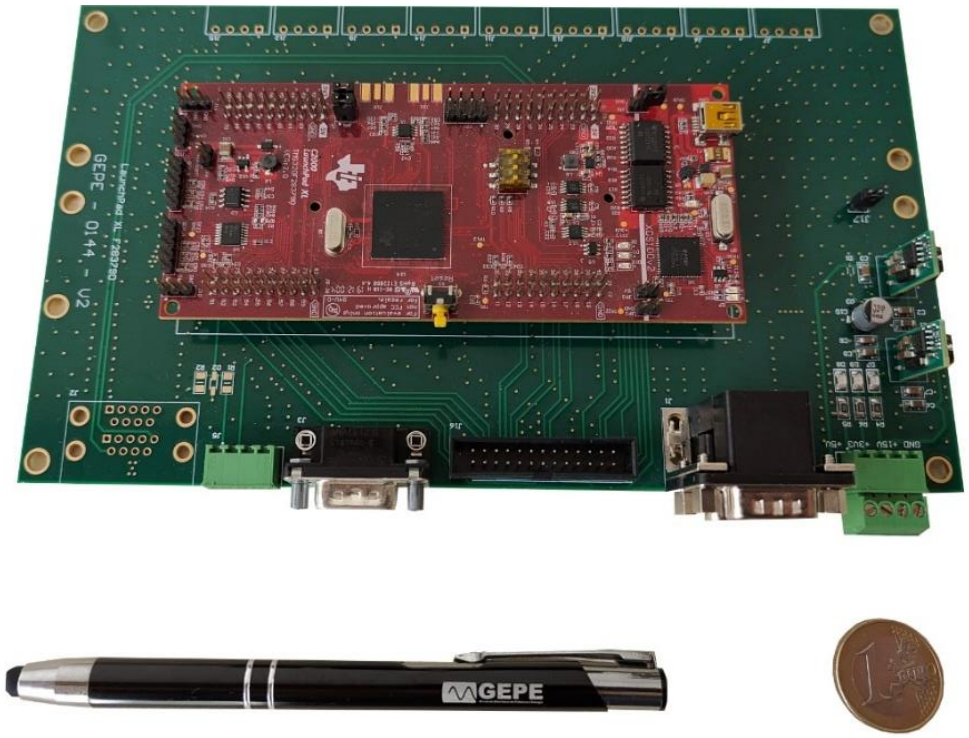


Figure 5.20 PCB of DSP TMS320F28379D dock station.

5.3.4 Software Implementation

Using the TMS320F28379D as software platform for the implementation of the digital control system of the power converter, the main steps were the acquisition of sensor data as inputs, perform calculations with the values obtained and generate PWM signals as output.

Regarding the data acquisition of the data from the sensors, as mentioned earlier, an external ADC was used. The acquisition of the ADC values on DSP is made via parallel communication. The DSP sends a conversion start signal, and the ADC responds with a busy signal, which triggers an extern interruption where the data signals are processed. This is made every 20 µs ensuring a 50 kHz sampling frequency.

The ADC sends 16 data signals each time the writing is allowed. These data signals are received as inputs in the DSP and were mapped together in groups of four in each register of the DSP, since it was not possible to physically access 16 ports in a row in a single register, which would facilitate the acquisition logic. In order to process the first step is to read the value of the four entire registers. Then it is applied a logic AND to save the data from the desired ports. Finally, it is made a shift in the values in order to organize the 16 data bits in from the higher to the lower. Once the bits are organized, a simple sum of

the values is made, and the final value is stored in an array. This corresponds to a 16-bit signal with the value of the controlled variable read, wither for voltage or for current.

In Figure 5.21, it is presented the workspace in the software Code Composer Studio 10.1.1 by Texas Instruments.

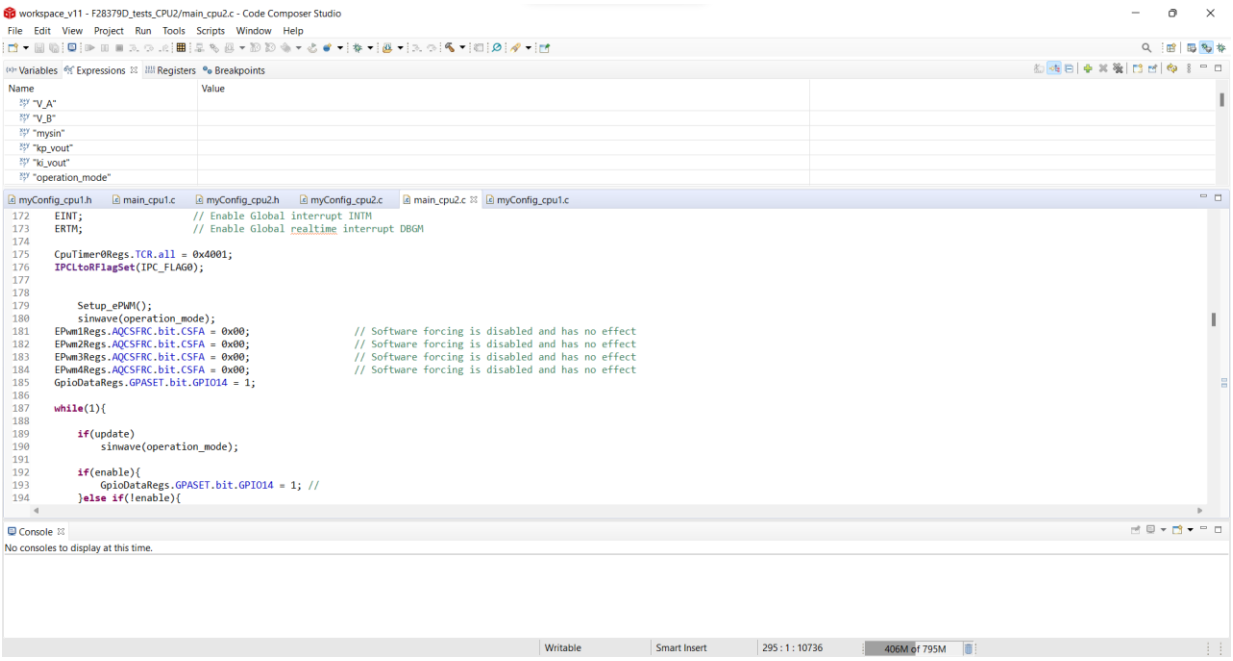


Figure 5.21 Code Composer Studio workspace.

In order to optimize the use of the DSP at its fullest, the two CPUs were utilized, having one dedicated only to data acquisition, while the second is responsible for the calculations and output the command signals. The array with the sensors acquisition is stored in CPU1 and passed to CPU2 through shared memory registers.

Regarding the implementation of the calculations, every 20 µs a function was called where the control equations were implemented. Important to mention that when before implementing the PLL to power grid interface, the reference sinusoidal signal was generated via software, where the number of points necessary is dictated by the sampling frequency ($f_{sampling}$) and the fundamental frequency of the reference signal (f_{sine}), as proposed in equation (5.1).

$$n = \frac{f_{sampling}}{f_{sine}} \tag{5.1}$$

Regarding the PWM generation, as mentioned in section 3.3, it is made by the comparison of a modulator and a carrier signal. The modulator wave corresponds to the output of the calculations. The carriers, on the other hand, are configured internally in the PWM channels of the DSP. As such 4 PWM channels were

initialized, with configuration of the carrier signals to a 20 kHz frequency, the selected switching frequency for the power semiconductors. The modulation technique selected was phase shift carrier, hence resulting in a programming of the phase angles of the carrier accordingly. Regarding the upper arm of the converter, the angles for the carriers were 0° and 180°, while in the lower arm, the carrier angles were 90° and 270°.

Regarding protection via software to the power converter, some verifications were made using the acquired sensor values, thus creating redundancy in the protection of the MMC, in combination with the already implemented hardware protection. Furthermore, the modulation index was set between 10% and 90%.

The main loop of the software implementation is presented in Appendix A.

5.4 System Integration

In the scope the dissertation, four submodules and four driver PCBs were developed, soldered, and tested individually, for a later integration in the power system. In the selected topology, such integration also requires some passive elements: capacitors in the DC-link and coupling coils that also operate as inductive filters. The components used are presented in Figure 5.22.

(a) (b)

Figure 5.22 Passive elements in the power circuit: (a) decoupling capacitors; (b) coupling coils.

Since the power in the output of the converter is pulsated due to the PWM switching, the capacitors are necessary to stabilize a voltage ripple in the DC-link. The selected capacitors for the application were 450 V, 2200 µF B43564-A5228 manufactured by EPCOS [85]. Regarding the coupling coils, the selected

was an iron core inductor with 6.8 mH at 50 Hz. This coil is commonly used in the GEPE laboratory for power electronics prototypes.

The power stage of the final prototype includes four submodules and respective drivers, 2 DC-link capacitors in parallel with the input power supplies, two pre-charge resistors with bypass switch, a circuit breaker and connectors for the loads or a transformer. It is important to mention that a physical protection mechanism, human activated was implemented in order to shut down the power supplies and the transformer recurring to an interlock stop button. Once this button is pressed, for the power supplies to be turned back on, first it is necessary to unlock the stop button, and then press the start button. Furthermore, whenever the power supplies are connected, a red light is turned on and remains on until the power is disconnected.

Regarding the connection of the submodules to each other, the power signals to the primary of the drivers are shared among the four submodules to avoid the creation of ground loops since they all share the same potential without closing the loop. This was a critical part of the design of the system as a whole, since the unification of the system developed required many connections between all the boards, with a common potential being shared in all, the ground. In order to minimize the ground loops, the ground signal was distributed from the DSP dock station board to the others.

The control stage of the final prototype includes the DSP dock station board, connected through flat cable to the external ADC board. The supply of the control stage is ensured by an AC-DC converter manufactured by Traco Power [86], which possesses the necessary outputs that the control system requires: 15 V, -15 V and 5 V. In order to facilitate the hardware debug and the visualization of the control signals, a DAC board utility developed in the GEPE laboratory was used. At last, as mentioned earlier, an entrance panel was used for physical interface with the system containing two buttons, an error reset for to clear the errors detected by the window comparators and a physical enable for the power commutations.

The prototype is equipped with gutters all around to facilitate the connections, as well as providing an aesthetically improvement of the final visualization. The layout of the prototype consisted of a visible separation of the control and power stages to minimize the EMI caption of electromagnetic noise prevenient from the power circuit to the control circuit, as well as allowing a better debug in terms of hardware and troubleshooting. As such, apart from the visible in the final prototype presented in Figure 5.23, all the connections made with cables through the gutters were planned in order not to cross power cables with signal cables, to reduce the electromagnetic interferences. Furthermore, the cables from the

same circuits were twisted in pairs to reduce electromagnetic radiation from one another, as well as mitigating the crosstalk with other cables.

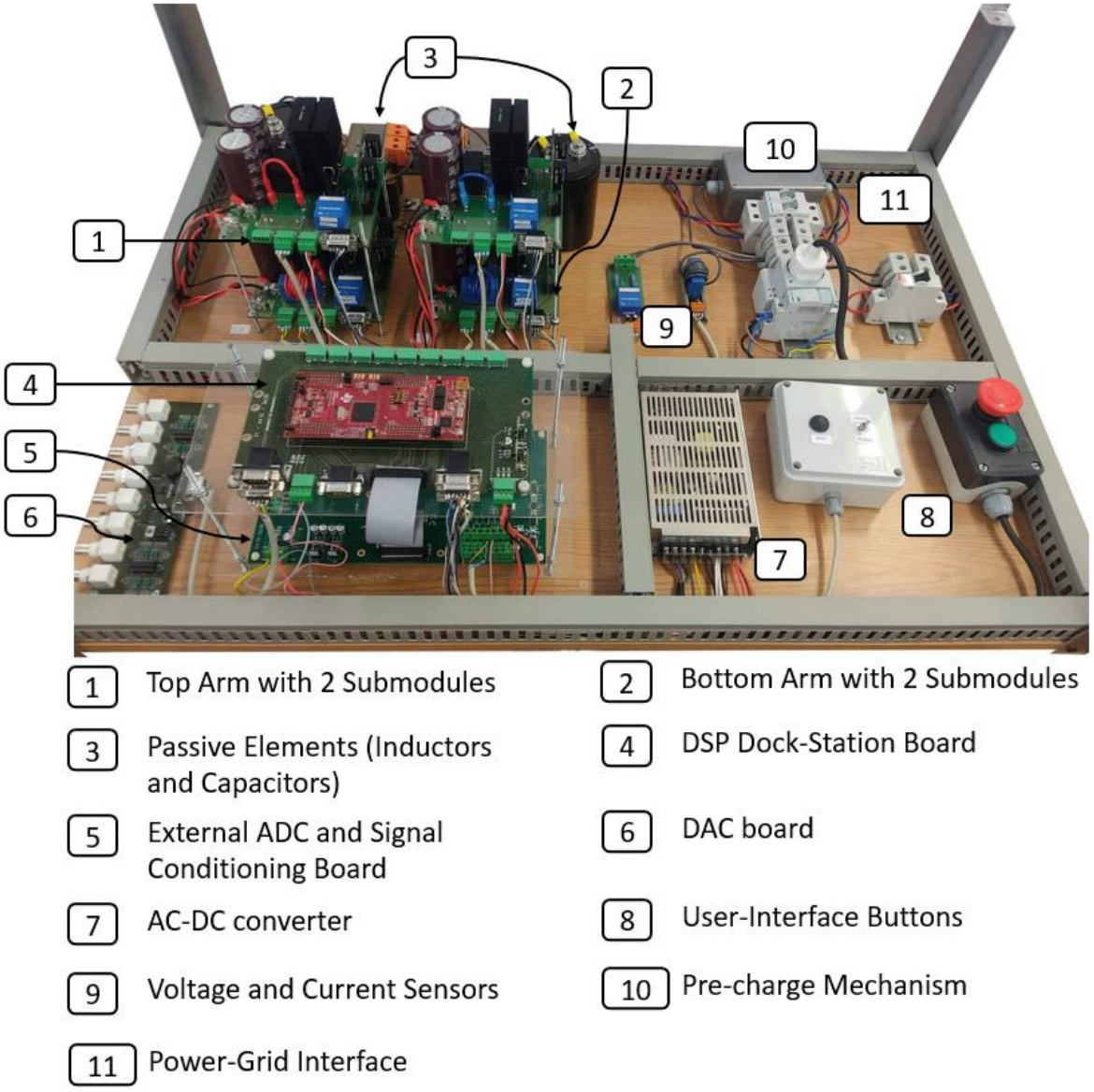


Figure 5.23 Final prototype of the developed MMC.

5.5 Conclusion

This chapter regards the implementation of an experimental prototype to validate the functioning of the chosen topology. For a better understanding of the system as a whole, three distinct separations were created in the organization of the chapter: the power stage and the control stage, and the software implementation, culminating in the integration to a final prototype.

Regarding the power stage, two main circuits were discussed, where a board was developed for each individually, however materializing in one. For each board, the used components were displayed, with a justification of the purpose fulfilled in the circuit. The submodule board contains 2 IGBTs with corresponding gate protection circuits, four capacitors with different capacity values and consequent dynamic response, two pairs of two series TVSs in antiparallel with the IGBTs for surge voltage protection and voltage and current sensors. The driver board contains a driver integrated circuit capable of driving a half-bridge converter with a single input PWM, creating a complementary internally with programmable deadtime, two isolated DC-DC converters to power outputs of the driver and gate resistors.

The control stage was subdivided in two different board, one containing data acquisition, signal conditioning and hardware protection, while the other serves as a dock station for the DSP. The data acquisition is made with a 16-bit external ADC, data that passes through signal conditioning in order for the values to be in reading range. Regarding the hardware protection, the values acquired go through a windows comparator that compare these with boundaries defined for all the controlled variables for an error generation. Upon the occurrence of an error, it is memorized in order for the switching of semiconductors to be returned only upon a physical reset button.

Following up the hardware implementation, the software implementation was discussed. It was necessary to develop software for the digital processing of the data acquired by the sensors and control the power converter. The implementation of the software was made in two different CPUs of the same DSP. The first CPU was dedicated to the data acquisition while the second CPU kept responsibility of the calculations and output of the PWM signals. The generation of the PWM signals is also discussed in this chapter.

The full prototype is displayed in the end of this chapter, where the main concern was to minimize noise in the system. To do so, a clear separation was created between the control and the power stages, for less electromagnetic compliance, was well as the effort to reduce the ground loops.

Chapter 6

MMC Experimental Validation

6.1 Introduction

Along this chapter, the experimental results thar allow the validation of the proposed topology, a MMC with two submodules in each arm in a half bridge topology are presented. At first, the individual tests are approached building up to the validation of the entire system, regarding the power converter itself, as well as the auxiliary circuits associated. Results are presented for different control techniques to better understand the functioning of the power converter.

It is important to refer that in order to ensure the safe operation of the MMC, the voltage and current values in the experimental tests were gradually incremented as the control techniques were validated, raising the voltage to a maximum value of 240 V in the split DC-link, with an output voltage of 50 V RMS in electrical power grid interface, recurring to a step-down transformer.

6.2 Individual Submodules

The MMC developed in the scope of this dissertation is composed by 4 Half-Bridge submodules. As such, before the integration of the entire system, it is necessary to validate each submodule individually. In order to do so, a test platform was developed consisting of an RC parallel circuit with a series inductance, as presented in Figure 6.1.

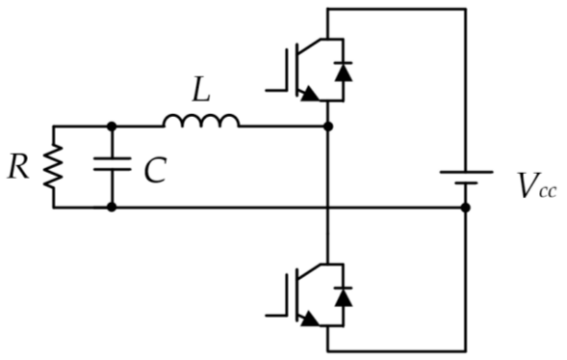
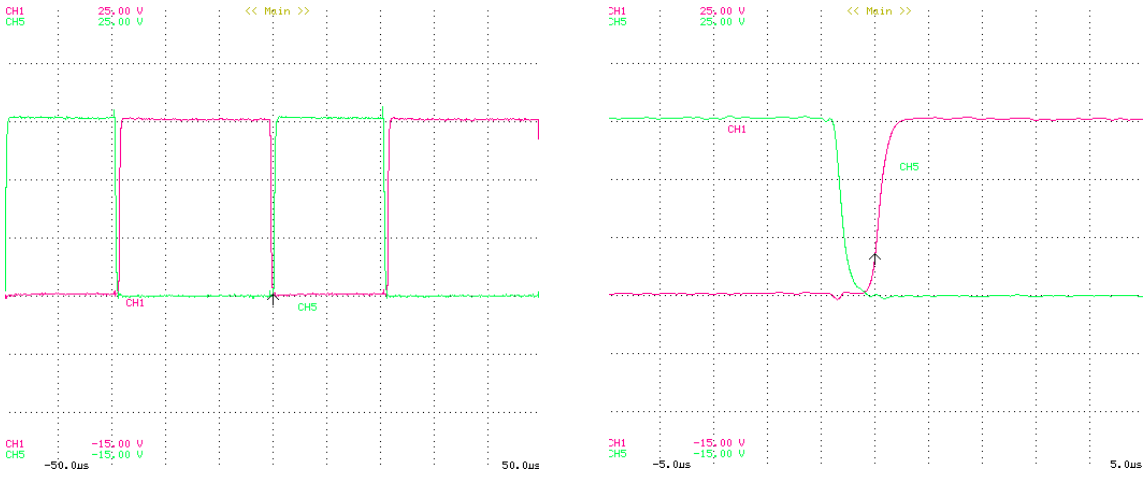


Figure 6.1 Circuit implemented for the test of each submodule.

Before powering the power circuit, the first step consisted of the verification of the driver output complementary PWM signals, as well as the deadtime between each signal as presented in Figure 6.2.

This verification was made with the driver already connected to the IGBTs in order to access its response on the circuit.

Analyzing the PWM signals on the gate of the IGBTs of a submodule it is possible to verify that the signals are indeed complementary, as can be seen in Figure 6.2(a), with a 10 µs/div. scale, where it is presented the PWM signals generation at a 20 kHz frequency. This scale, however, does not enable the visualization of the deadtime, so the signal was zoomed in ten times, as presented in Figure 6.2(b), with a 1 µs/div. scale. It is possible to verify that the deadtime is approximately 750 ns, as programmed by the deadtime resistor on the driver circuit. It is also important to note that the charge and discharge of the gate capacitors are clearly visible, and the signals do not intersect each other, resulting in a safe functioning of each submodule.



(a) (b)

Figure 6.2 Voltage signals on the gate of the IGBTs in each submodule: (a)Complementary PWM signals (10 µs/div.). (b) Deadtime visualization (1 µs/div.).

The individual submodule tests were performed with the component values presented in Table 6-1, a 30 Ω resistor in parallel with a 10 µF capacitor, with a series inductance of 6.8 mH, powered by a power supply of 30 V.

Table 6-1 Individual submodule test parameters.

R	30 Ω
C	10 µF
L	6.8 mH
V_{cc}	30 V

The tests were performed with open loop control for the validation of the power circuits with a 15 V peak to peak, 50 Hz frequency output reference.

In Figure 6.3, the experimental results for a single submodule are presented, with the resistive load voltage signal represented in black with a 5 V/div. scale, where it is possible to observe that the peak-to-peak voltage follows the 15 V reference, presenting an offset since the submodule is an half-bridge converter with a single DC-link, thus not creating negative output voltage values. The current is represented in red and possesses the same waveshape as the voltage since it is measured in the resistive load. The current was measured using a current probe with an output of 100 mV/A.

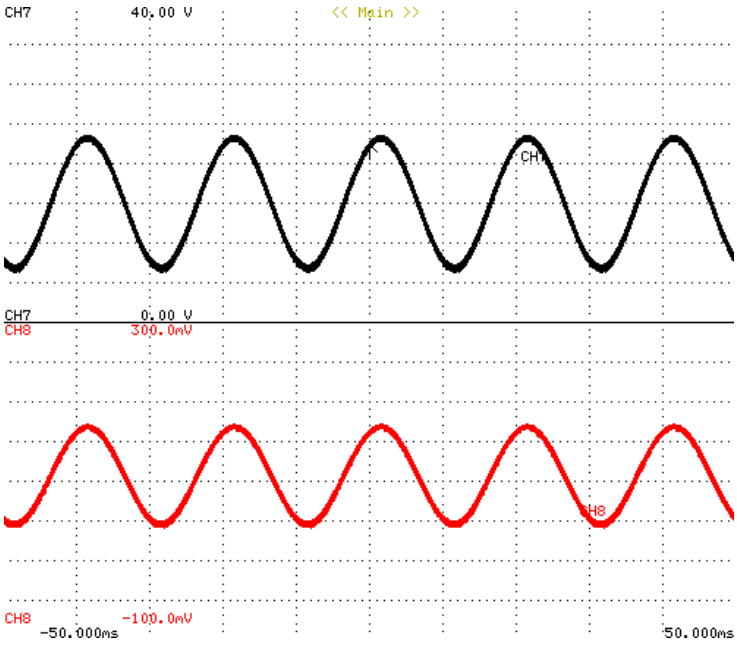


Figure 6.3 Experimental results for a single submodule operation: Resistive load voltage and current (10 ms/div.).

The process presented in this section was followed for all the submodules to validate their functioning as an individual, in order to be able to integrate them into the MMC.

6.3 Open Loop Control of the MMC

With the integration of the entire system, it is necessary to evaluate its behavior as a whole. Due to the complexity of the system itself, open loop control is a simple, yet powerful tool that allows the validation of the power circuit of the MMC, as well as the modulation technique. It is important to refer that in the first tests of the MMC, each submodule was equipped with a power supply to manage the balancing of voltages across all the submodules, since the closed loop control was not yet implemented. Hence, using 30 V in each power supply and an output voltage reference of 25 V peak, the results are as presented in Figure 6.4 and Figure 6.5.

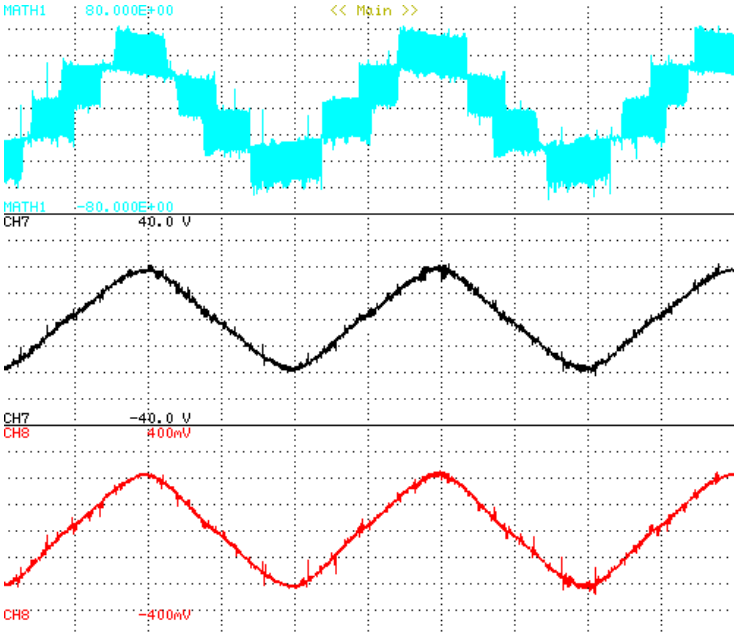


Figure 6.4 Experimental results for MMC operation in open loop with a 10 Ω load resistor: Output voltage levels, output voltage, load current (5 ms/div.).

In Figure 6.4, are laid out the experimental results for the operation of the MMC with a 10 Ω resistor as a load where 3 distinct signals are presented: The output voltage levels measured between the inductive filters in blue, where 5 different levels are displayed; The output voltage of the converter in black with a 10 V/div. scale and the load current in red with a 1A/div. scale.

Although validating both the functioning of the power converter and the phase shift carrier modulation, it is possible to visualize that there is a small discrepancy between the positive and the negative levels in the voltage and the current and the waveshape is only an approximation of a sinusoidal wave. This effect can occur due to differences in the hardware of the MMC, namely between the upper arm and lower arm submodules. However, this can be mitigated by the control system. Furthermore, it is important to demark that the peak voltage value on the output of the converter does not match the reference, since the open loop control does not compensate the voltage drops across the IGBTs in conduction.

In Figure 6.5, the same experimental results are laid out, with the use of a higher load, a 6.5 Ω resistor. The difference between the positive side and the negative one in the current are more notorious as the peak value is increased to a peak value of nearly 3 A. It is very important the observe that in both results presented, both the voltage and the current do not possess offset, which compensation would result in higher complexity in the control algorithm.

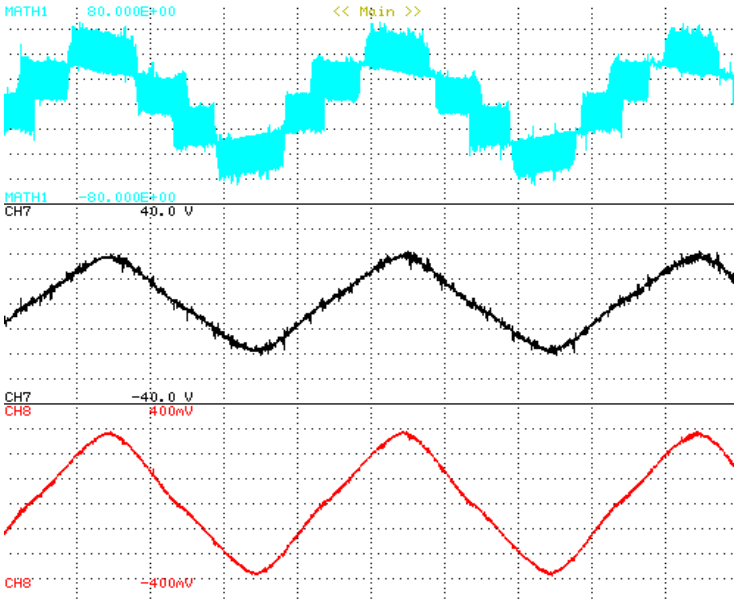


Figure 6.5 Experimental results for MMC operation in open loop with a 6.5 Ω load resistor: Output voltage levels, output voltage, load current (5 ms/div.).

6.4 Close Loop Voltage Control of the MMC

Having successfully validated the operation of the power stage of the MMC and the phase shift carrier modulation, the close loop control of the output voltage of the MMC was implemented recurring to a PI controller. Along this section are presented the results of the behavior of the MMC using voltage control on the output. For comparative purposes, the results presented in Figure 6.6, and Figure 6.7, were acquired using the exact same conditions as those presented in the previous section with open loop control, lowering the peak reference voltage for 20 V to comply with the modulation index, due to the additional voltage drops on the semiconductors.

Just as presented in Figure 6.4, and Figure 6.5, Figure 6.6, and Figure 6.7 present output voltage levels, the output voltage and the load current of the MMC operation. It is clear that closing the loop, the waveform of the output voltage of the MMC acquired a sinusoidal waveform, thus following the reference provided by the DSP. The same happened for the current signal, as the load is resistive.

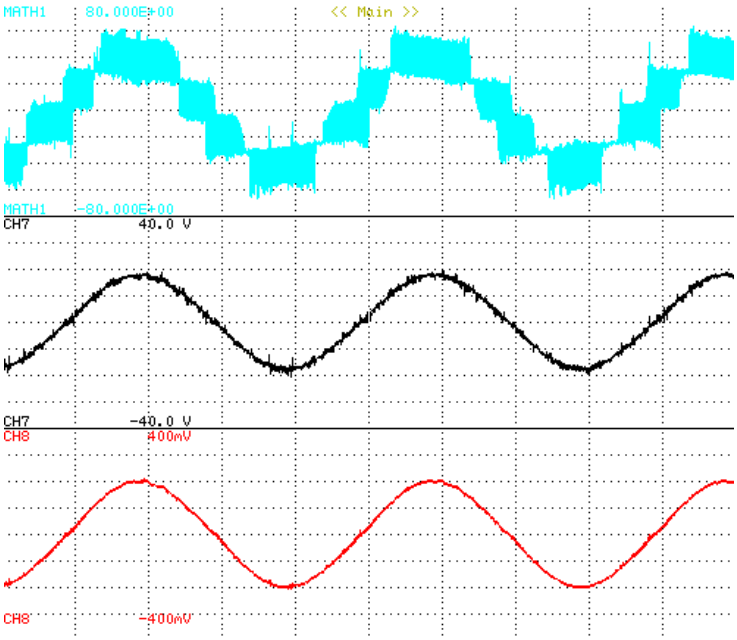


Figure 6.6 Experimental results for MMC operation in close loop voltage control with a 10 Ω load resistor: Output voltage levels, output voltage, load current (5 ms/div.).

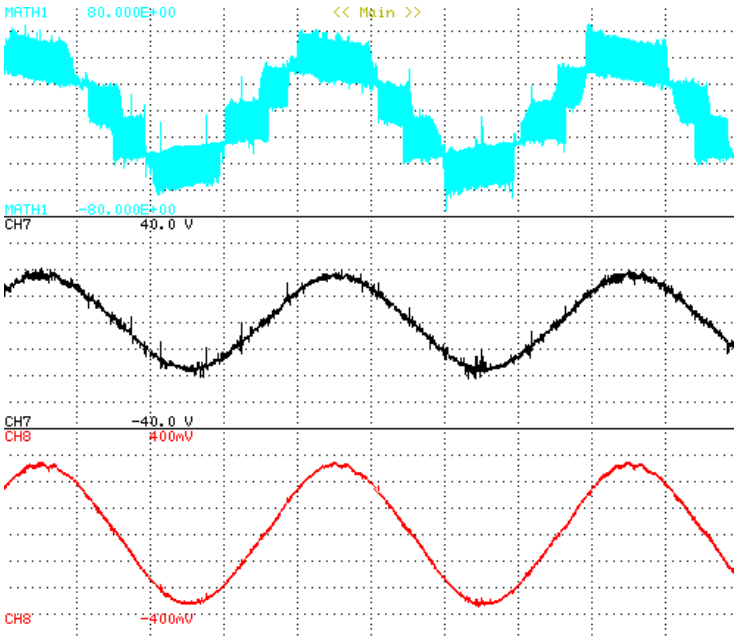


Figure 6.7 Experimental results for MMC operation in close loop voltage control with a 6.5 Ω load resistor: Output voltage levels, output voltage, load current (5 ms/div.).

To fully validate the close loop voltage control of the MMC, the dynamic behavior of the converter was assessed by changing the load value to double the value, from 13 Ω to 6.5 Ω while operating. As the voltage is the variable in control, the waveform and the peak value must remain the same disregarding the load variations. In Figure 6.8, the experimental results for the MMC operating in close loop control with a load variation from 13 Ω to 6.5 Ω are presented.

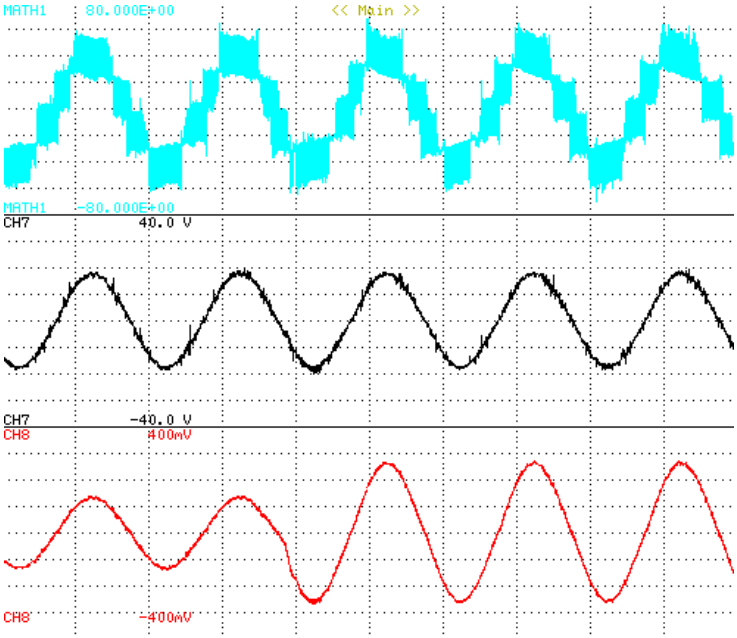


Figure 6.8 Experimental results for MMC operation in close loop voltage control with a load variation from 13 Ω to 6.5 Ω load resistor: output voltage levels, output voltage, load current (10 ms/div.).

Just as the previous results, the results include the output voltage levels measured between the inductive filters in blue, the output voltage of the converter in black with a 10 V/div. scale and the load current in red with a 1 A/div. scale. As expected, the voltage waveform does not suffer any alteration while the current doubles its value, thus fully validating the voltage loop voltage control of the MMC.

6.5 Submodule Voltage Balancing

Regarding the chosen topology of MMC, most control complexity lies on the voltage balancing across the submodules. However, such control is crucial for an equal power distribution across the submodules, one of the main advantages of the MMC, as well as improving the quality of the output waveform with low distortion. The DC-link of each submodule is composed by capacitors that constantly switch state from charging to discharging. When the capacitors charge, energy is being stored in the submodule, which is later delivered to power the submodule output when discharging. This results in ripple on the submodule voltages. The ripple is increased for higher power at stake and can be mitigated by higher capacity values.

The results presented in this section were obtained with a split DC-link voltage of 140 V, 70 V in each power supply with a variation on the resistive load for a clear visualization of the system behavior, particularly the voltage across all the submodules and the effect caused on the voltage and current. The control used for the MMC output was a PI controller on the output voltage, same as the previous results. The reference signal provided to the MMC was a 50 V peak, 50 Hz signal.

The experimental results for the operation of the MMC with close loop voltage control and submodule voltage balancing in a transitory event are presented in Figure 6.9. The results include the voltage levels measured between the inductive filters in blue, the output voltage of the converter in black with a 20 V/div. scale, the load current in red with a 2 A/div. scale, and the voltage of the four submodules with a 20 V/div. scale.

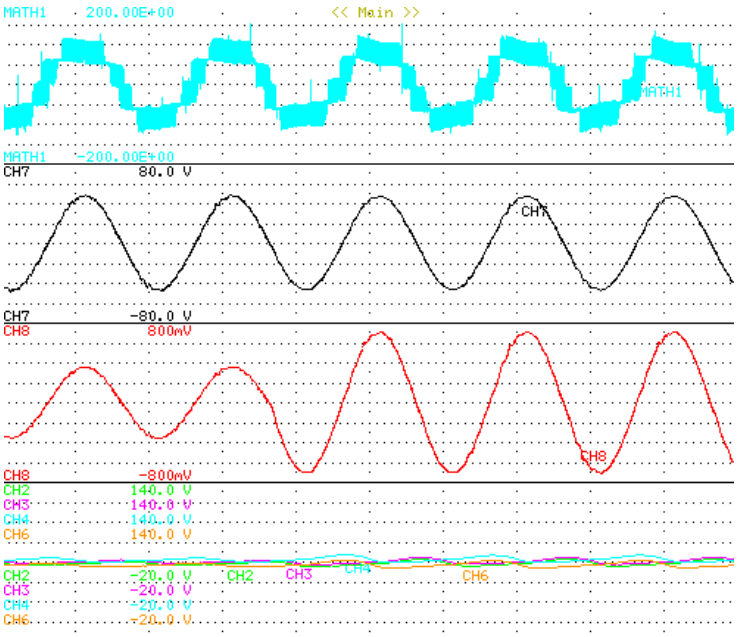


Figure 6.9 Experimental results for MMC operation in close loop voltage control and submodule voltage balancing with a load variation from 13 Ω to 6.5 Ω load resistor: output voltage levels, output voltage, load current, submodule voltages (10 ms/div.).

From the output of the converter perspective, the output voltage follows the reference at all times, including in the current transitory for double the previous value in the load change, as intended. Regarding the balancing of the submodules, it is possible to observe that the medium value of the voltage across the 4 submodules is approximately 60 V. Theoretically, the voltage across each submodule should be the same as the voltage in each DC-link power supply, 70 V in this case, but due the power losses across the MMC, the medium voltage across each arm tended to 120 V in all the tests, thus using 60 V as reference for all the submodules.

The results presented in Figure 6.10, were obtained in the exact same conditions as in Figure 6.9, only changing the submodule voltage scale on the oscilloscope to 2 V/div. and the coupling to DC, thus disregarding the medium value, in order to take a closer look on the detail of the ripple voltage across the submodules. As foreseen, the ripple increases with the power at stake in the MMC. Using approximations in the following values, for a 90 W output, the ripple is about 3.2 V, while for 180 W, the ripple is roughly 6.2 V, disregarding the first transitory.

The results obtained allowed the validation of the submodule voltage balancing control, enabling the possibility to power the MMC using only power supplies in the DC-link of the converter.

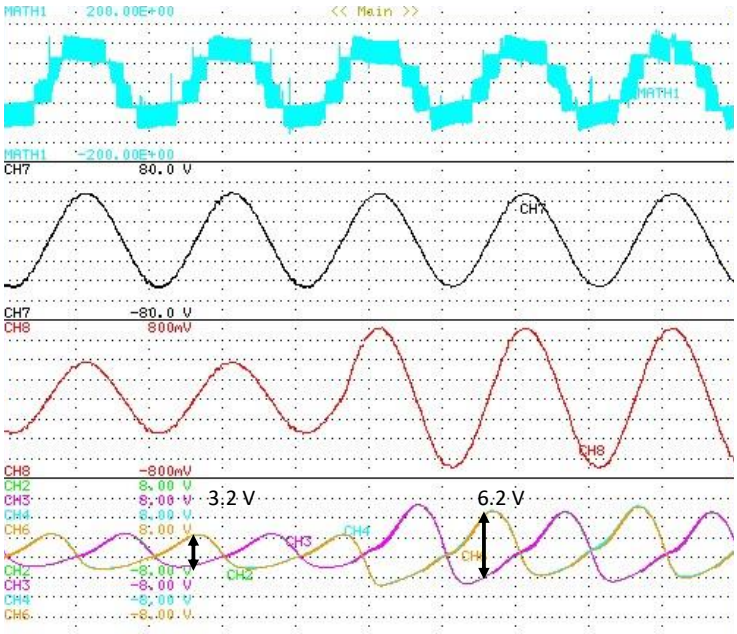


Figure 6.10 Experimental results for MMC operation in close loop voltage control and submodule voltage balancing with a load variation from 13 Ω to 6.5 Ω load resistor: output voltage levels, output voltage, load current, submodule voltage ripple (10 ms/div.).

6.6 Closed-Loop Current Control of the MMC

As the main focus of this dissertation is to implement a MMC to interface with the electrical power grid, it was necessary to validate the current control of the MMC. The control was implemented similarly to the voltage control, using a PI controller with the controllable variable being the current. This step is crucial for the validation of the current control before connecting to the electrical power grid.

The presented results in Figure 6.11, were obtained using a 6.5 Ω resistor as load, 140 V in the split DC-link and a reference signal of 5 A RMS, 50 Hz. The experimental results of the MMC operation in close loop current control with submodule voltage balancing are presented, including the voltage levels measured between the inductive filters in blue, the output voltage of the converter in black with a 20 V/div. scale, the load current in red with a 2 A/div. scale, and the voltage of the four submodules with a 20 V/div. scale.

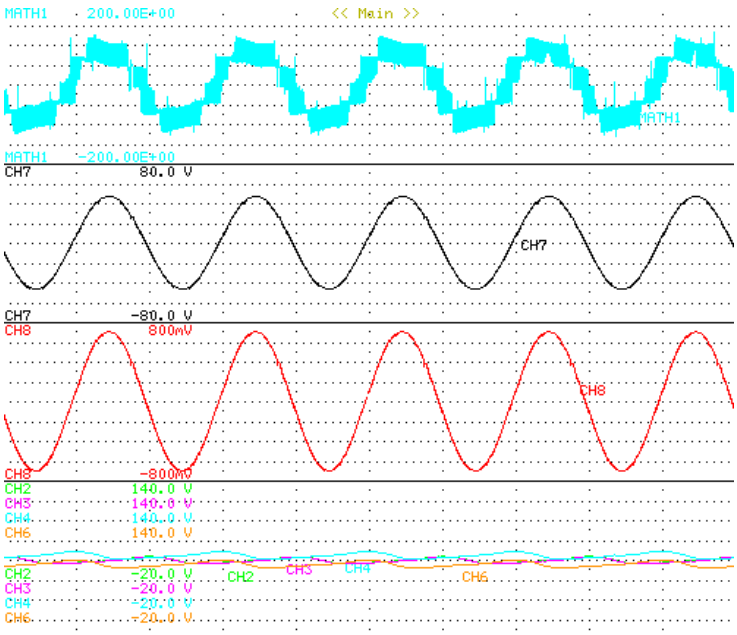


Figure 6.11 Experimental results for MMC operation in close loop current control and submodule voltage balancing: output voltage levels, output voltage, load current, submodule voltages (10 ms/div.).

As the load is resistive, the output voltage of the MMC is the product of the current with the resistor value, resulting in a 32.5 V RMS voltage signal. The output current follows the reference stipulated and the voltage across all the submodules remain constant with a medium value 60 V.

6.7 Electric Power Grid Interface with Current Control

With the validation of both the submodules voltage balancing strategy and the output current control of the MMC, all the conditions were gathered for the final validation of the power converter operating in interface with the electrical power grid, using a step down transformer for insulation, as well as lowering the voltage at stake, thus improving the security of the tests, as well as the facility to perform such tests, since many power supplies would be necessary for the MMC to operate an nominal voltage value. Regarding the synchronization of the MMC with the electrical power grid, Figure 6.12, presents the results of the PLL response in steady state prevenient from the DAC where can be observed the synchronism in both phase and amplitude. The black signal refers to the PLL output, while the pink refers to the electrical power grid voltage, both in a 2 V/div.. As can be inferred from the visualization of the signals, PLL is fully synchronized with the grid.

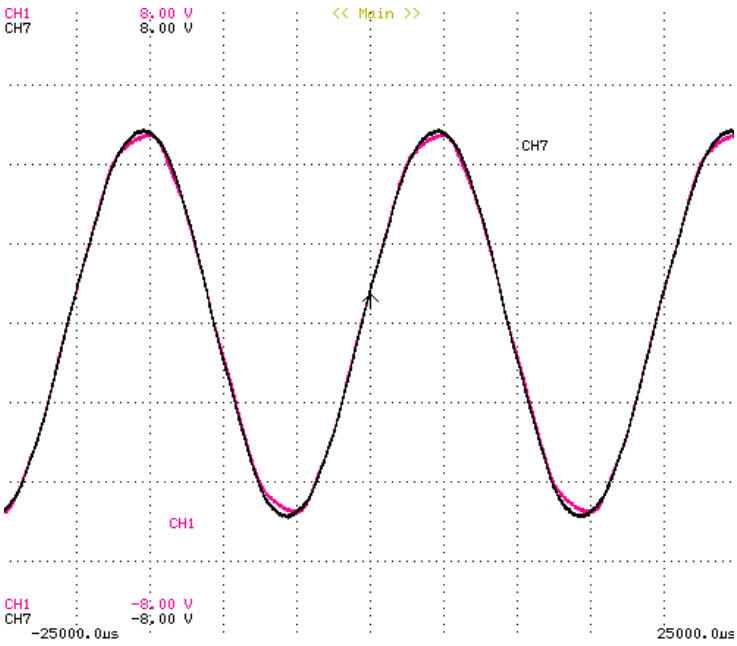


Figure 6.12 PLL steady state behavior (5 ms/div.).

Regarding the tests for the final validation of the MMC, as main objective of this dissertation, the output of the power converter was connected to the electrical power grid by a step-down transformer from 230 V RMS to 50 V RMS. The split DC-link of the power converter was powered with 240 V, 120 V in each power supply. As the voltage across the capacitors of the submodules possess a high value, a pre charge was effectuated using the 100 Ω resistors in series with both arms present in the prototype. In the chosen topology, the pre charge circuit can only charge the capacitors to half the voltage nominal voltage, 60 V in is particular case. The pre charge circuit also protects the converter against short circuits in the AC side since the resistors are placed in series with the power circuit and are later bypassed by a circuit breaker. Regarding the reference value for the output of the MMC, the results presented were acquired for a 300 W output reference. The output voltage of the converter is imposed by the grid, only varying the current output of the converter.

In Figure 6.13, the results for a 300 W power reference in interface with the electrical power grid are presented. The results contain the output voltage levels of the MMC measured across the inductive filters in blue, the output voltage of the converter in black with a 20 V/div. scale, the output current of the converter in red with a 2 A/div. scale and the voltage across the submodules with a 20 V/div. scale as well.

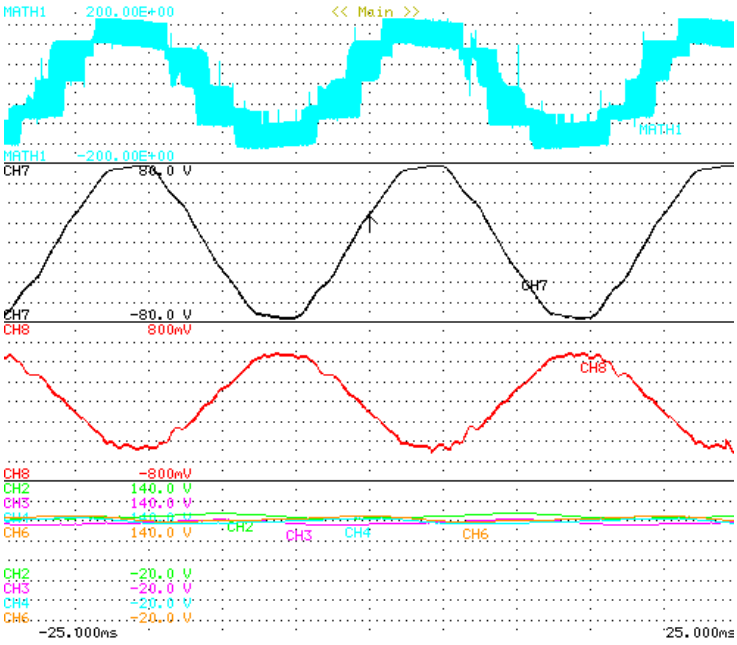


Figure 6.13 Experimental results for MMC operation in interface with electrical power grid: output voltage levels, output voltage, load current, submodule voltages (5 ms/div.).

As can be observed, the output voltage of the converter is slightly above the 50 V RMS, which is necessary for the power converter to inject power in the electrical grid. As the power converter in indeed injecting power in the electrical grid, the current is in phase opposition with the output voltage, possessing however slight distortion in its waveshape. Regarding the voltage across the submodules, using 120 V in each power supply of the DC-link, the medium voltage of the arm voltage settled at 200 V, thus selecting 100 V for reference for each submodule, and it can be observed that the balancing is successfully obtained. Recurring to a digital wattmeter, the measured power output of the MMC was 302 W.

Regarding the operation of all power converters, the semiconductors temperature is of major concern since the heat degrades the conduction characteristics, which results in more power losses in the circuit. This leads to a cycle of loss in efficiency, and, as such, the temperature of the IGBTs and corresponding heat sink was monitored at all stages, recurring to a thermal camera. After 20 minutes of operation with an output power of 302 W, with a room temperature of 26°C, the temperature in the heatsinks of the IGBTs of all submodules was measured, having verified a 33°C temperature in all measurements, meaning an equal raise of 7°C in all submodules IGBTs. This test also allowed the verification that after 20 minutes of operation, the behavior of the power converter remained unshaken.

At last, it was calculated an approximation of the efficiency of the MMC using a digital wattmeter in the input, and a digital wattmeter in the output of the converter. This test was performed for three different values of output power, as presented in Table 6-2.

Table 6-2 MMC efficiency depending on the output power.

Output Power	Efficiency
99 W	89%
202 W	90%
302 W	91%

6.8 Conclusion

After the implementation of the MMC and auxiliary circuits, the experimental validation of the entire system is of paramount importance to ensure the good functioning of the prototype, as well as the safety of the ones around it. In a first stage, the tests were conducted in the submodules individually thus validating the four half bridge circuits and auxiliary circuitry. As the functioning of the submodules was validated, the following steps consisted of the validation of the entire system.

In this chapter, several experimental results were laid out regarding the control of the MMC. The main goal was to interface with the electrical power grid, however, in order to do so, it was necessary to validate and understand the control of the power converter.

The first control validated was open loop control, which allowed the validation of the phase shift carrier modulation technique, as well as the functioning of the power circuit. The waveform of the output voltage, however, was not quite sinusoidal, and presented slight differences between the positive and negative levels.

Then it was validated the closed loop control on the output voltage, where a significant improvement was verified comparing to the open loop control, since the output voltage of the converter became sinusoidal and symmetrical, as intended. The voltage control allowed the validation of the MMC in load transitory. Still using close loop voltage control, the submodule voltage balancing was evaluated which proved slightly different from the computational simulations, since due to power losses across the converter, the voltage in each submodule does not quite reach its theoretical value. It was also verified that the ripple on the capacitor voltages increases along with the power at stake.

The next step on the validation process was made on the current control of the MMC, where it was possible to observe that the output current of the converter follows the refence given by the DSP. This control technique is important since it is the one used in the final objective of the present dissertation, the interface with the electrical power grid.

At last, it was presented the PLL synchronism with the electrical power grid in both phase and amplitude, followed by results of the MMC operating at 300 W in interface with the electrical power grid through a 50 V step down transformer, using a split DC-link of 240 V. As the MMC was injecting power in the electrical grid, the output voltage possessed a higher value than the nominal, nearly 56 V, with a current waveform in phase opposition of the voltage. The current, however, possesses a slight distortion. Recurring to a digital wattmeter in the input and the output of the MMC, the efficiency of the converter was estimated for different values of power at stake, being 91% efficiency the best result obtained with the tests performed, where the temperature in the IBGTs of all submodules suffered a raise of 7°C in relation with the room temperature, after 20 minutes of functioning, which is a very satisfactory result.

Chapter 7

Conclusion

7.1 Conclusions

In the length of the present dissertation it is presented a full stack development of a Half-bridge submodule based Modular Multilevel Converter, from a theoretical study to computational simulations, culminating in the implementation and validation of a reduced scale prototype.

The writing of this dissertation begins with an introductory chapter where a brief contextualization regarding multilevel converters in the field of power electronics is provided, discussing the advantages and disadvantages of this family of electronic power converters, with special focus on the particular converter in study, the MMC. In the first chapter, it is introduced the proposed topology that is discussed in the course of the dissertation, in a block diagram containing the subdivisions in an high-level approach of the implementation of the power converter. The chapter carries on with the presentation of the main personal and professional motivations, as well as listing the objectives of the present dissertation.

After a brief introduction, the main applications of the use of multilevel converters are presented in the second chapter, with special attention to the application of the MMC in particular since it is the topic of this dissertation. As such, after a long study of the literature, it was verified that the MMC most common usage is very high power and high voltage systems, mainly in HVDC systems for the interface of renewable energies, such as wind power to electrical grids in DC current at a very high voltage. However, the literature proposes that MMC are covered by a wide spectrum of possible applications, where some take advantage or particular characteristics of the MMC, such as medium-voltage motors and static compensators that under specific conditions, can operate without the use of a insulation transformer. The study of the applications where the MMC is used proved to be of fundamental importance, since it aroused a motivation to improve the personal knowledge of different fields of power electronics, namely in wind power applications.

The third chapter starts with a discussion in further detail of the characteristics of the multilevel converters, namely the advantages and disadvantages in comparison to the conventional power converters. In the length of this chapter, several topologies of multilevel converters were approached presenting a brief explanation, as well as a switching state table in order to allow the better understanding

about the functioning of the topologies. Then it was introduced the MMC concept, where different submodules were discussed mostly in terms of output levels, number of components and control complexity. Based on such comparative study, the chose topology of the submodules of the MMC selected for this dissertation was the Half-Bridge, due to a smaller number of components, resulting in less complexity in the hardware development, resulting however in the loss of an output level in each submodule.

After enumerating several converter and submodule topologies, the third chapter carries on with the presentation of modulation and control techniques for the MMC. Regarding the modulation of the power converter, the two base techniques were discussed, namely phase shift carrier and level shift carrier. Each technique was studied, and it was verified that regarding MMC, the level shift carrier causes uneven power losses across the submodules, thus reducing both the efficiency in long term, and also the lifetime of the converter in good functioning conditions, since some submodules would suffer much more wear than others. The phase shift carrier proved to be a simple, yet power modulation technique for the MMC. Regarding the control of the MMC, two different techniques were introduced, the PI controller and the model predictive control. Both techniques go along with the modulation, which results in a constant switching frequency for the submodules of the MMC, defined by the carrier signals of the modulation. The chapter ends with the submodule capacitors balancing technique, which allows a even distribution of the power among all the submodules, thus reducing the circulating current of the MMC.

The fourth chapter begins with a detailed explanation of the functioning of the proposed topology, to allow a better comprehension of synthesis of the output signals of the MMC. Following up, since the converter is meant to interface with the electrical power grid, it was presented the PLL algorithm implemented, as well as computational simulation results to validate the synchronization with the grid. The chapter carries on with the computational simulations for a MMC with four submodules in each arm, in order to create an approximate version of the system in nominal operation. The rated power for the simulation was set to 5 kW, the power converter at stake is single phase. The simulations validated the functioning of the proposed topology in steady state operating and under power transitory, while always keeping the voltage of the capacitors of each submodule balanced, with a 100 Hz ripple. In a final stage of the chapter, a reduced scale simulation model was presented, in order to support and serve as comparison to the implementation and testing of the prototype.

The fifth chapter lays out the implementation process of the experimental prototype developed in the scope of this dissertation. As the converter allows a modular construction, that feature was availed to the

most, which proved most valuable in troubleshooting of the power circuit. As such, each submodule was built in its own board, containing the capacitors for a DC-link of the submodule, IGBTs, voltage and current sensing, gate protection circuits and surge voltage protection recurring to TVS. The driver circuit was also placed in a separate board in order to create a system with driver modularity as well. Regarding the control circuits of the prototype, a dock station was developed in four-layer PCB, in order to create a centralized platform to facilitate the control of the power converter. A second board was used containing an 16-bit external ADC, signal conditioning and hardware protection circuits, to ensure a safe and precise data acquisition from the sensors. The implementation of the entire prototype was carefully planned in terms of circuits positions as well as the necessary connections to reduce the electromagnetic compliance, as well as the ground loops, thus mitigating the amount of noise caused by the hardware.

After the implementation of the entire prototype, the sixth and final chapter of the present dissertation reports the experimental tests carried out to perform the validation of the proposed topology. At first, each submodule was evaluated individually with an RLC load in order to synthesize a sinusoidal waveform on the output. In this test, it was possible to validate the effectiveness of the selected deadtime, as well as the functioning of each submodule individually. Then, the functioning of the prototype was a whole was validated in open loop, where two details were observed in the synthesized voltage signal: (i) the waveshape was not sinusoidal, only an approximation with discrepancies in the positive and negative levels; (ii) the peak voltage value did not reach the refence value due to voltage drops in the semiconductors. Moving on to the close loop voltage control, using a PI controller the output voltage became sinusoidal and symmetrical, as intended, and the steady state error almost inextant. This control allowed the validation of the MMC in load transitory operation, with a dynamic response always inferior to 5 ms. Next, the submodule voltage balancing results were presented, resulting in the validation of proposed topology in full. At last, the current control was evaluated to prepare the power converter to interface with the electrical power grid, which was the final objective of this dissertation.

The present dissertation was developed according to the waterfall methodology, as extensively described. Only after a bibliographical revision and study of the literature did the development of the power converter itself begin. The computational simulations presented as a powerful tool for the tuning of the control algorithms, as well as the power circuit validation. However, throughout the implementation and validation process of the experimental prototype, it is possible to verify that the simulations can only reach so far. Countless non idealities that do not appear in the simulations were encountered during the final stages of the project, resulting in results slightly different from the ones obtained in the simulations. As such,

next are presented the main conclusions achieved with this dissertation work related to the Development of a Single-Phase Modular Multilevel Converter:

- The development of this work promoted the acquisition of knowledge in diverse areas that were not taught during the course, which was of paramount importance for the full development of a Modular Multilevel Converter from scratch. As nowadays there an overflow of information available, the initial investigation work was developed with caution, searching for trustworthy sources that would support the work development.
- Regarding the computational simulations, several models were developed and improved daily, each time perfecting the operation of the system, as well as obtaining more and more knowledge about power electronics and control algorithms.
- The implementation of the prototype was the stage where most time was dedicated but also where more knowledge was acquired, since many different tasks were accomplished: from the selection of the components to the design of the PCBs, where countless details were considered to create a robust system; the development of a unified prototype for the MMC counting with power circuits and control properly separated physically with optimized connections to reduce noise; and finally, the software development where many unknown knowledge were acquired with the constant study of the datasheet and technical refence manual of the DSP in order to implement a robust control unit.
- The experimental validation of the power converter proposed was successfully accomplished, presenting satisfactory results in different stages of operation, and with different types of control, both in voltage and in current.
- Regarding the voltage across all the submodules, it was verified that even though the waveshape and the ripple match the simulations, due to power losses across the converter, the medium value of the voltage was slightly inferior to the theoretical, which was considered in the control of the MMC, most specifically, in the submodule voltage control.
- Regarding the operation in electrical power grid interface, it was verified that the waveform of the output voltage of the MMC is imposed by the grid voltage. However, since the power converter was injecting power in the electrical power grid, the output voltage was approximately 6 V higher in order to be able to successfully inject power, due to voltage drops on the coupling coils. Furthermore, the waveshape of the current presented some distortion and it was verified experimentally that the efficiency of the converter increases with the power at stake. At a 300 W operating power, the temperature in the heatsink of the IGBTs suffered a raise of 7°C from the room temperature.

The present dissertation required a substantial amount of computational simulations, hardware and software. Regarding the hardware used in the present dissertation, apart from the board presented in Figure 5.17 contemplating the external ADC and signal conditioning, all the hardware was fully developed by the author od this dissertation. Regarding the software and computational simulations, both were fully developed by the author.

7.2 Suggestions for Future Works

Once achieved the conclusion of the experimental validation of the developed prototype, a retrospective was made about all the work elaborated in the scope of the present dissertation. With the purpose of achieving better results, several observations were made about possible ways to improve the overall performance of the system.

As the driver for each submodule was implemented in separate boards, it would be different to evaluate the performance each the MMC using different driver circuits, with a variation of the driving voltage in order to compare different results to choose the most appropriate. As for the submodules, the migration to full-bridge would be advantageous, since each submodule regenerates one more level than the half-bridge, with possibility of operating with the double of frequency.

Regarding the semiconductor technology, it would be interesting migrate to four pin SiC in order to be able to raise the switching frequency, which results in lower switching losses due to the SOAr curve of the SiC MOSFETs. The IGBTs used in the prototype share the same encapsulation as the four pin SiC, which would allow a direct placement in the submodules, without changes in the power board. The driver, however, should be revised to such purpose. To further reduce the parasitic inductance created by the length of the pins, seven pin SMD SiC MOSFETs could be used. In order to do so, the submodule board would have to be redesigned to fit the alteration, since the pinout is completely different.

The size of the prototype facilitated hardware debug and troubleshooting. However, several modifications could be made in order to migrate to a significatively more compact version. Regarding the voltage and current sensing, more compact sensors could be used, namely SMD with internal protections, significatively reducing the size of each submodule, as well as adding redundancy in the protection of the MMC. Regarding the boards for DSP dock station and for the external ADC and signal conditioning, both could be combined into a single board.

Even though the MMC was tested operating in electrical power grid interface though a 230 V to 50 V RMS step-down transformer, it would be interesting to test the converter in nominal conditions, adding more submodules to each arm in order to reduce the THD and the stress on the semiconductors even further, considering the option to add two additional legs on the converter, thus migrating to a three-phase MMC, as commonly seen.

Another major improvement would be to implement an automatic mechanism to turn on and off the entire system, containing connection to the electrical power grid, submodule capacitors pre-charge and bypass. Complementary to this mechanism, a graphical interface could be implemented in order to facilitate a real time observation of the value of all the variables of the system, as well as allowing the control and command of the MMC.

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Appendix 1 – Main Loop Code

```
while(1){

        if(update)
            sinwave(operation_mode);

        if(enable){
            GpioDataRegs.GPASET.bit.GPIO14 = 1; //enableout
        }else if(!enable){
            GpioDataRegs.GPACLEAR.bit.GPIO14 = 1;
        }
        i_up = V_A[0];
        i_down = V_A[1];
        i_out = V_A[2];
        v_out = V_A[3];
        v_sm3 = V_B[0];
        v_sm4 = V_B[1];
        v_sm2 = V_B[2];
        v_sm1 = V_B[3];

        if(IPCRtoLFlagBusy(IPC_FLAG1) ){        // End Read ADC

            switch(operation_mode){
            case 0: //OpenLoop
                comparador1=mysin[sinindex] + PWM_Period_CCCA/2 + aux1;
                comparador2=mysin[sinindex] + PWM_Period_CCCA/2 + aux2;
                comparador3=(-1)*mysin[sinindex] + PWM_Period_CCCA/2 + aux3;
                comparador4=(-1)*mysin[sinindex] + PWM_Period_CCCA/2 + aux4;
                Update_PWM();
                break;
            case 1: //Close Loop Voltage
                error_PI_out = mysin[sinindex] - v_out;
                sum_PI_out += error_PI_out;
                com_PI_out = error_PI_out * kp_vout + sum_PI_out*ki_vout;
                if(com_PI_out > 1000)
                    com_PI_out = 1000;
                if(com_PI_out < -1000)
                    com_PI_out = -1000;

                comparador1 = com_PI_out + PWM_Period_CCCA/2 + aux1;
                comparador2 = com_PI_out + PWM_Period_CCCA/2 + aux2;
                comparador3 = PWM_Period_CCCA/2 - com_PI_out + aux3;
                comparador4 = PWM_Period_CCCA/2 - com_PI_out + aux4;
                Update_PWM();
                break;
            case 2: //Close Loop Current
                error_PI_iout = mysin[sinindex] - i_out;
                sum_PI_iout += error_PI_iout;
                com_PI_iout = error_PI_iout * kp_iout + sum_PI_iout*ki_iout;
                if(com_PI_iout > 1000)
                    com_PI_iout = 1000;
                if(com_PI_iout < -1000)
                    com_PI_iout = -1000;

                comparador1 = com_PI_iout + PWM_Period_CCCA/2 + aux1;
                comparador2 = com_PI_iout + PWM_Period_CCCA/2 + aux2;
```

```
                comparador3 = PWM_Period_CCCA/2 - com_PI_iout + aux3;
                comparador4 = PWM_Period_CCCA/2 - com_PI_iout + aux4;
                Update_PWM();
                break;
            case 3: // Voltage Balance
                error_PI_iout = mysin[sinindex] - i_out;
                sum_PI_iout += error_PI_iout;
                com_PI_iout = error_PI_iout * kp_iout + sum_PI_iout*ki_iout;
                if(com_PI_iout > 1000)
                    com_PI_iout = 1000;
                if(com_PI_iout < -1000)
                    com_PI_iout = -1000;

                SM_voltage_control();
                comparador1 = com_PI_iout + PWM_Period_CCCA/2 + errorV1 + aux1;
                comparador2 = com_PI_iout + PWM_Period_CCCA/2 + errorV2 + aux2;
                comparador3 = PWM_Period_CCCA/2 - com_PI_iout + errorV3 + aux3;
                comparador4 = PWM_Period_CCCA/2 - com_PI_iout + errorV4 + aux4;
                Update_PWM();
                break;
            case 4: // Power Grid Interface
                error_PI_iout = y*iref_max - i_out;
                sum_PI_iout += error_PI_iout;
                com_PI_iout = error_PI_iout * kp_iout + sum_PI_iout*ki_iout;
                if(com_PI_iout > 1000)
                    com_PI_iout = 1000;
                if(com_PI_iout < -1000)
                    com_PI_iout = -1000;

                SM_voltage_control();
                comparador1 = com_PI_iout + PWM_Period_CCCA/2 + errorV1 + aux1;
                comparador2 = com_PI_iout + PWM_Period_CCCA/2 + errorV2 + aux2;
                comparador3 = PWM_Period_CCCA/2 - com_PI_iout + errorV3 + aux3;
                comparador4 = PWM_Period_CCCA/2 - com_PI_iout + errorV4 + aux4;

                Update_PWM();
                break;
            }

            pll();

            dacD = (int)(V_OUT_pll * aux6);
            dacE = (int)(ydelay*2000);
            dacF =(int)(y*2000);
            dacG = v_out * aux5;
      //      DAC_Update( dacA, dacB, dacC, dacD, dacE, dacF, dacG, dacH);
            IPCRtoLFlagAcknowledge(IPC_FLAG1);
           IPCLtoRFlagClear(IPC_FLAG1);
        }
    }
}
```

Appendix 2 – Submodule PCB Layout

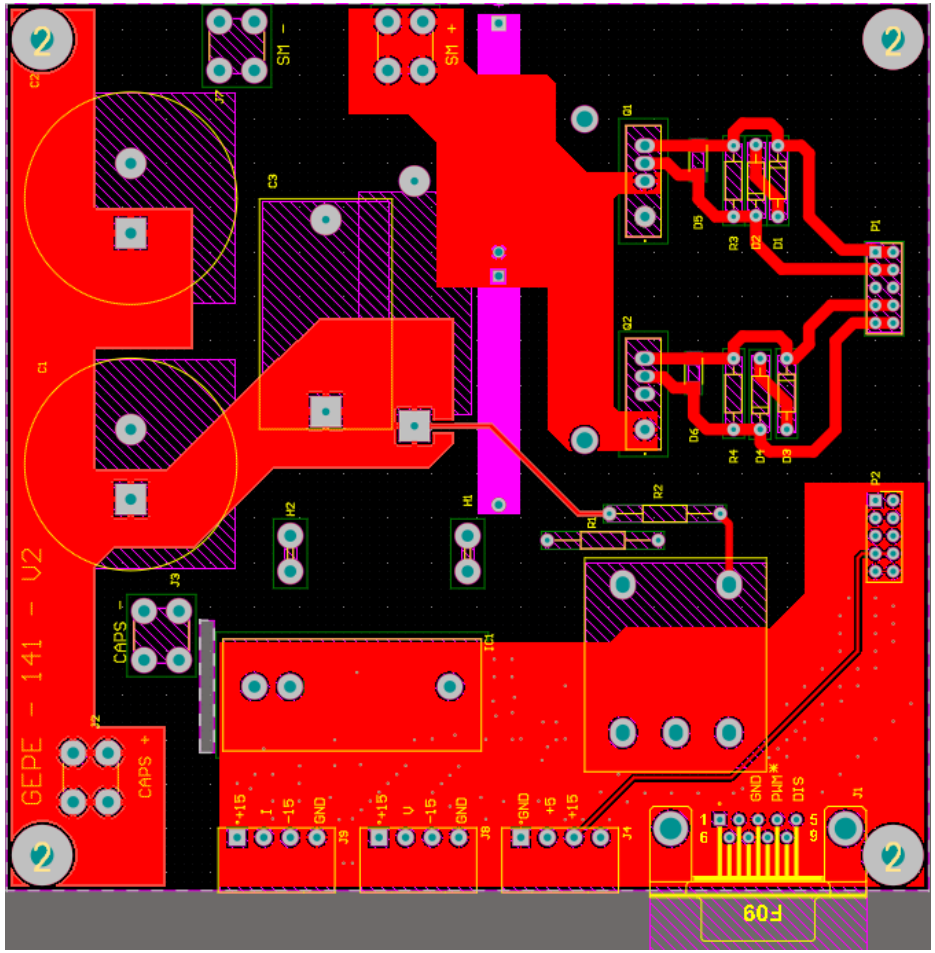

Figure A1: Submodule PCB layout in Altium Designer: Top View.

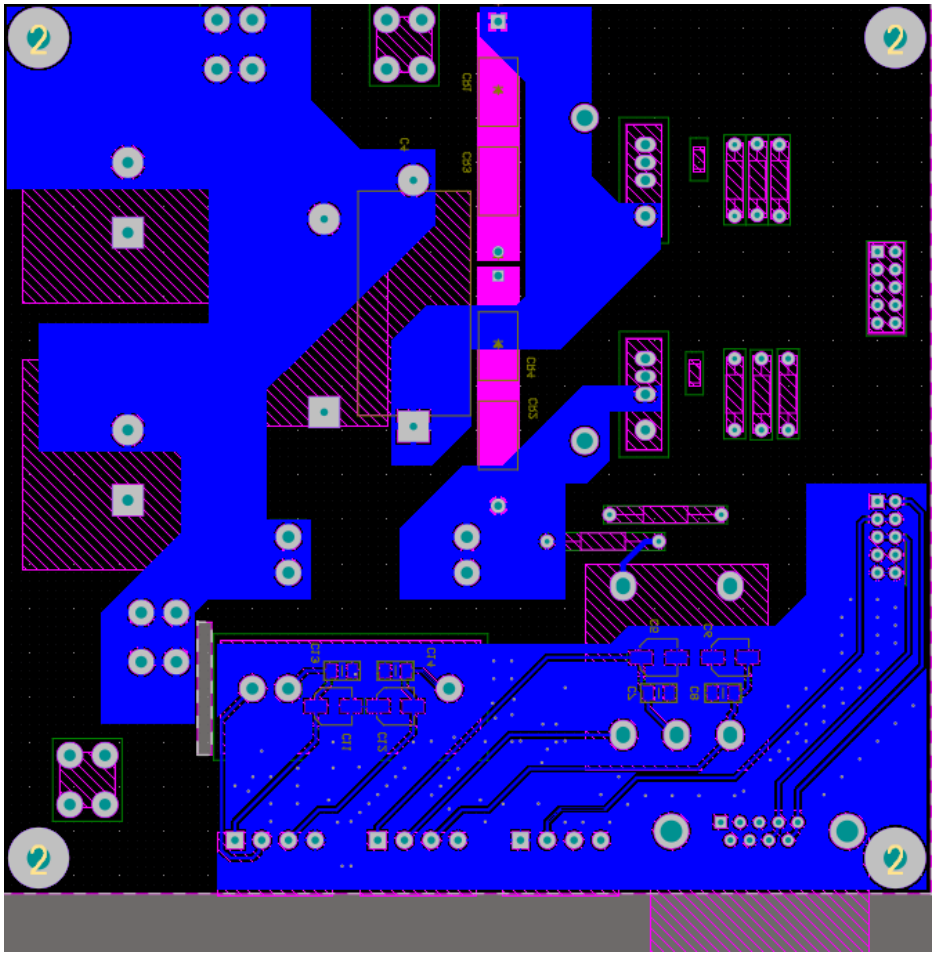

Figure A2: Submodule PCB layout in Altium Designer: Bottom View

Appendix 3 – Driver PCB Layout

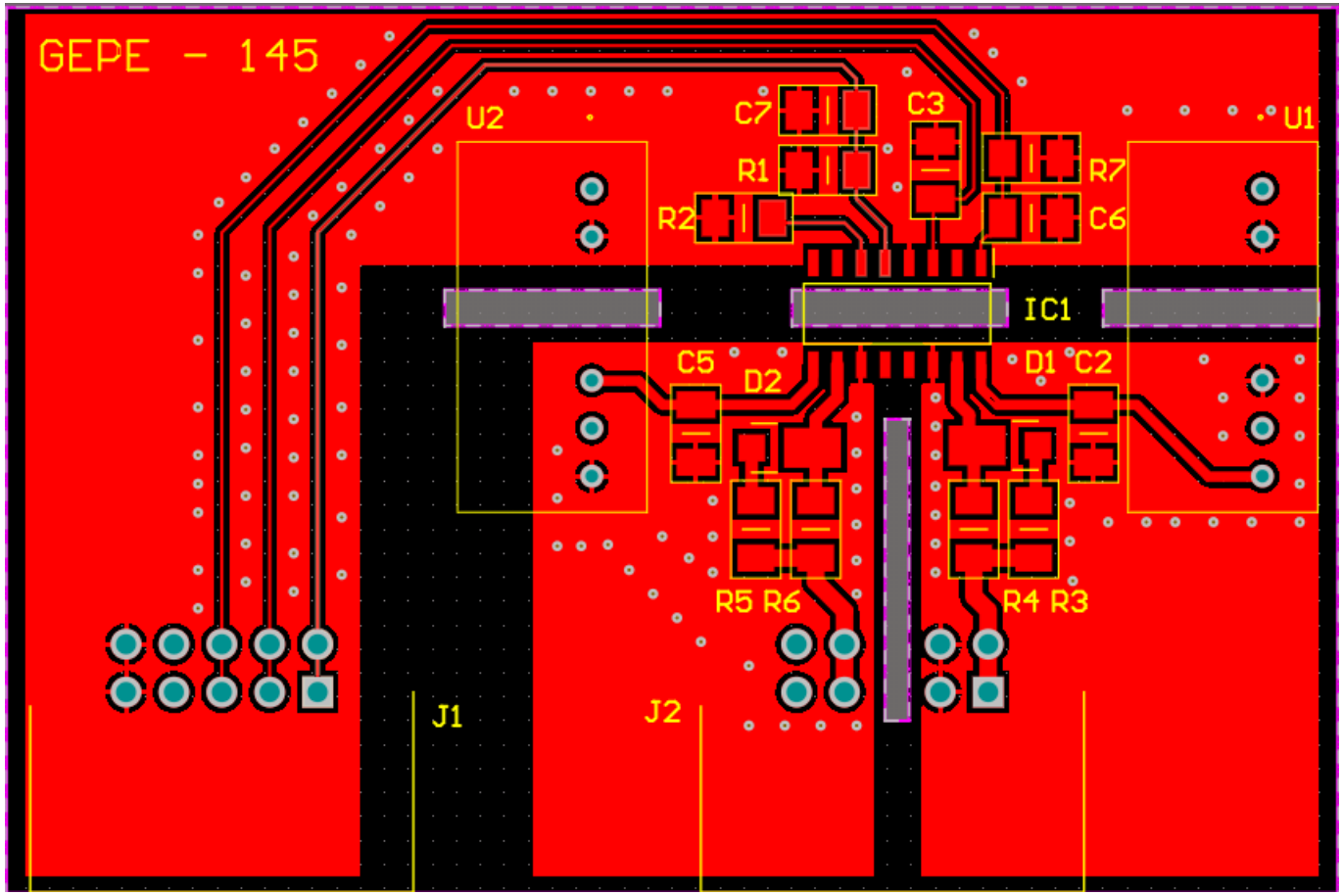

Figure A3: Driver PCB layout in Altium Designer: Top View.

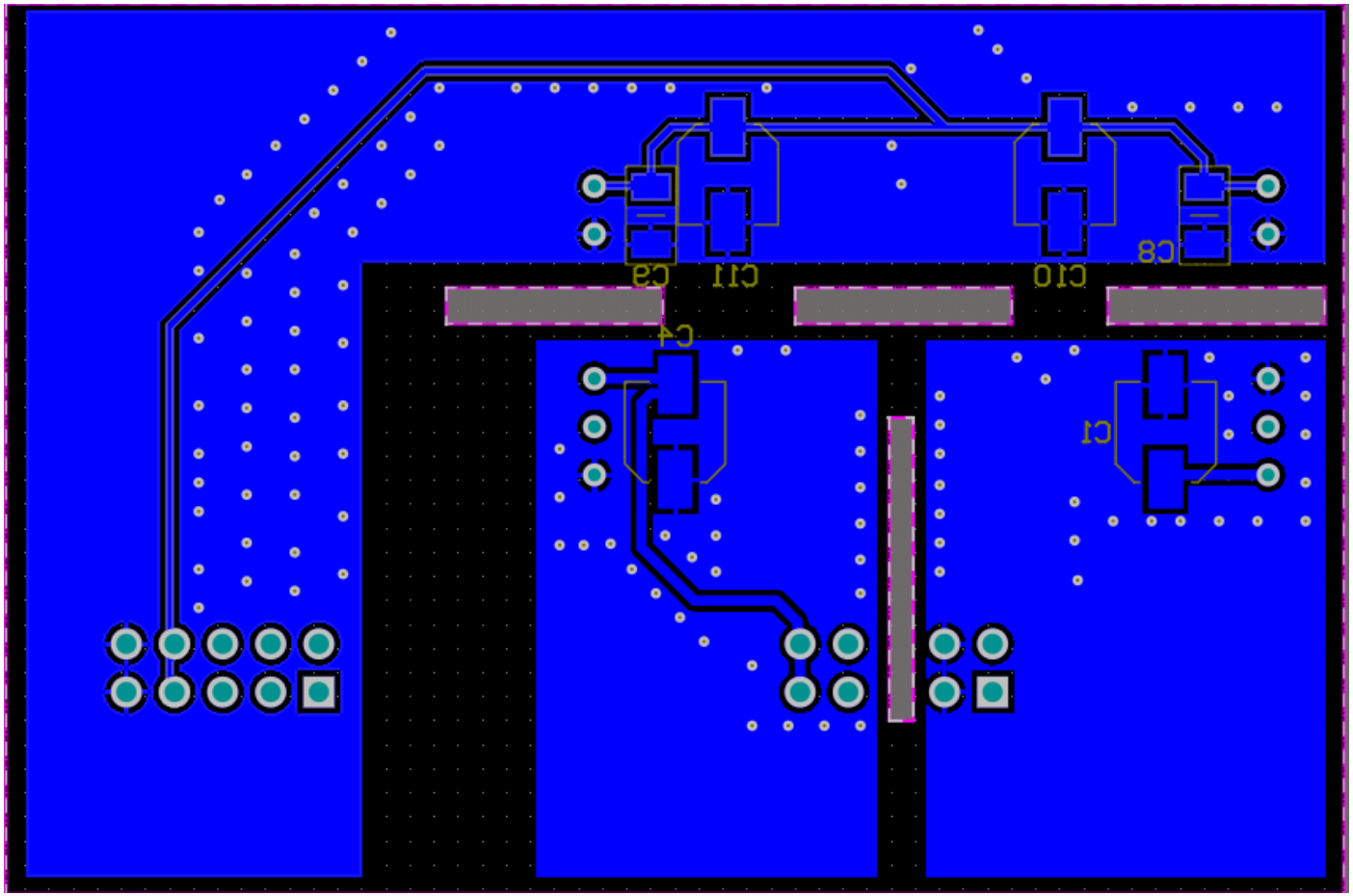

Figure A4: Driver PCB layout in Altium Designer: Bottom View

Appendix 4 – Dock Station PCB Layout

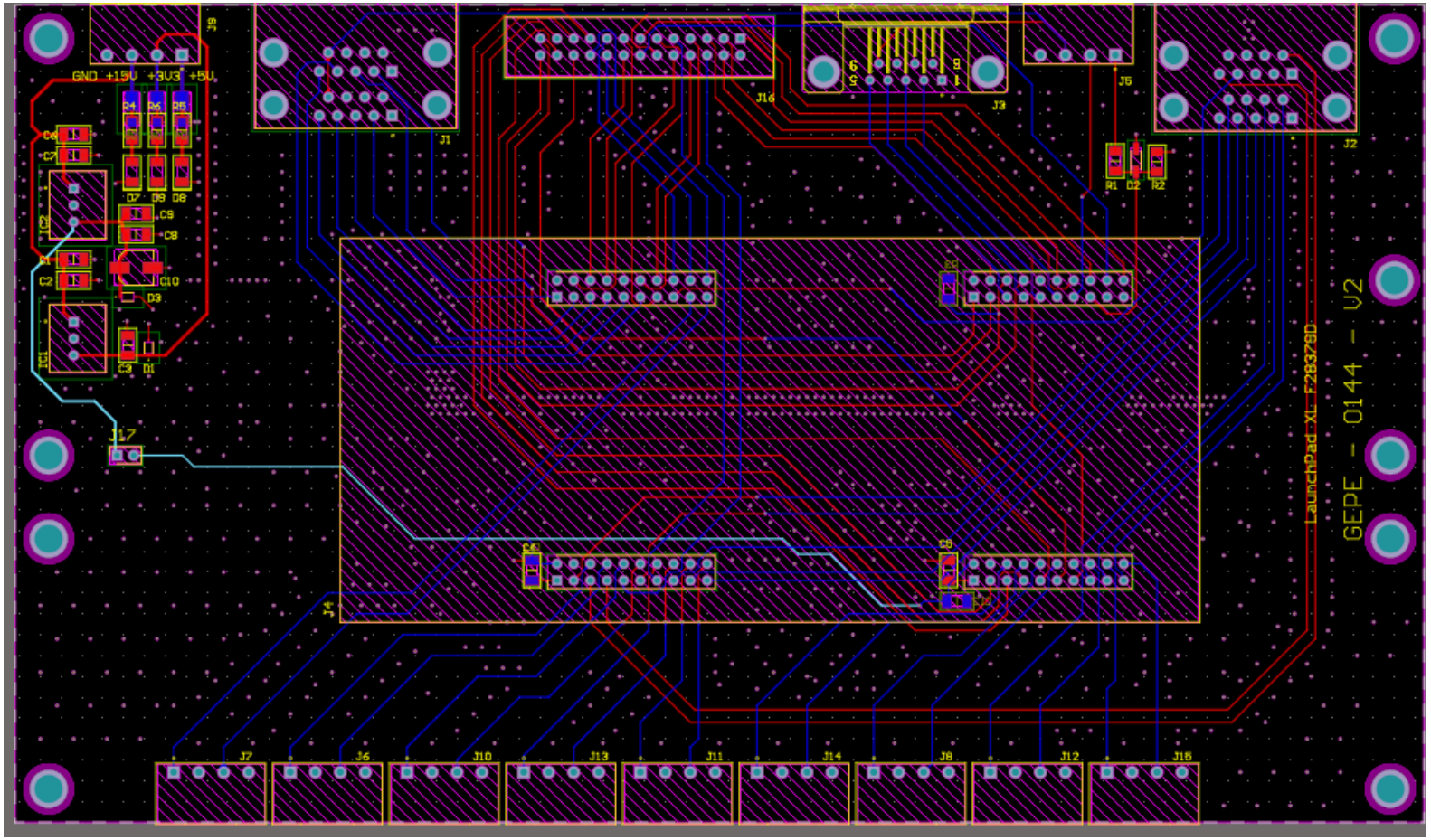

Figure A5: Dock Station PCB layout in Altium Designer.