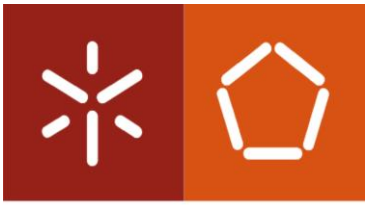

Universidade do Minho
Escola de Engenharia

Lucas Morais Baptista

Graphene transistors for radio frequency applications

Dissertação de Mestrado
Mestrado Integrado em Engenharia Física
Área de Especialização em Dispositivos, Microssistemas e Nanotecnologias

Trabalho efetuado sob a orientação do
Professor Doutor Paulo Mateus Mendes e
Professor Doutor João Pedro S. H. A. Alpuim

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DECLARAÇÃO

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A todos um especial obrigado por estarem presentes e pelo apoio oferecido.

RESUMO

O grafeno atraiu imensa atenção devido à alta mobilidade dos portadores de carga, tornando um potencial novo material para eletrónica de radio frequência. Transístores fabricados com grafeno, fabricados até à data, possuem frequência de corte intrínsecas de 427 GHz. O fabrico de transístores de grafeno para aplicações de radiofrequência é dificultado devido às tecnologias de fabrico CMOS não poderem ser usadas, no seu estado atual, para este novo material. Neste trabalho, uma deposição física da porta e do óxido da porta foi escolhida de forma a minimizar os danos causados à rede de grafeno e um processo de auto alinhamento para reduzir as resistências de contacto.

De forma a maximizar as figuras de mérito das estruturas pretendidas, foram feitas simulações que correlacionam os parâmetros físicos do dispositivo com as figuras de mérito. Os resultados obtidos dessas simulações mostraram que a elevada discrepância entre as figuras de mérito intrínsecas e extrínsecas resultam do elevado rácio entre as capacitâncias da porta-dreno e porta-fonte para as capacitâncias parasíticas da porta e do dreno. Um aumento da camada de passivação e redução dos pads resultam na redução significativa do rácio entre os dois. As simulações também mostraram que reduzindo as resistências, capacidades e indutâncias parasitas resulta numa melhoria das figuras de mérito. A redução da largura do canal e aumento do comprimento do canal resulta no aumento das figuras de mérito intrínsecas e consequentemente as extrínsecas.

O grafeno foi crescido por CVD numa folha de cobre, que produz alta qualidade e grandes áreas, e transferido para um substrato isolador. Nano-fios de níquel foram crescidos por deposição eletroquímica usando estruturas de oxido de alumínio anodizado (AAO) com uma camada de semente fina de ouro e uma mistura de $NiSO_4$, $NiCl_2$ e H_3BO_3, produziram nano-fios com diâmetros entre 200 e 400 nm. A estrutura foi removida com uma solução de NaOH, expondo os nano-fios.

A cobertura dos nano-fios foi realizada através da oxidação do níquel e deposição de dióxido de silício. Ambas estas estruturas de núcleo-concha foram utilizadas na fabricação dos transístores.

Os nano-fios núcleo-concha foram libertados da camada semente com uma solução de KI e I_2, e subsequentemente aleatoriamente posicionados em cima do grafeno. Imagens de alta resolução foram obtidas da exata posição dos nano-fios e com a ajuda de marcadores de Titânio-

Tungstênio (TiW), previamente depositados, mascaras para os processos litográficos foram desenhadas, estabelecendo um comprimento do canal em 3 μm. O processo de auto alinhamento foi por fim usado para depositar os contactos do dreno e fonte (Cr/Pd), alinhando-os perfeitamente e reduzindo a resistência de contacto por consequência.

Um processo dieletroforético foi também desenvolvido para posicionar precisamente os nano-fios no substrato e possibilitar a escalabilidade do processo de fabrico.

Por último, caracterização dos dispositivos fabricados foi realizada. Os dispositivos fabricados na primeira iteração mostraram baixo isolamento entre a porta e o canal, sendo esta atribuída ao dielétrico escolhido. Os dispositivos da segunda iteração do processo de fabrico foram impossíveis de caracterizar eletricamente devido à falta de conexão elétrica após a primeira ligação das sondas de medição.

Palavras-chave: grafeno, transistor de efeito de campo, nanofio, fabricação

ABSTRACT

Graphene has attracted an immense amount of attention due to its high carrier mobility, making it a potentially new material for radio-frequency electronics. Transistors fabricated with graphene have reached intrinsic cut-off frequencies of 300 GHz. The fabrication of graphene RF transistors is challenging as most of the standard CMOS technologies cannot be employed in their current state to this new material. In this work, a physical deposition of the gate and gate oxide was chosen to minimize the damages to the graphene lattice and a self-aligned process to reduce the contact resistance.

In order to maximize the figures of merit of the intended structure, simulations were made correlating the physical parameters to the figures of merit. Results obtained from these simulations showed that the high discrepancy between intrinsic and extrinsic figures of merit resulted from the high ratio between the gate-drain and gate-source capacitances to the parasitic gate and drain parasitic capacitances. An increase in the passivation layer and reduction of the gate and drain pads results in a significantly lower ratio between the two. Simulations also showed that, by minimizing the parasitic resistances, capacitances and inductances results in the increase of both intrinsic and extrinsic figures of merit. Reduction of the channel length and increase of the channel width results in the increase of the intrinsic, and subsequently extrinsic, figures of merit.

Graphene was grown by CVD on a copper foil, which yielded high quality and large area graphene, and transferred onto the insulating substrate. Nickel nanowires were grown by electrochemical deposition using an Anodized Aluminum Oxide (AAO) template with a gold seed layer and a mixture of $NiSO_4$, $NiCl_2$ and H_3BO_3, resulting in nanowires with diameters ranging from 200 to 400 nanometers. The template was removed with a solution of NaOH creating free standing nanowires. Coating of the nanowires was performed through the oxidation of nickel and deposition of silicon dioxide. Both of these types of core-shell nanowires were used in the fabrication of the transistors.

The core-shell nanowires were released from the seed layer with a solution of KI and I_2 and subsequently randomly placed on top of the graphene. High resolution images of the nanowires precise position were taken and with the aid of Titanium-Tungsten (TiW) markers previously deposited, masks for a lithographic process were designed, setting the channel width

to 3 μm. A self-aligned process was lastly employed to deposit the Drain-Source contacts (Cr/Pd), perfectly aligning them and in turn, greatly reducing the access resistance.

A dielectrophoretic method was also developed to perfectly position the nanowires on the substrate and in turn scale up the device fabrication process.

Lastly, characterization of the fabrication took place. Devices fabricated on the first run of the experiment showed poor isolation between the gate and channel of the devices. This was attributed to the dielectric choice. The second set of fabricated devices were unable to be characterized as connections made onto the devices failed to provide electrical contact after the first placement of the measuring probes.

Keywords: graphene, field-effect transistor, nanowire, fabrication

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AC	Alternating Current
AAO	Anodized Aluminum Oxide
AFM	Atomic Force Microscopy
ALD	Atomic Layer Deposition
CMP	Chemical Mechanical Planarization
CVD	Chemical Vapor Deposition
CMOS	Complementary Metal Oxide Semiconductor
DLC	Diamond Like Carbon
DI	Deionized
DC	Direct Current
EDX	Energy Dispersive X-ray
FET	Field Effect Transistor
FIB	Focused Ion Beam
GFET	Graphene Field Effect Transistor
HEMT	High Electron Mobility Transistor
HOPG	Highly Oriented Pyrolytic Graphite
INL	Iberian Nanotechnology Laboratory
ICP	Inductively Coupled Plasma
IBM	International Business Machines
IPA	Isopropyl Alcohol
LO	Local Oscillator
LNA	Low Noise Amplifier
MAG	Maximum Available Gain
MEMS	Micro Electro Mechanical Systems
MMIC	Monolithic Microwave Integrated Circuit
PTCA	Perylene Tetra Carboxylic Acid
PECVD	Plasma Enhanced Chemical Vapor Deposition
PLD	Physical Layer Deposition
PVD	Physical Vapor Deposition
PDMS	PolyDiMethylSiloxane

PMGI	PolyMethylGlutarimide
PMMA	PolyMethyl MethAcrylate
RF	Radio Frequency
RIE	Reactive Ion Etching
SEM	Scanning Electron Microscope
TEM	Transmission Electron Microscope
TMA	TriMethylAluminum

1 INTRODUCTION

Throughout the past decades there have been immense advances in the field of electronics which affect our daily lives. These advances can be attributed to the miniaturization of electronic devices, in particular the silicon-based transistors. The number of transistors per chip has been increasing exponentially, reaching the billion mark which in turn means that the physical structure has reached the scale of nanometres. Such advances will eventually come to a halt imposed by the physical limits and to ensure a continued progress of electronic technology, alternative materials or different operating principles are needed.

1.1 Graphene technology

Graphene was first isolated in 2004 by Geim and Novolesov in 2004 [1]. It has attracted a lot of attention due to its outstanding properties and can be considered as complement to or extension of the existing silicon-based electronics.

Despite the dominant position of silicon, the interest and investment in the research of alternative materials and technologies has been steadily increasing. Device miniaturization has been the enabler of the continuous technological progress we have grown accustomed to and followed the Moore´s law. Gordon Moore stated that the size of transistors would decrease and its number on a chip would double every 18 months. This trend followed ever since and today transistors per chip have reached the billion mark. However, miniaturization of devices has reached its limit and technological progress will eventually come to a halt.

To replace the silicon technology, the new materials or processes, have to excel when compared to the dominant technology. Even with superior performance and comparable price alone will not guarantee the adoption of the new technology due to the large investment in CMOS technology. III-V semiconductors are a good example, as they excel in terms of electron mobility, but due to their high cost, they have not made it to mass manufactured consumer electronic devices.

Graphene is a zero-gap semiconductor (i.e., semi-metal) and for this reason, graphene-based field-effect transistors cannot be turned-off. This invalidates graphene to be used as silicon is

today in CMOS logic circuits. On the other hand, the graphene´s high carrier mobility, coupled with the large current density of the material, opens up the possibility of RF analogue applications.

Application such as RF communication systems, power control, sensors and actuators include some analogue components or subsystems, where the performance scaling has not been as fast as with digital processing or have not been significantly improved for a while and adoption of new technologies is thus easier. With the shift towards mobile computing, brings interest to different characteristics of materials such as light weight, flexibility and transparency.

1.2 Graphene based radiofrequency devices

Several devices for radio-frequency applications have been developed throughout the years. These range from passive components, such as capacitors and antennas, to active components, such as field-effect transistors and oscillators.

Graphene antennas were proposed and fabricated in [2]. The radiation efficiency of these antennas is lower, when compared to its metallic counterparts, however the authors claim that graphene-based antennas can be more advantageous due to its wideband properties. The fabricated antennas were measured from 8 to 12 GHz.

CMOS compatible graphene capacitors have been fabricated in [3]. The capacity density obtained was of 2.65 $fF/\mu m^2$, which is 100 times higher than RF MEMS. Through the study of the structure it was seen that, the number of fingers in the capacitor can be altered to increase the capacitance while reducing the graphene resistance. This in turn, allows for a higher Q factor for the devices. The devices fabricated achieved Q factors above 50 for frequencies between 1.1 GHz to 24.8 GHz.

Graphene ring-oscillators have been developed in [4]. Through the use of top-gated field-effect transistors, the fabricated devices achieved oscillating frequencies of 1.22 GHz.

Subsequently, a graphene mixer was also demonstrated without the need of an external local oscillator.

The previously mentioned RF components are essential for RF communication systems. Through the use of graphene in these devices, gigahertz operating systems are a possibility, with a lower cost of manufacture. However, RF communication systems require high performance from all its components. One of the key components of the RF systems is the transistor, as it is used for the mixers and doublers as well as the LNA and oscillator.

Graphene-based transistors have been fabricated ever since its discovery in 2004. The first transistors fabricated were gated through the substrate and not viable for radio-frequency applications. Several approaches have been developed for the fabrication of graphene transistors operating in the gigahertz or even terahertz band. Fabrication of said devices had to accommodate to the pre-existent and dominant silicon technology. Some of the fabrication processes used for silicon are not compatible with the new material, as it degrades it´s lattice, introducing defects and impurities, which lowers the devices performance.

Several approaches were implemented to circumnavigate these problems, and to date, graphene field-effect transistors already reach the terahertz band, in terms of cut-off frequency.

1.3 Work Motivation

The main motivation of this dissertation is to produce a fabrication method of graphene-based field effect transistors for radio-frequency applications, using, as possible, standard and large-scale clean room fabrication technologies. Graphene-based transistors fabricated previously in the research centre were not optimized for radio-frequency applications. Several methods of fabrication from literature were reviewed and based on the available tools, a physical structure was chosen.

In order to better understand how the physical parameters of the chosen structure would influence the figures of merit, modelling of the proposed transistors is required. Several models for these types of devices have been reported in literature, however, these are few and far between. A model that best describes the transistors performance must be first implemented

and validated so that it can be used later on for the development of radio-frequency circuits and devices.

As stated before, the research centre had not fabricated to date, graphene transistors for radio-frequency applications. For this reason, fabrication of graphene field-effect transistors based on the work of [5], will be implemented. This structure requires nanowires to be grown and a dielectric deposited to serve as gate and gate insulator of the device.

In order to synthesise the nanowires, electrochemical deposition of nickel onto AAO templates is the method used. Dielectric shells of nickel oxide and silicon dioxide are both experimented upon to serve as the gate dielectric.

To assess the performance of the fabricated devices and to validate the model developed, characterization of the structures is required through the use of RF probes as well as DC probes.

1.4 Contributions

During the work of this dissertation several contributions were made and will be listed below:

- A radio-frequency model was adapted from literature to match the intended fabrication structure. Performance assessment of the devices based on their physical structures took place and the figures of merit were retrieved for each of the physical layouts.

- Electrochemical growth of nickel nanowires on anodized aluminum oxide templates and subsequent shell deposition of nickel oxide and silicon dioxide was performed. Release and transfer of the synthesized nanowires was also achieved.

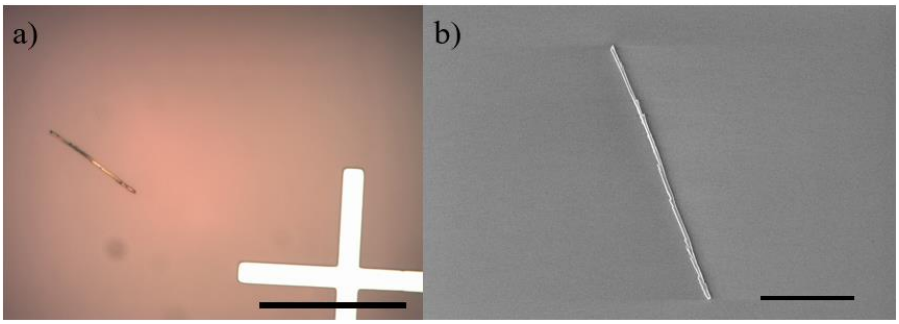

Figure 1: Optical and corresponding SEM images of the nanowires released from the seed layer. a) Scale bar: 90 μm. b) Scale bar: 10 μm.

- A method of precise nanowire placement through a dielectrophoretic process was also performed.

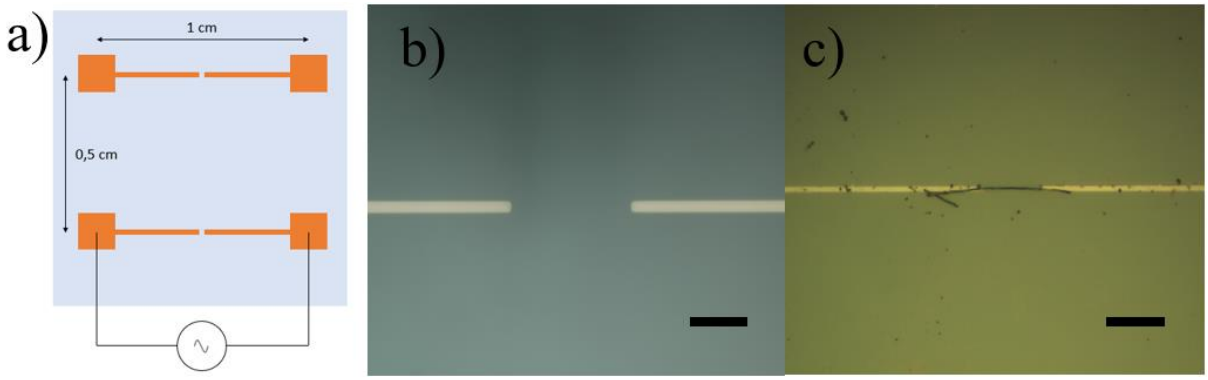

Figure 2: Dielectric assembly of nanowires. a) Top view schematic of the structure. b) Optical microscope image of the ends of a pair of electrodes. Scale bar: 10 µm. c) Optical microscope images of the electrodes of b) with an aligned nanowire between them. Scale bar: 20 µm.

- Fabrication and characterization of two types of graphene field-effect transistors was performed.

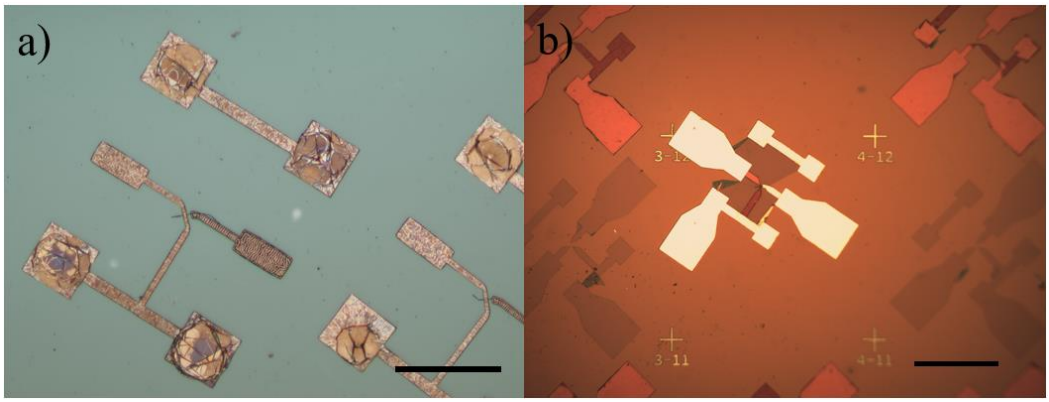

Figure 3: Resulting transistors of both the fabrication processes. a) Optical image of a graphene field-effect transistor with nickel/nickel oxide core-shell nanowire gate. Scale bar: 100 µm. b) Optical image of a graphene field-effect transistor with nickel/silicon dioxide core-shell nanowire gate. Scale bar: 200 µm.

1.5 Thesis organization

In the first chapter, a contextualization of graphene and the possibilities it brings when compared to other technologies is introduced alongside the motivation and contributions of this work.

The second chapter contains a review of graphene properties and applications for radio-frequency devices. Fabrication constraints and a state-of-the-art of field-effect transistors fabricated for radio-frequency applications is also presented.

The third chapter contains an assessment of the available technologies for the author and a transistor proposal for fabrication of the device. Device modeling is also performed to provide values for the physical layout of the device.

The fourth chapter contains the synthesis process of nickel nanowires electrochemically deposited onto anodized aluminum oxide templates.

The fifth chapter contains the fabrication process of the first graphene field effect transistors based on a core-shell nanowire gate of nickel and nickel oxide.

The sixth chapter contains the fabrication process of the second graphene field effect transistors based on a core-shell nanowire gate of nickel and silicon dioxide.

Finally, the seventh chapter contains the conclusions and future work.

2 GRAPHENE BASED RF DEVICES

Graphene has attracted a lot of attention as a possible enabler for future electronics, however fabrication of such devices has encountered several setbacks since CMOS technologies cannot be readily implemented onto this new material. Performance of graphene transistor is inherently linked to its synthesis and the device fabrication process. In this chapter, a small introduction to graphene, its properties and a review of state-of-the-art graphene synthesis and fabrication processes of graphene-based radio-frequency transistors will be presented.

2.1 Graphene

2.1.1 What is graphene?

Graphene is a 2D-material that was first isolated by Geim and Novolesov in 2004 [1] and has attracted a lot of attention due to its extraordinary mechanical, electronic and optical properties among others [6]. These properties stem from the double covalent bonds between the carbon atoms sp^2, well-establishing its monotonical hexagonal shape. Graphene is the basic structural element of other allotropes, including graphite, carbon nanotubes and fullerenes.

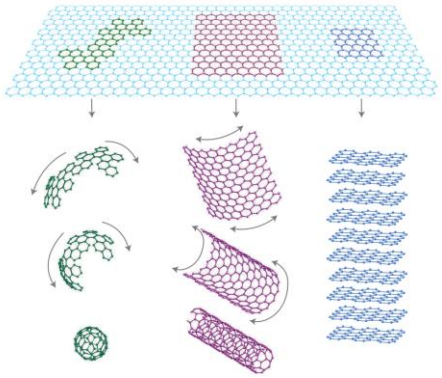

Figure 4: Graphene and its allotropes, fullerenes, carbon nanotubes and graphite, from left to right. [7]

The unitary cell is composed by two carbon atoms, alternating between them in a triangular lattice structure. The honeycomb structure is the overlap of two identical primitive lattices (Figure 5). The distance between each carbon atom in the hexagonal structure is 0.142 nm while in the reciprocal lattice is 0.42 nm.

The point K and K' have the same distance to the point of maximum symmetry (Γ) and are denominated the Dirac points. These points determine the electronic properties of graphene since there is where the Fermi level is located.

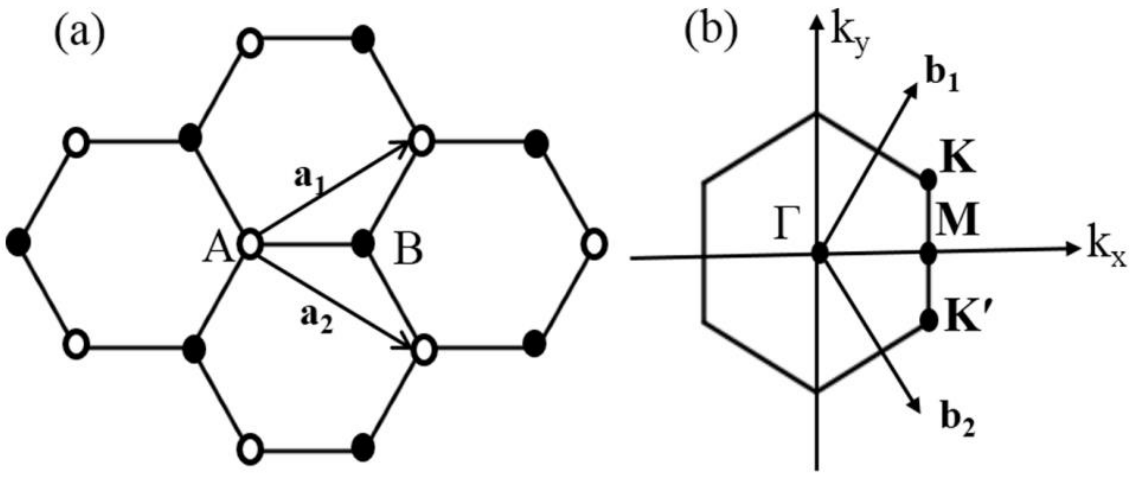

Figure 5: a) Honeycomb lattice structure of graphene (direct lattice). b) Corresponding Brillouin zone, showing the high-symmetry points.

2.1.2 Graphene properties and characterization

Graphene is a zero-bandgap semiconductor, due to its conduction and valence band touching at the Dirac points. Three of the four valence electrons participate in the bond to the next neighbour (covalent bonds) and the fourth pi orbital is perpendicular to the plane. As a consequence, the charge carriers can be described by the Dirac equation. As a semiconductor, the charge carriers present in graphene can be either electrons or holes and the carrier concentration (doping) can be changed depending on the presence of an electric field (gating). The particularity of the graphene density of states is that in the singularities, the valence and conduction bands touch, also known as the Dirac points. The charge carriers in these linear zones form what are known as the Dirac cones where the minimum conductivity is the Dirac

point. In the linear zones charge carriers have long uninterrupted paths and velocities of 1/300 the speed of light, which translates into a reduced mass, obeying to the relativistic equation (Dirac equation). Graphene over a dielectric substrate, at room temperature, has always a conductivity at the Dirac points due to the thermally generated electrons and carrier puddles that form in the graphene dielectric substrate.

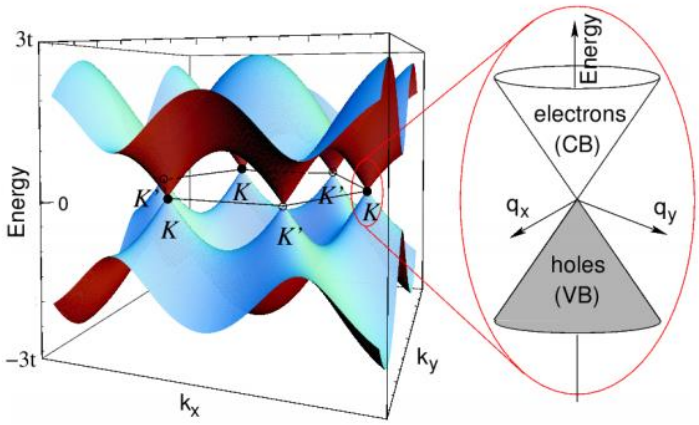

Figure 6: Energy bands of graphene obtained from the tight-binding model and zoom around the Dirac point at K. Figure retrieved from reference [8]

The covalent bonds of the carbon atoms are isometrically equal translating into a strong resistance to mechanical forces parallel to the plane. In the case of bi-layer graphene the bonds between each graphene layer are established by the Van der Walls forces (weak electrostatic force). For this reason, the mechanical exfoliation of graphene is made possible.

The thermal conductivity of graphene is given by the mobility of phonons in the lattice. Similarly to the electronic conductivity, the thermal conductivity is inversely proportional to the concentration of defects in the lattice. High thermal conductivity of graphene, higher than the exceptional copper, make it an efficient material for heat dissipation applications.

Due to the atom thick structure of graphene, its light transmittance is 97.7 % [8]. Layers added to the graphene monolayer decrease its transmittance by a factor of 2.3 %, with an approximate linear relation. The transmittance of the graphene sheet can provide the number of layers present.

Although graphene is invisible to the naked eye, it can be characterized through the spectrum of inelastic dispersion, that comes from the interaction between phonons, the Raman spectrum (Figure 7). The most intense peaks found in the spectrum are the G peak (around 1600 cm^{-1}) which is present in all graphitic materials, the 2D peak (around 2700 cm^{-1}) which only

appears on monolayer or few layer graphene films, and the D peak (around 1350 cm^{-1}) which correlates with defects on the graphene sheet. The quality of graphene is given by ratio between the G and 2D peaks as the 2D must be more intense than the G. Another form of quality assessment is the intensity of the D peak, which should be as low intensity as possible for high quality graphene sheets.

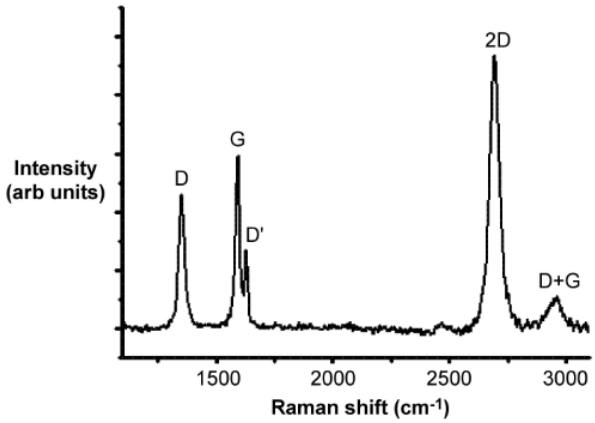

Figure 7: Raman spectrum of monolayer graphene with 514.5 nm excitation laser wavelength. Figure retrieved from reference [10]

2.1.3 Graphene applications

Fifteen years have passed since graphene was first isolated in 2004 and many research has been devoted to this material, from its synthesis and transfer, to applications that affect our day-to-day lives. Consequently, products that incorporate graphene have started to appear. Graphene properties allow for a variety of applications that range from composites and coatings, energy, sensors, and electronics, among others.

Examples such as shoes where the rubber is mixed with graphene enhancing its durability and elasticity, or the use in storage drivers as a heat dissipators, are products that already have hit the market. However, graphene still holds potential on a variety of different applications.

Graphene can also be used in photonics and optoelectronics through the combination of its optical and electronic properties. In optoelectronic devices , graphene behaves as a transparent

conducting film and is used in a dye-sensitized solar cells[9]. The flexibility of graphene can also enable the production of flexible devices such as light emitting devices[10], and touch screens[11]. Graphene absorption of light over a wide spectrum, from ultraviolet to terahertz, makes it suitable for photodetector devices such as the ultrahigh-bandwidth photodetector based on few-layer graphene reported in [12].

Field-effect transistors[13], integrated circuits[14], capacitors[15], and sensors[16] have also been reported in literature. Due to its high electron mobility and compatibility with silicon technologies, it is believed that graphene can replace the highly used silicon.

Intel cofounder, Gordon Moore, predicted in a published paper in 1965, that the number of transistors in a microchip would double every 18-24 months[17]. This trend followed ever since and became known as the More's law with its main driver being the scaling down of transistors width and length, allowing more transistors per chip while maintaining the same power consumption.

The effects of down scaling have brought the industry to a point where the gate length of a transistors has reached sub-20 nm mark. These devices have increased source drain current leakages due to their proximity. Gate oxide thickness has been reduced as well, which in turn increase the gate current leakages. All of these effects increase the off current of devices and boost their power consumption. To go beyond the scaling limits of silicon, novel devices based on a combination of new materials compatible with the already advanced technology of silicon, such as graphene, will be required. As stated prior, graphene is a semi-metal and graphene-based transistors cannot be turned off. A method of creating a band gap in graphene is to cut it into narrow ribbons with less than tens of nanometres which in turn would allow digital applications for this material. On a simpler approach, graphene analogue/RF devices are a possibility as there is no requirement of turning off the device.

2.2 Graphene-based RF devices

Despite its many applications, in this work we will be focused on the use of graphene to support innovative RF devices.

2.2.1 RF devices

Several radio-frequency devices have appeared in literature, where graphene is used due to its outstanding properties, mainly electronics. These range from passive components, capacitors and resonators, to active components, frequency multipliers and RF signal mixers.

The reason why this material sparked interest in the in the radio-frequency community is due to its high charge carrier mobility (200 000 cm^2/Vs), which is the highest carrier mobility of any known material. This value, when compared to other semiconductors, has 100 times more mobility than silicon and 10 times more than the state-of-the-art high mobility group III-V semiconductors (InSb), which is an enabler of higher performance values. Figure 8 shows the comparison between Si MOSFETs and the best III-V HEMTs devices in terms of figures of merit for RF transistors.

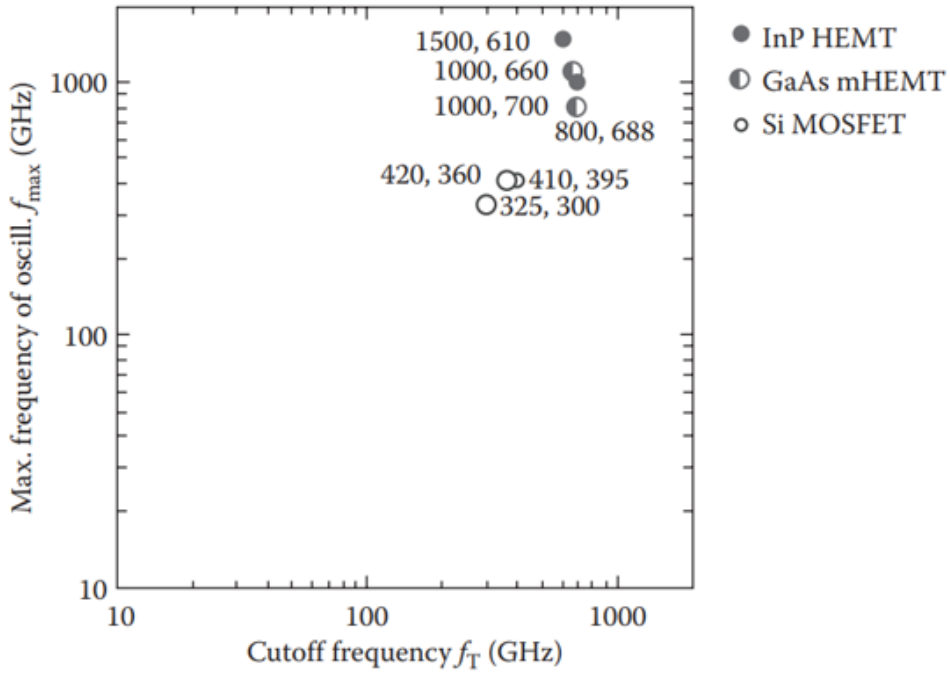

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Figure 8: Maximum frequency of oscillation fmáx versus cut-off frequency fT of Si RF MOSFETs (open circles) and III–V HEMTs (InP HEMTs: full circles, GaAs mHEMTs: half-full circles). The numbers next to the symbols indicate fmáx (first number) and fT (second number) in GHz for the best transistors of each type. Figure adapted from reference [18].

Due to the ambipolar conduction of graphene, non-linear electronics circuits became a possibility[19], which cannot be performed with traditional unipolar devices. In conventional unipolar devices, the majority carrier type in the channel is determined by the doping and cannot be changed after its fabrication. Ambipolar devices can be switched between p- type and n-type conduction by controlling the position of the Fermi level using a gate bias. GFETs biased at its minimum conduction point and superimposing a sinusoidal signal to a dc bias to the gate electrode modulates the carrier type in the channel. Source-drain voltages swing in response to the ac signal applied to the gate and a frequency doubling occurs at the output.

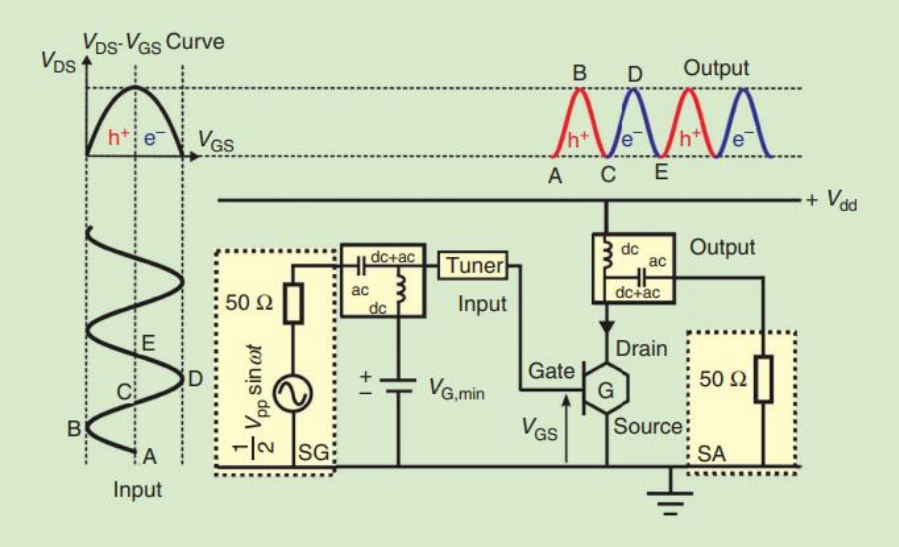

Figure 9: Demonstration circuit for a graphene frequency multiplier operating in a gigahertz frequency range. Figure retrieved from reference [19]

RF mixers are also made possible due to the symmetrical transfer characteristics of the GFETs [14]. The graphene transistor is modulated by two signals, the RF signal and LO signal and the drain source current contains the mixed frequencies. The symmetrical current characteristics of graphene can be expressed as follows:

$$I_D = a_0 + a_1\left(V_G - V_{G,min}\right)^2 + a_2\left(V_G - V_{G,min}\right)^4 + \cdots \quad (1)$$

where $V_{G,min}$ is the gate voltage at the minimum conduction point and a0, a2, a4, . . . are constants. When biased at the minimum conduction of the device, assuming symmetrical transfer characteristics, odd-order intermodulation are supressed, and all the power is coupled to the difference and sum frequencies of even odd terms. Eliminating the odd-order intermodulation products, which are present in unipolar devices, simplifies the circuit.

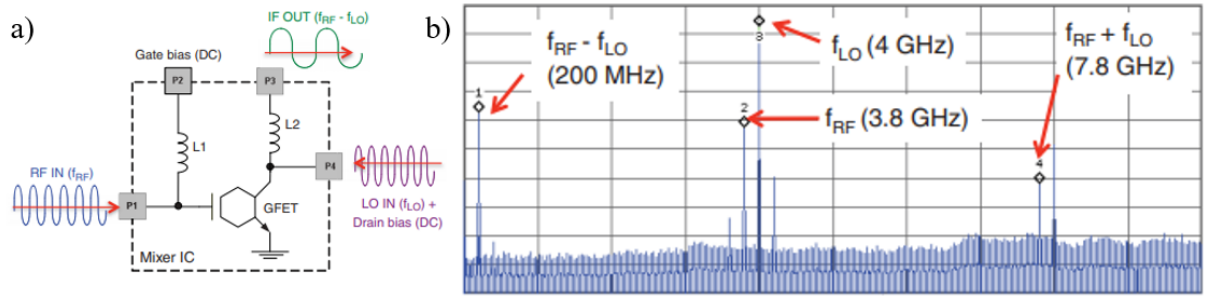

Figure 10: Graphene-based mixer. a) Circuit diagram of a four-port graphene RF frequency mixer. b) Output spectrum of the mixer, between 0 and 10 GHz. Figure adapted from reference [14]

The high carrier mobility and the high current saturation velocity of graphene can potentially allow high operating frequencies as well as low noise devices thus enabling the most attractive analogue applications of GFETs, the low noise amplifier (LNA). Graphene transistor show high current density and excellent electrostatic confinement which increase the conversion efficiency. A graphene Monolithic Microwave Integrated Circuit (MMIC) has been reported in literature [20], working in the Ku band with a small signal power gain of 3.4 dB at 14.3 GHz, and a minimum noise figure of 6.2 dB.

The devices presented previously, all have the same component in common, the transistor.

2.2.2 Graphene-based RF transistors

Graphene-based transistors have been developed ever since its first isolation. The devices first fabricated used the back-gate configuration, which is the most commonly used in physics experiments due to its simplicity, but such configuration is not suited for RF applications. A 300 nm SiO_2 layer on top of the conductive silicon [21], which is used to apply the gate voltage, possesses a low modulation of the channel and large parasitic capacitances.

Top gate graphene field effect transistors developed possess the highest figures of merit reported to date. Several different approaches have been studied for the implementation of these structures. Direct deposition of the dielectric onto graphene through a physical vapor deposition process yields the worst results as the graphene lattice is degraded by the process. Atomic layer deposition requires a functionalization step, prior to the deposition, to enable the deposition of

the dielectric. Amongst all the processes developed, functionalization through metal oxide buffers deposited by evaporation achieve the best results seen in literature. A conjunction of this functionalization step with a T-shape gate allows graphene devices to have cut-off frequencies and maximum oscillating frequencies up to 300 GHz and 200 GHz [13], respectfully.

Other strategies implemented, are through the physical transfer of pre-patterned structures. Although unconventional methods, these achieve the highest cut-off frequencies in literature, 427 GHz[22], as the graphene lattice is not degraded by the fabrication method.

2.2.3 Figures of merit of graphene-based RF transistors

The figures of merit stated previously, cut-off frequency and maximum oscillating frequency, are the two most important ones for GFETs. The cut-off frequency of a transistor is given when the small signal current gain reaches unity and can be written for the intrinsic and extrinsic devices. The intrinsic value only considers parameters that are related to the transistor, while extrinsic also takes into account all the remaining components of the device, the metallic pads and the contacts between metals, which translate into parasitic resistances, inductances and capacitances. The cut-off frequency of graphene field effect transistors is given by:

$$f_{T,int} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{2}$$

$$f_{T,ext} = \frac{g_m}{2\pi\left[(C_{gs} + C_{gd})\left(1 + \frac{R_d + R_s}{R_{ds}}\right) + C_{gd}g_m(R_d + R_s) + C_{pg}\right]} \tag{3}$$

while the maximum oscillating frequency is given by:

$$f_{máx,int} = \frac{g_m}{4\pi C_{gs}} \frac{1}{\sqrt{g_{ds}R_i}} \tag{4}$$

$$f_{máx,ext} = \frac{f_{T,ext}}{2\sqrt{(R_g + R_i + R_s) * g_{ds} + 2\pi f_{T,ext} C_{gd} R_g}} \tag{5}$$

Where g_m is the transconductance in Siemens, C_{gs} and C_{gd} are the gate-source and gate-drain capacitances in Farads, R_d, R_s, R_g, R_i and R_{ds} ($i.e., \frac{1}{g_{ds}}$) are the drain, source, gate,

channel resistance and the dielectric resistance in ohms and C_{pg} is the parasitic gate capacitance in Farads.

2.2.4 Fabrication constraints

GFETs for radio-frequency applications fabricated to date, cannot compete against the established applications. This is due to the fabrication processes that are employed to fabricate these devices. Through the use of the pre-established CMOS technologies, the graphene sheet is degraded, and devices fabricated suffer from high resistances and carrier scattering.

Before the fabrication of graphene devices, graphene itself has to be synthesized. Several methods have been reported in literature and the aim for high quality, single crystal monolayer graphene is far from over. However, centimetre sizes of the intended material have been reported in literature. The high crystallinity of graphene implicates lower resistance as the electrons or holes, depending on the gating, can move longer distances without interruption which translates into higher mobility values. High quality graphene is achieved through mechanically exfoliated graphene, however, this process is not scalable and only sees use in laboratory works. On the other hand, thermal chemical vapor deposition of graphene has been reported to grow the centimetre size sheet, stated prior, and the scalability of the process enables its use in applications.

In the chemical vapor deposition process, the graphene is grown on a catalytic substrate (i.e. Cu, Ni) and afterwards additional processes, etching the metal and transfer to the substrate where the devices will be fabricated, has to be performed. The transfer processes reported to date, each in their own way, introduce defects and impurities to the graphene sheet. Polymer assisted transfer (i.e. PMMA, PDMS) of graphene is one of the most commonly used techniques. However, after the removal of the polymer from the graphene, residues are left behind which increase the resistance of metal contacts made onto it.

The substrate to which the graphene sheets are transferred onto also affect the electronic properties of the graphene devices. High rugosity of the substrate where the graphene sheet sits results in an increase of the carrier scattering. The dangling bonds and carrier traps seen in low quality dielectrics, interact with charge carriers of the graphene and lower their mobility. This

is one of the reasons suspended graphene has such a higher value of carrier mobility than graphene on a SiO_2 substrate. Higher quality dielectrics with low level of rugosity are therefore required to maximize the performance of graphene-based devices.

Dielectric integration onto the graphene sheets is another fabrication process that hinders device performance. As stated before, harsh depositions methods, such as physical vapor deposition (i.e. sputtering) result in the degradation of the graphene lattice. Since the graphene is a monotonical layer, sputtering techniques tend to create tears in the sheet. Several approaches have been developed to replace the PVD of the dielectrics. Evaporation of oxide buffers, such as aluminium which quickly oxidizes into Al_2O_3 when exposed to air, are softer approaches to the dielectric deposition. Although these still introduce defects into the graphene lattice, oxide formed from this technique is of high quality. Other approaches, such as physical transfer of the gate stack and buried gates, have also been researched. These however, are unconventional methods which difficult the scalability of the devices fabricated.

Lastly, contact resistance have also posed a problem in the fabrication of the graphene-based devices. Contact resistances, for radio-frequency applications, should be as low as possible. Resistances in graphene-based devices can come from the graphene transfer process and the fabrication processes implemented on graphene. Approaches such as t-shaped gates can significantly decrease the gate resistance as the area of the gate is higher than the channel length. Buried gates also have an advantage as the gate can be prolonged into the substrate possessing a high width to length ratio thus decreasing the gate resistance.

On the following sections the fabrication issues that can hinder graphene transistor performance will be introduced and discussed.

2.3 Graphene Synthesis

Ever since graphene, a single layer of carbon atoms bonded together in a hexagonal lattice, first appeared, many efforts have been made to develop new processing techniques for efficient synthesis of large-scale graphene. These range from bottom-up approaches (i.e. chemical vapor deposition, epitaxial growth) to top-down approaches (i.e. mechanical or chemical exfoliation).

However, mechanical exfoliation, epitaxial growth and thermal chemical vapor deposition (CVD) are the most commonly used today [23].

2.3.1 Mechanical exfoliation

Exfoliation is simply described as the separation of different layers, in this case graphene, from the bulk graphite. Graphite is composed of several layers of graphene which are bond together by weak Van der Walls forces, making it possible, in theory, to remove such layers by breaking these bonds.

Novoselov *et al* [1] have described a method to isolate a monolayer of graphene from HOPG (Highly Ordered Pyrolytic Graphite) using Scotch tape which in turn earned them a Nobel prize in 2010. The method uses normal forces to separate the two layers and can be described as such. HOPG were dry etched in oxygen plasma to create 5-micron thick mesas. These mesas were then stuck to the photoresist and with scotch tape after baking it, the layers of graphene were peeled off. Once peeled off, the single layers of graphene were released from the photoresist in acetone. This production method of graphene was found to be very reliable and simple, which was later used to produce two-dimensional atomic crystals from other materials.[24] This method of fabrication produces graphene of few layers to single layers with lateral sizes of µm to cm. Although large sizes and unmodified graphene sheets can be produced by his method it lacks when it comes to scaling production only seeing its use in laboratory work.

2.3.2 Thermal decomposition (SiC)

Thermal decomposition of SiC [25], [26] is a simple method which consist in heating the substrate (SiC) to temperatures up to 1500 ºC where the sublimation of silicon occurs which in turn leaves behind a rich carbon surface. C. Berger *et al.*[25] have utilized temperatures from 1240 ºC to 1500 ºC under ultra-high vacuum and achieved graphene with mobilities up to 1100 cm^2/Vs. K. V. Emtsev *et al.* [26] on the other hand, have utilized temperatures of 1650 ºC and pressures of 900 mbar which allows for surface diffusion and subsequently, restructuring

of the surface, creating monolayer graphene films with sizes up to 50 μm and mobilities up to 2000 cm^2/Vs.

2.3.3 Thermal Chemical Vapor Deposition

Monolayer graphene films were first CVD grown in 2009 by Li *et al* [27] using a polycrystalline Cu foil as substrate and a mixture of methane and hydrogen as the gas precursor. The CVD method of growing graphene is considered the most promising due to its simple process and capability of producing large area graphene with high crystalline quality.[28] Centimetre size single crystal graphene have been reported in literature [29] with mobilities up to 3500 $cm^2/V.s$.

The CVD method requires a precursor to transport the carbon to the catalytic substrate, as they can be in the form of solid, liquid or gas. Even though the precursors can be in different forms, they always need to reach the catalytic substrate in the form of gas. A critical parameter in graphene synthesis is that the energy required for the whole process depends on the type of precursor used. The use of precursors with low CH bond energy and catalysts are methods of reducing this energy. Gaseous precursors are the most commonly used in CVD graphene synthesis with hydrocarbons gases such as methane (CH_4) and acetylene (C_2H_2) seeing the most use[23]. As for catalysts, Cu has many advantages when compared to other transition metals which include ease of transfer, economical cost and good control of number of layers.

2.4 Graphene Transfer methods

The CVD graphene growth method is the most commonly used as it can produce high quality graphene over a large area with low economical costs. However, in order to use this graphene in electronic devices, it has to be transferred from the catalytic substrate that it was grown on to the intended surface. These types of processes sometimes require a step of etching the catalytic substrate underneath (i.e. Ni or Cu) which can be done with the use of etching

solvents such as $Fe(NO_3)_3$, $FeCl_3$ or $(NH_4)_2S_2O_8$. The most prominent graphene transfer methods are as follows.

2.4.1 Polymer assisted transfer

Polymer assisted transfer[30], uses a polymer, the most common being PDMS and PMMA, to perform the transfer from the catalytic substrate to the work area. The polymer is coated on top of the graphene and then the catalytic substrate is removed with the assistance of an etchant solution. The polymer is then removed from the graphene after transferring them to the work area. This transfer process can leave some residues attached to the surface after its removal which can introduce some resistance when a metal contact is made.

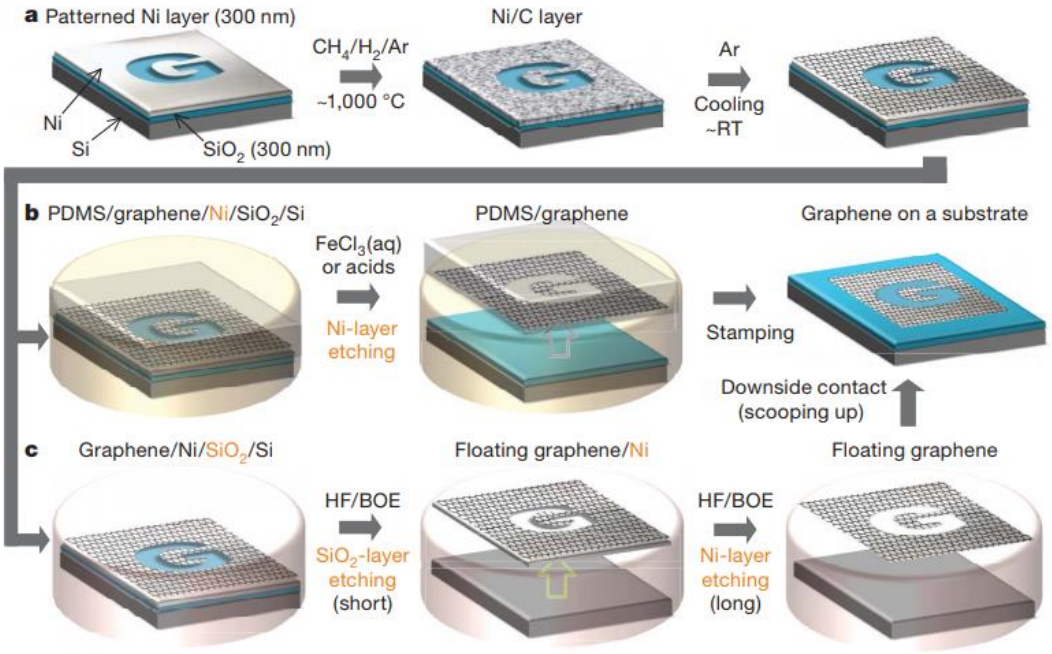

Figure 11: Synthesis and dry transfer process of a graphene film grown by CVD on top of a Ni substrate. a) Synthesis of patterned graphene films on thin nickel layers. b) Etching using FeCl3 (or acids) and transfer of graphene films using a PDMS stamp. c) Etching using BOE or hydrogen fluoride (HF) solution and transfer of graphene films. Figure adapted/reproduced from reference [30]

2.4.2 Roll-to-roll transfer

Roll-to-roll [11], uses two rollers which spin together while applying heat and pressure to the graphene/copper substrate which has been attached with a thermal release tape. The copper is then etched, and the graphene/release tape are ready to be transferred to the work area. This transfer process provides an already scale-up production of graphene on ultra large copper substrates. However, it still suffers from the same problems of the polymer assisted transfer, as one is required for the transfer.

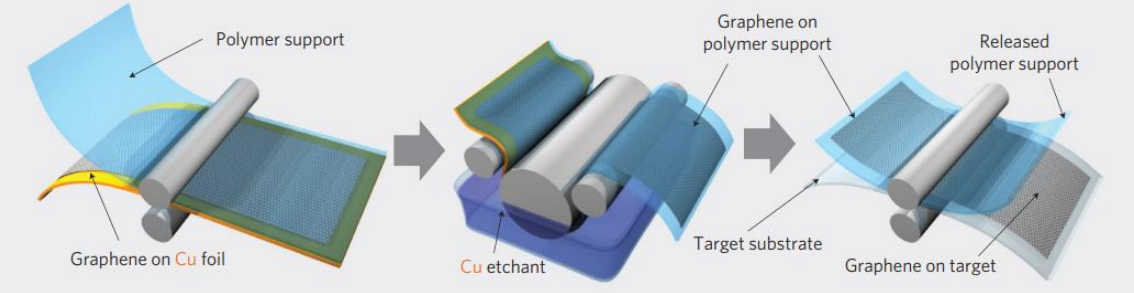

Figure 12: Schematic of the roll-based production of graphene films grown on a copper foil. The polymer is attached to the graphene/copper substrate, followed by the copper etch and finally the release of the graphene from the polymer on to the work area. Figure adapted/reproduced from reference [11]

2.4.3 Bubbling method

The bubbling method [31], [32] consists in the electrochemical delamination of the graphene from the growth substrate. An dc voltage is applied to the graphene, protected with a polymer layer, and through the reduction of water ($2H_2O(l) + 2e^- = H_2(g) + 2OH^-(aq)$), bubbles of hydrogen emerge in the interface between the graphene and the metal which provide a gentle but persistent force. Y. Wang *et al.* [31] used this method to transfer graphene grown in a copper foil and saw small etch of the copper in the process, while L. Gao *et al.* [32] used graphene grown in a platinum foil and due to the platinum inert nature, no etch of the growth substrate was seen. This transfer process has the advantage of reutilization of the catalytic substrate and as a result a lower economical cost.

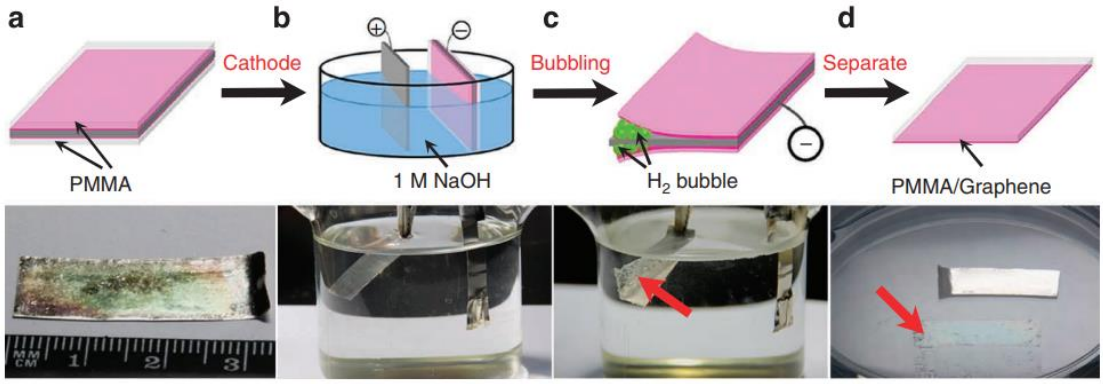

Figure 13: Bubbling transfer method. a) Pt foil with grown graphene covered by a PMMA layer. (b) The PMMA/graphene/Pt in (a) was used as a cathode, and a Pt foil was used as an anode. (c) The PMMA/graphene was gradually separated from the Pt substrate driven by the H2 bubbles produced at the cathode after applying a constant current. (d) The completely separated PMMA/graphene layer and Pt foil after bubbling for tens of seconds. Figure adapted/retrieved from reference [32].

2.5 Direct deposition of the gate dielectric onto graphene

Dielectric integration on graphene devices has been one of the most critical processes in the device fabrication, as standard CMOS technologies introduce significant damages to the graphene lattice. In this section, several approaches for dielectric integration on graphene and subsequently, graphene RF transistors will be presented alongside its performance values.

2.5.1 Physical vapor deposition

Physical Vapor Depositions is a process in which the intended material for deposition is vaporized from a solid or liquid source, transported in the form of vapor through vacuum or low pressure gaseous to the substrate, where it condenses. PVD produces low quality dielectrics and causes damages to the graphene. T. J. Echtermeyer *et al* [33] have utilized mechanically exfoliated graphene flakes to fabricate a top gated field effect device. The device was fabricated on a p-type silicon wafer with a 300 nm SiO_2 as passivation layer and after graphene transfer,

SiO_2 was evaporated onto the surface to serve as gate dielectric. Since the fabrication method enabled a top and back gate configuration, I-V curves, and subsequent carrier mobilities, could be extracted. Electron and hole carrier mobilities changed from 4790 $cm^2/V.s$ and 4780 $cm^2/V.s$ to 710 $cm^2/V.s$ and 530 $cm^2/V.s$, respectfully, after the PVD process.

Z. H. Ni *et al* [34] have utilized Raman spectroscopy to characterize the graphene layer after several types of depositions and concluded that PVD methods introduce significant defects into the graphene. RF sputtering, PLD and e-beam evaporation are all utilized in the research. For comparison, PMMA is spin coated onto the graphene and the Raman spectroscopy shows no significant damages introduced.

These results and the fact that, to the best of the authors knowledge, no articles cite a major breakthrough in the use of PVD to deposit dielectric oxides onto graphene without severely damaging its lattice, excludes it from a potential fabrication method.

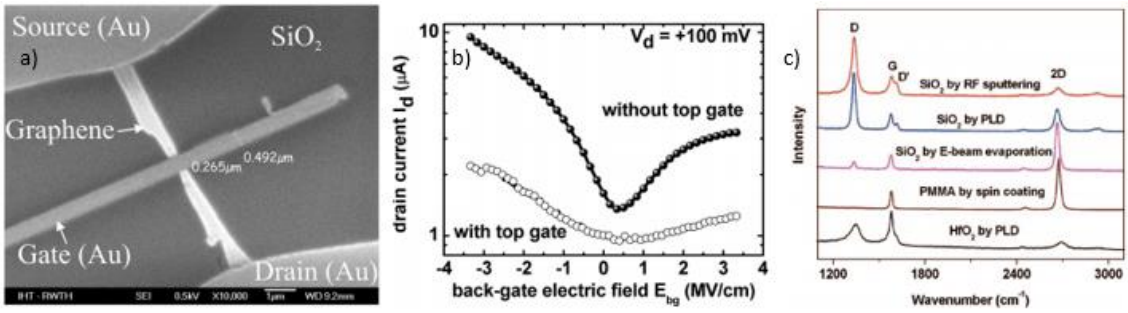

Figure 14: Field effect device and its I-V curves before and after top gate oxide evaporation. Raman spectroscopy of different types of physical depositions of oxide onto graphene. Figures adapted/ retrieve from references [33] and [34].

2.5.2 Atomic layer deposition

ALD is a thin film deposition technique that uses a sequential, self-limiting surface reactions. ALD is able to conformally deposit very thin layers of high-k oxides, making it a useful tool in the semiconductor industry. X. Wang *et al* [35] have demonstrated that ALD of Al_2O_3 yields no deposition on top of pristine graphene (Figure 15) and attributed this to the lack of dangling bonds on the graphene surface. In contrast, the metal oxide is deposited on the graphene edges and the graphene defect sites as these have dangling bonds that the ALD precursors can attach to. For this reason, a functionalization step is needed to grow high-k

dielectric layers on graphene, as it provides intentional nucleation sites on the inert surface of graphene.

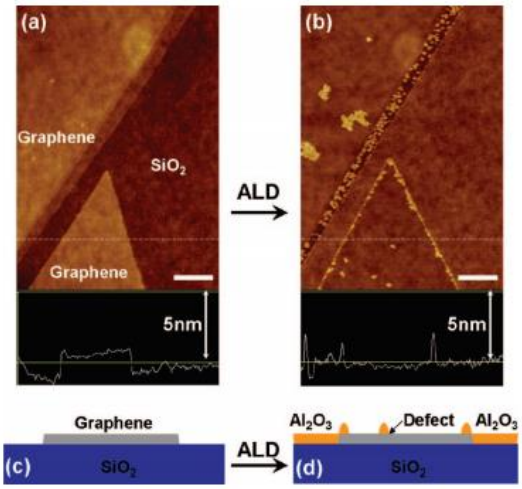

Figure 15: Experimental results of X. Wang *et al.* a) and b) AFM images of the graphene layer. c) and d) Representations of the AFM images. Figures adapted/retrieved from reference [35].

Organic buffer layer:

X. Wan *et al* [35] have proposed, in their work, an intermediate step to deposit Al_2O_3. This step consisted on soaking the chip, with the already transferred graphene layer, on a solution of 3,4,9,10-perylene tetracarboxylic acid (PTCA) for 30 minutes. After rinsing and blow dry, the chip was quickly placed on the ALD chamber. PTCA, after adhering onto the surface, enables the deposition of deposition of aluminum oxide via trimethylaluminum (TMA) precursor, on its carboxylate functional groups. (Figure 16).

Y. M. Lin *et al* [36] have used a functionalization layer consisting of 50 cycles of NO_2-TMA (trimethylaluminum) which enabled an ALD of Al_2O_3 on graphene. The device consisted of e-beam lithography defined Ti/Au (1 nm/50 nm) thin films as the source and drain electrodes, a 12 nm thick Al_2O_3 layer deposited by ALD as the gate insulator, and Pd/Au (10 nm/50 nm) thin film as the top gate. Device characterization of before (through back gate) and after (through top gate) top gate deposition shows that the devices performance suffered due to this deposition. The authors attribute this current and mobility degradations to charged impurity scattering associated with the NO_2 functionalization layer and interface phonon scattering in

the oxide. However, these devices manage to achieve a cut-off frequency of 4 GHz after de-embedding.

Although ALD is made possible with this technique, there is a significant reduction in transconductance after the deposition, which does not allow for high performance of such devices.

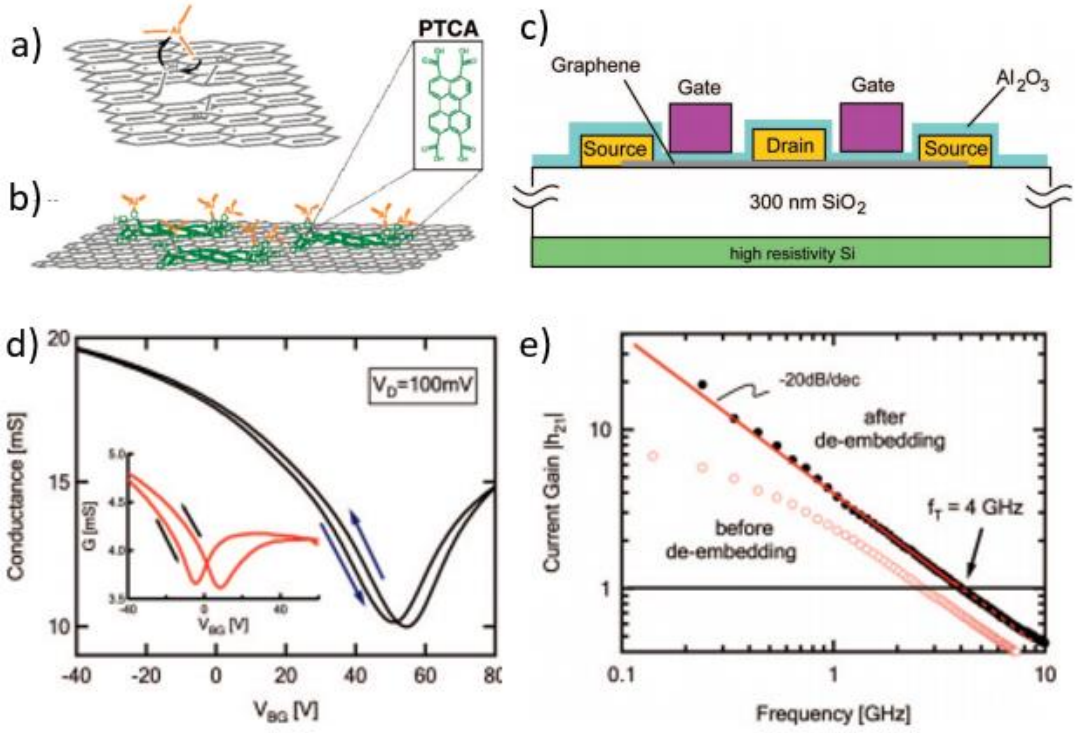

Figure 16: Molecular layer functionalization aid on depositing high-k dielectrics on graphene. a) Atomic layer deposition of aluminum oxide via trimethylaluminum (TMA) precursor on graphene containing a defect site. b) Atomic layer deposition of aluminum oxide via trimethylaluminum (TMA) precursor on perylene tetracarboxylic acid (PTCA)-coated graphene. c) Schematic cross section of the graphene transistor. d) I-V curves before and after top gate deposition. Inset shows the transfer curve after the ALD of the top gate dielectric. e) The current gain h21 calculated from the measured S parameters as a function of frequency. Figures adapted/retrieved from references [35] and [36].

Polymer buffer layer:

Y. M. Lin *et al.* [37] have utilized a thin layer of a polymer to provide functional groups for the ALD molecules and deposit a gate stack on top of the graphene.

The graphene used was epitaxially grown on a SiC substrate and the source-drain electrodes of were formed by e-beam lithography followed by lift-off and consisted of Ti/Pd/Au (1 nm/ 20 nm/ 40 nm). The excess graphene was etched with oxygen plasma and PMMA as the etch mask. A 10 nm layer of *polyhydroxystyrene* was spin coated followed by a 10 nm deposition of HfO_2 by ALD. Lastly, the top gate was formed using the same method and the same materials

as the source-drain electrodes. A device with channel width of 2 μm and channel length of 210 nm achieved a cut-off frequency of 210 GHz with a peak scaled transconductance of 0.32 mS/μm.

Epitaxially grown graphene has the advantage of not requiring a transfer process as the SiC substrate is semi-insulating. However, the morphology of such graphene usually contains steps which can hinder the devices performance. For this reason, scaling of this fabrication method is unsure as the device's performance would be dependent of its position on the wafer (Figure 17).

Another setback of this fabrication method is the use of the polymer layer itself. Usually polymers have lower k than the oxides and by placing these at the interface of the top gate and the channel, the gating effect is reduced which lowers the device performance.

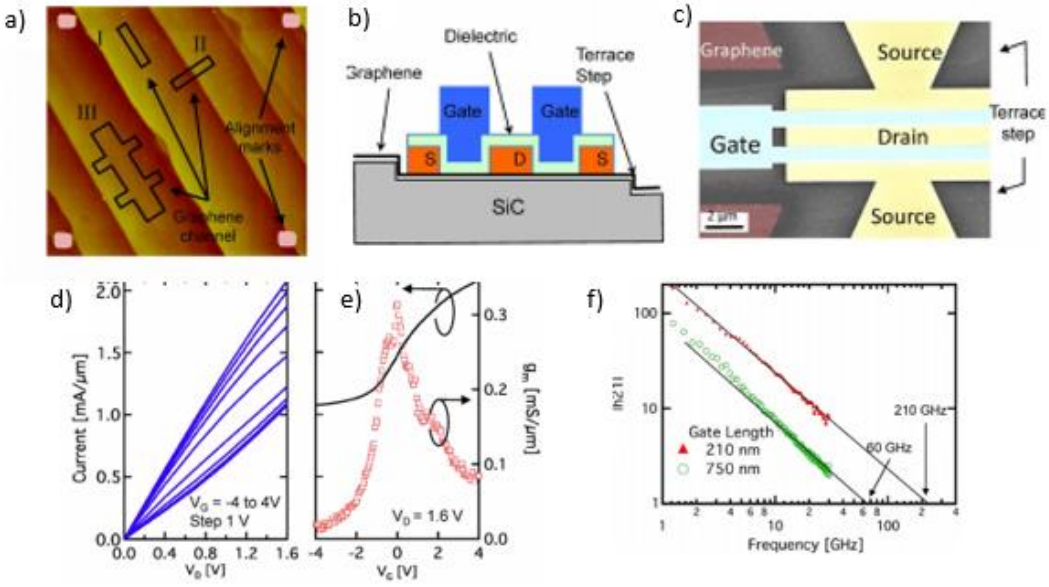

Figure 17: Transistor with a polymer buffer layer. a) AFM image of epitaxial graphene grown on SiC, showing the terrace structure and steps. b) Schematic cross-section of a top-gated GFET. c) (false colour) SEM image of a dual channel graphene FET where both channels are located within a single terrace. d) and e) Measured transfer characteristics of graphene FETs with 210 nm of channel length. f) Measured current gain |h21| of GFETs. Figures adapted/retrieved from reference [37].

Buffer layer of metal oxides:

Another strategy for the integration of ALD is through the use of a metal oxide layer. Y. Wu *et al.* [38] have deposited a thin aluminum layer (1-2 nm) before the ALD of Al_2O_3. This thin layer quickly oxidizes into Al_2O_3 and provides nucleation sites for the ALD process.

CVD grown graphene on a copper foil was transferred to a diamond like carbon substrate and through e-beam lithography the contacts for source, drain and gate were formed while the excess graphene was removed with plasma etching. Pd/Au form the source drain metal stack. Through electron beam evaporation a thin layer of Al is deposited and oxidized before the ALD of Al_2O_3. The devices fabricated with channel lengths of 40 nm achieved cut-off frequencies of 300 GHz and a maximum oscillation frequency of 20 GHz. Although there are no values of transconductance for these particular devices, the authors report that for a device with a channel length of 650 nm its transconductance is 0.038 mS/μm.

Although a huge leap, from previous reported works at the time, in terms of maximum oscillating frequency, this value still falls short of the cut-of frequency of the device. As the maximum oscillating frequency does not represent intrinsic performance and its largely affected by extrinsic components and device layout, it can be improved by reducing gate resistance and improved internal conductance.

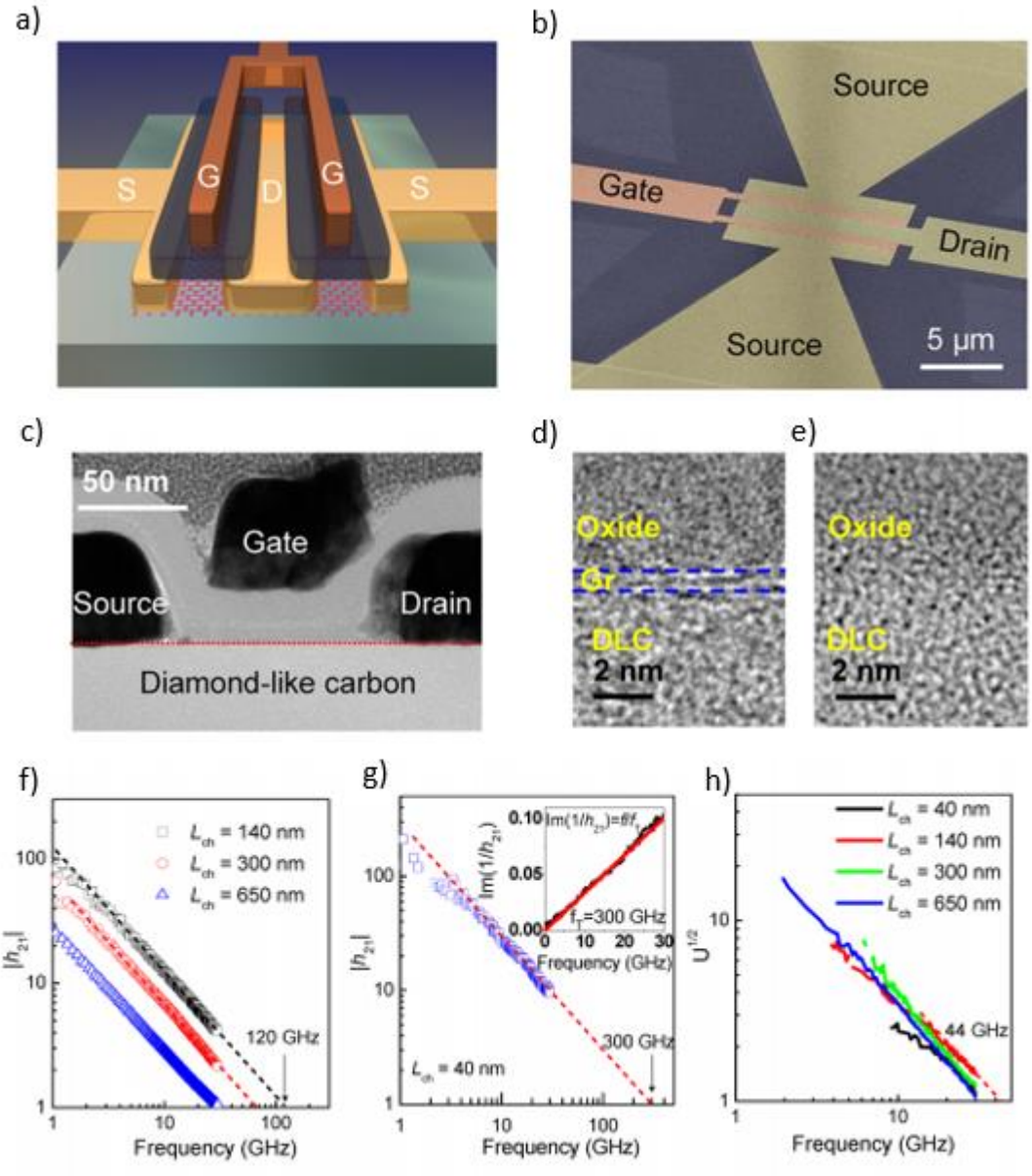

Figure 18: Schematic and electron images and RF characterization of graphene transistors. a) Schematic view of a top-gated graphene RF transistor on a DLC substrate. b) SEM image of the RF device. c) Cross-section TEM images of the transistor. d) and e) the high-resolution TEM image of the channel region of an active device and an open device where graphene is etched away, respectively. f) Small-signal current gain |h21| versus frequency for devices with 140, 300 and 650 nm. g) Small-signal current gain |h21| versus frequency for the 40 nm device with a peak fT of 300 GHz, consistent with the value derived from Gummel's method shown in the inset. h) Mason's unilateral gain versus frequency for the above four devices, with a peak fmáx of 44 GHz obtained from the 140 nm device Figures adapted/retrieved from reference [38].

2.5.3 T-shaped gate

The use of a T-shaped gate is a common approach to ensure a low gate resistance with a small channel length, which are essential for high speed devices[39]. Through the use of multilayer photoresist (e.g. ZEP/PMGI/ZEP) and electron beam lithography with the modulation of the e-beam exposure doses, the intended layers of the multi-layered photoresist film are exposed and developed, thus achieving the t-shape.

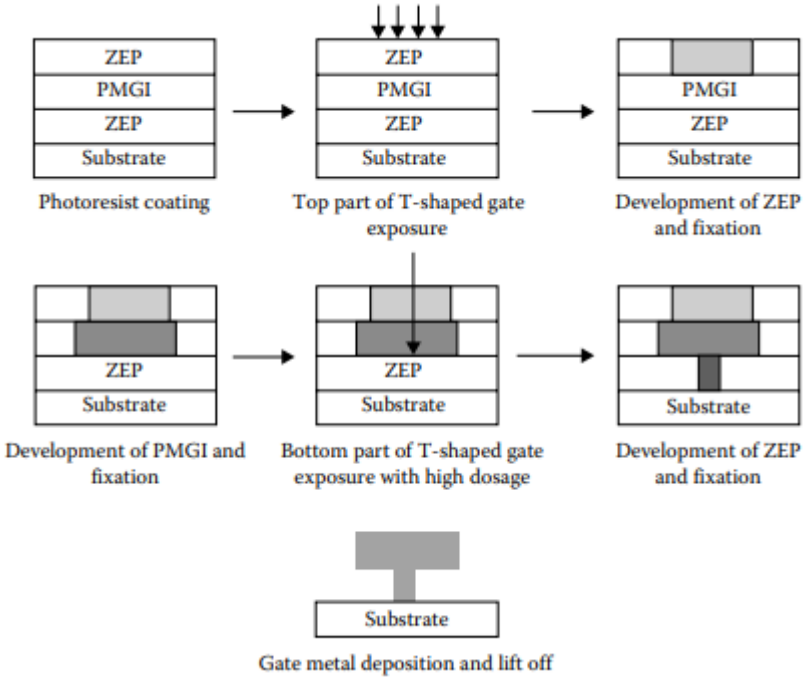

Figure 19: Electron beam lithography process flow of T-shaped gate. Figure adapted/retrieved from reference. [39].

Z. H. Feng *et al.* [40] have utilized these T-shaped gates to fabricate their graphene transistors. Monolayer graphene was synthesised with thermal decomposition of a SiC substrate followed by a thin film deposition of gold (30 nm). This film is deposited with the intention of creating a better ohmic contact between the metal and the graphene. Having a step which involves the use of photoresist or PMMA on top of the graphene creates organic residues which are hard to remove and causes the resistance of the device to increase. The tri-layer photoresist film is patterned through e-beam lithography and the gold is removed with a solution of KI : I2. A thin layer of aluminium (2 nm) is deposited and left exposed to air to self-oxidized and create the gate dielectric of Al_2O_3. Aluminium (180 nm) is lastly deposited to create the gate metallization followed by a lift off process of the tri-layer photoresist.

Fabricated devices with gate length of 100 nm and width of 8*2 μm (double finger set-up) had cut off frequencies of 93 GHz and fmax of 105 GHz while the transconductance achieved was 0.71 mS/μm.

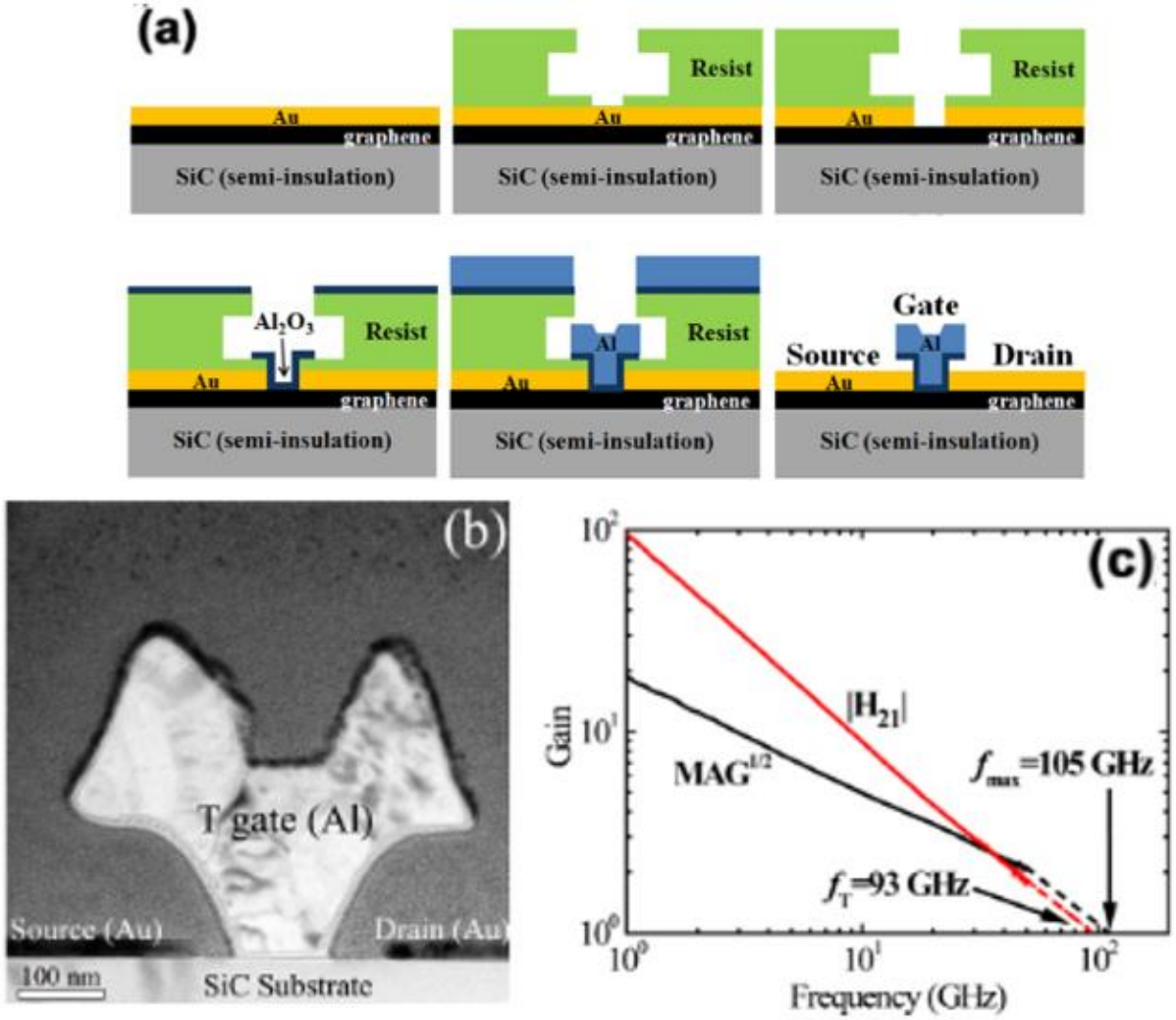

Figure 20: Graphene transistor self-aligned T-shaped gate on a SiC substrate. a) Process flow of the fabricated transistors. b) TEM cross section image of the T-shaped gate. c) Small-signal current gain |H21| and maximum available gain (MAG) of a 100 nm gate length GFET. Figures adapted/retrieved from reference [40].

Utilizing the same methodology, Y. Wu *et al.* [13] have produced devices with better RF characteristics. Exchanging graphene grown by thermal decomposition of SiC for graphene grown by CVD on a copper foil, a smaller gate length, a higher dielectric thickness (8 nm of Al_2O_3) and a thicker metal gate (50 nm Ti/450 nm Au), the group achieved devices with fT of 255 GHz and fmáx of 200 GHz, the highest reported to date for a graphene FET.

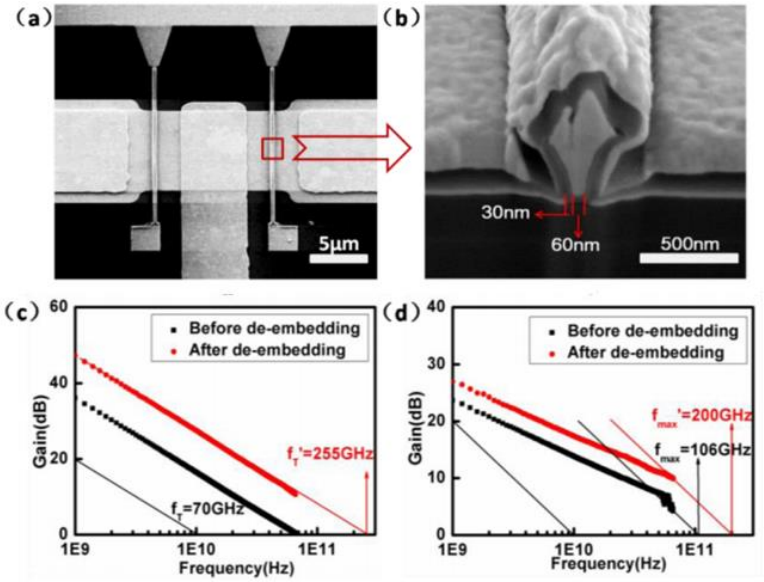

Figure 21: Graphene transistor with self-aligned T-shape gate on a silicon/ silicon dioxide substrate. a) SEM image of the fabricated GFET. b) Cross-section FIB image of the fabricated GFET. c) Measured current gain |h21| of the G-FET before and after de-embedding. d) Measured unilateral gain (U) of the G-FET before and after de-embedding. Figures adapted/retrieved from reference [13].

2.6 Physical assembly of nanostructures

Although many advancements have been made in dielectric integration of top gated graphene field effect transistors, these still affect its structure and hold back the true potential of the material. A whole new approach has been presented in literature where the gate dielectric is physically transferred onto the graphene sheet. With this new approach, it is possible to preserve the graphene properties while also obtaining high quality dielectrics. Due to the fact that the dielectric is grown away from the final structure, it can be fabricated in conditions that otherwise would be damaging to the graphene (i.e. temperature, pressure…), and allow for the integration of materials that otherwise would be impossible to use through standard CMOS technologies. L. Liao *et al*. [41] have physically transferred aluminum oxide nanoribbons grown through physical vapor transport at 1400 ºC onto mechanically exfoliated graphene. Devices fabricated have shown mobilities up to 23600 cm^2/V.s, the highest reported to date for top gated graphene field effect transistors. This stems from the fact that mechanically exfoliated

graphene, the method that best preserves the graphene quality, and high quality Al_2O_3 present the best defect free structures.

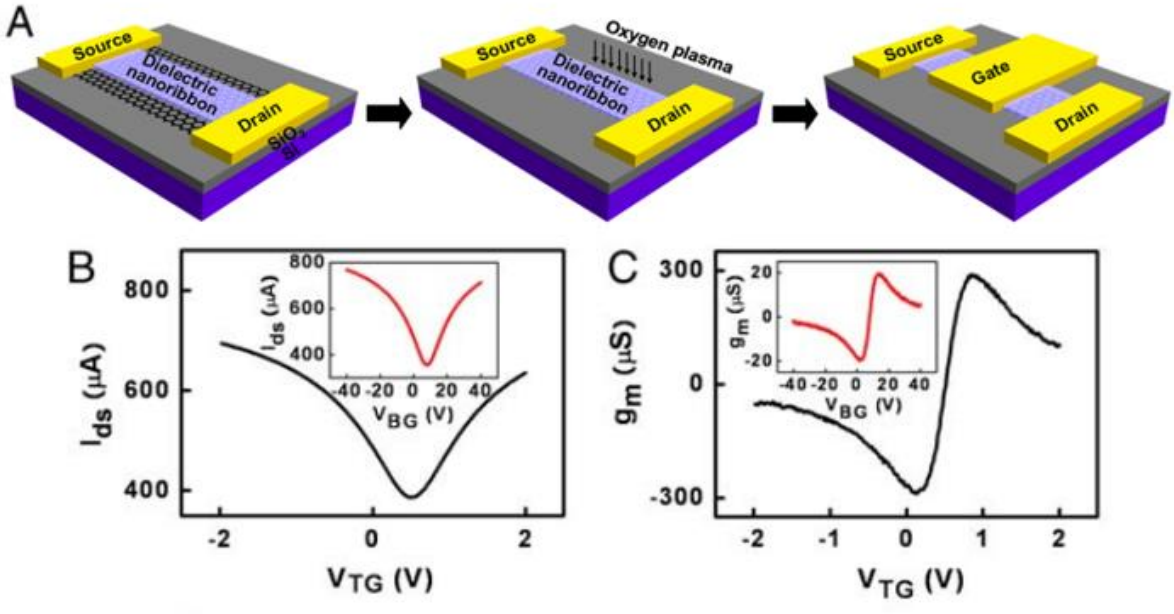

Figure 22: Top-gated graphene transistors with high-κ oxide nanoribbons as gate dielectrics. a) Schematic of fabrication process flow. b) Transfer characteristics for the device using top and back gate (Inset). c) Transconductance values as a function of top gate voltage. Inset shows transconductance values as a function of back gate voltage. Figure adapted/retrieved from reference [41].

L. Liao has gone on to experiment with other nanostructures for physical transfer besides nanoribbons, which include core-shell nanowires[5], [42] and gate stacks[22].

2.6.1 Graphene transistor with a self-aligned core-shell nanowire gate

L. Liao *et al.* [5] have synthesized Co_2Si nanowires, with a vapor transport method in a CVD furnace and coated it with a 5 nm thick shell of Al_2O_3 through an ALD process. These were then physically dry-transferred onto mechanically exfoliated graphene on top of 300 nm thick layer of thermal silicon dioxide. Source, drain and gate external electrodes were patterned by electron-beam lithography, buffered oxide etching to remove the Al_2O_3 shell and expose the Co_2Si core, and a metal stack of titanium (70 nm) and gold (50 nm). A final 10 nm thick layer of platinum was deposited on the graphene channel and over the nanowire as the self-aligned

source-drain contacts. Fabricated devices with channel lengths (i.e. wire diameter) of 144 nm, 182 nm and 210 nm achieved intrinsic cut-off frequencies of 300 GHz, 168 GHz and 125 GHz while extrinsic cut-off frequencies are below 2.3 GHz, and the transconductance measured on an unspecified device achieved a peak of 1.27 mS/μm. The discrepancy between the intrinsic and extrinsic cut-off frequencies is attributed, by the author, to be due to the large ratio between the parasitic and gate capacitances. A thicker silicon dioxide layer and smaller pad size are two methods found by the author to improve this discrepancy, however, the improved fabricated devices only reached an extrinsic cut-off frequency of 4.6 GHz.

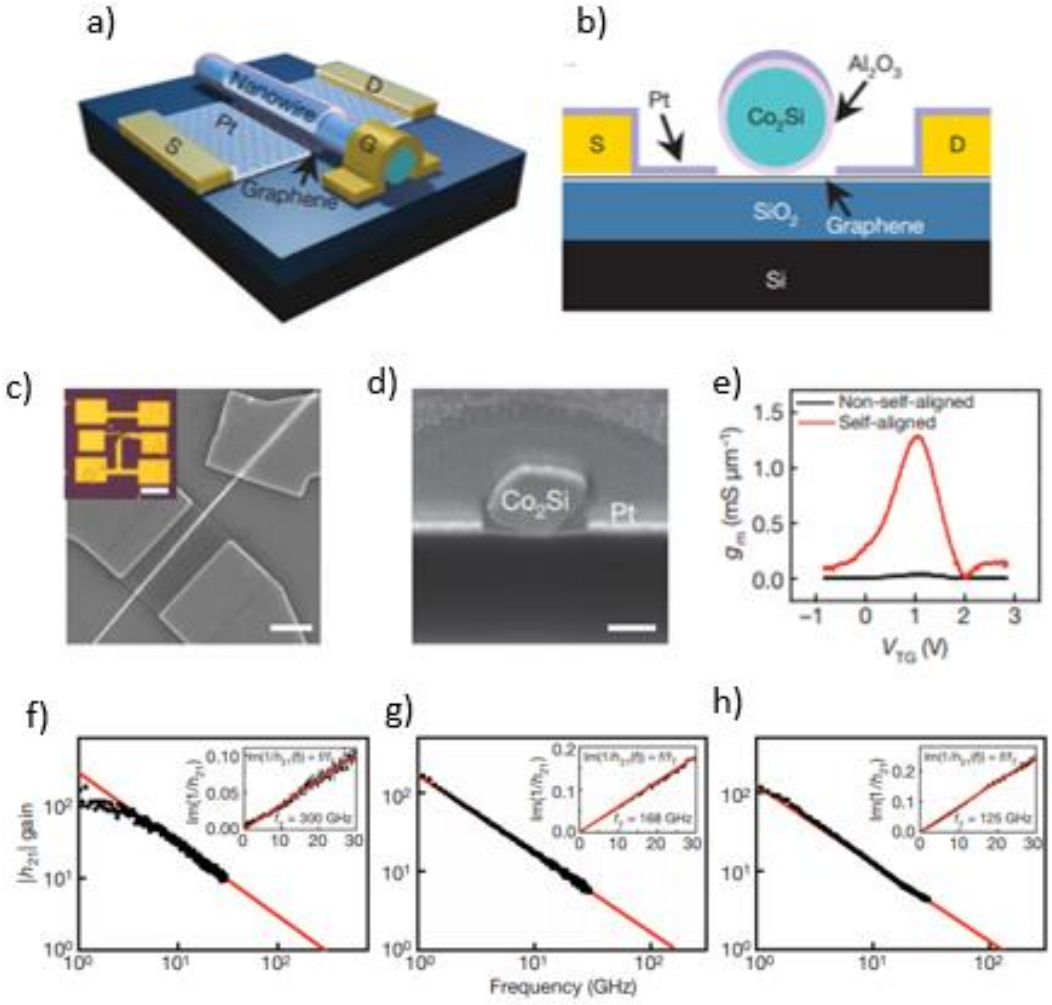

Figure 23: Graphene transistor with self-aligned core-shell nanowire gate. a) Birds eye view schematic of the device. b) Cross section schematic of the device. c) SEM image of the device. Inset, an optical microscope image of the overall device. e) Transconductance values, before (black) and after (red), the self-aligned process. f), g) and h) Measured small-signal current gain |h21| as a function of frequency for devices with gate length of 144 nm, 182 nm and 210 nm, respectfully. Figures adapted/retrieved from reference [5].

In an attempt to up-scale the process and at the same time increase the extrinsic cut-off frequency of the devices with the purpose of creating RF circuits, L. Liao *et al.* [43] exchanged the high resistivity silicon with silicon dioxide for a glass substrate and employed a dielectrophoretic assembled process for the nanowires. Mechanically exfoliated graphene is not suited for large production of devices, so CVD-grown graphene is used. As the quality of graphene diminishes, so its intrinsic cut-off frequency, reaching 72 GHz for a device with a channel length of 170 nm, however, the extrinsic cut-off frequency achieved is 55 GHz. The glass substrate does not dissipate energy through it and for this reason, the parasitic gate capacitance is severely reduced, when compared with the silicon with silicon dioxide devices, allowing for high extrinsic cut-off frequencies.

Another difference of this fabrication process from the aforementioned is the graphene patterning. Previously, the nanowires were assembled onto the mechanically exfoliated graphene, but on this process the graphene is first patterned between the electrodes and only then are the nanowires placed. Although not explicit in the text, the graphene patterned most likely used some sort of resist that can introduce some defects into the lattice and leave behind some residues upon removal, which can lower the device performance. This performance decrease is seen in the devices transconductance which, when compared to the 1.27 mS/μm of the previous, lacks as it only achieves 0.36 mS/μm.

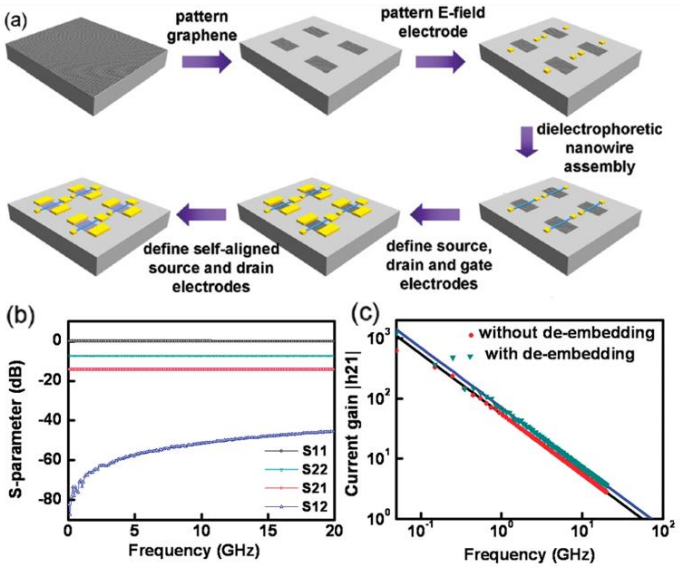

Figure 24: Graphene transistor with self-aligned core-shell nanowire gate on glass. a) Fabrication process of the device. b) Measured S-parameters of the fabricated devices. c) Measured small-signal current gain |h21| as a function of frequency, before and after de-embedding. Figures adapted/retrieved from reference [43].

2.6.2 Graphene transistors with triangular shaped GaN nanowires

Triangular shaped GaN nanowires were also experimented with[42]. The highly doped GaN nanowires formed a Schottky-like barrier at the interface with the graphene and the depletion layer in the nanowire functioning as semi-high k dielectric, creating an insulation between the gate and the channel. Devices with channel length of 100 nm and widths of 2 μm showed exceptional DC characteristics with transconductance values of 2.3 mS/μm. The intrinsic cut-off frequency of a graphene transistor can be calculated using the following formula[44]:

$$f_{T,intrinsic} = \frac{g_m}{2\pi C_g} \tag{6}$$

Where the g_m is the maximum transconductance, and C_g is the gate capacitance. For this particular device, the intrinsic calculated cut-off frequency is 840 GHz. The author goes on to plot the intrinsic cut-off frequency relative to the channel length and reaches the conclusion that cut-off frequencies exceeding the 1 THz can be achieved with sub-70 nm channel length devices. It is worth noting that this study was conducted not taking into account the limitations of gate delay. In order to enable these types of results, nanowire resistance and contact resistance between the metal and nanowire have to be reduced as much as possible. This theoretical experiment serves once again to prove the potential of graphene devices.

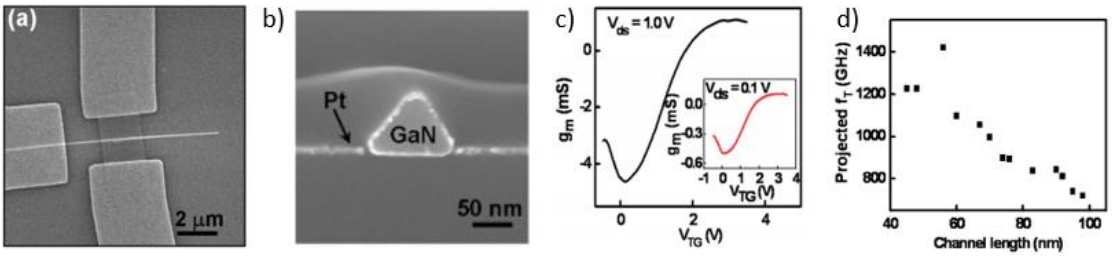

Figure 25: Graphene transistor with self-aligned triangular shaped nanowire gate. a) SEM image of the device. b) SEM cross-section image of the device. c) Transconductance as a function of top gate voltage for different Vds. d) Projected f_T values for different channel lengths. Figures retrieved/adapted from reference [42].

2.6.3 Graphene transistors with transferred gate stacks

The methodology described previously for the device fabrication, although functional, is a very demanding approach due to the requirement of unconventional nanowire-assembly processes. A different approach has been taken, one that consists in the physical assemble of a previously patterned gate stack.[22] The gate stack, consisting of Al_2O_3/Ti/Au, is deposited on top of 50 nm of Au on a silicon/silicon dioxide substrate by standard atomic layer deposition (ALD), lithography, and reactive ion etching (RIE) processes. The 50 nm gold layer has poor adhesion to the silicon dioxide layer and for that reason is a good candidate for a peeling process. A final ALD process followed by RIE leaves the sidewall of the gate with Al_2O_3. This gate stack is then peeled off the silicon dioxide substrate, the Au layer etched and finally transferred onto previously patterned CVD-grown graphene with the assistance of thermal release tape. The thermal release tape is removed with a acetone and the external contacts of the device are patterned followed by the final thin layer of Pd/Au (5 nm/10 nm) across the gate stack to complete the self-aligned process.

A fabricated device with channel length of 67 nm achieved a cut-off frequency 427 GHz, the highest reported cut-off frequency so far, and a transconductance value of 1.33 mS/μm. No particular value is given for this device in terms of fmax, however, for a device with channel length of 220 nm, the cut-off frequency value is 57 GHz, the fmax value is 29 GHz and its transconductance is 0.49 mS/μm.

The reason that these devices possess such a high fmax values, when compared to the previous physically transferred devices, is due to the fact that the fmax scales with the cut-off frequency, gate resistance and source-drain conductance. The author goes on to state that in order to increase this value of the devices, the quality of graphene should be higher while increasing the source-drain current saturation and decreasing the gate resistance.

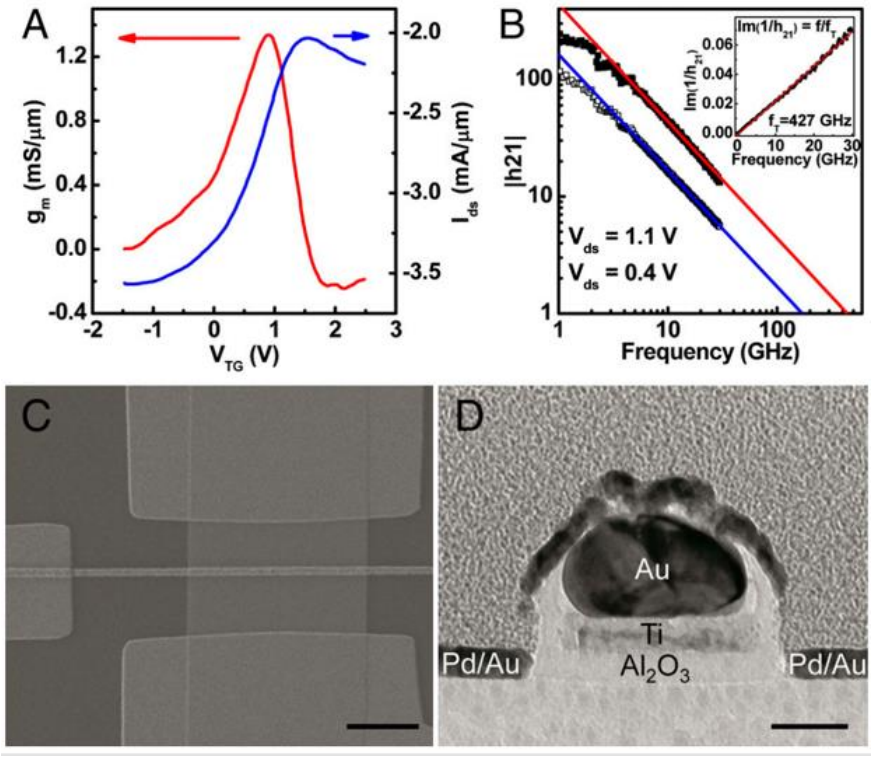

Figure 26: Self-aligned graphene transistors with transferred gate stacks. a) The transfer characteristics and corresponding transconductance for the 67-nm channel-length self-aligned peeled graphene device. b) Measured small-signal current gain |h21| of the 67 nm channel device as a function of frequency for Vds = 1.1 V (red) and Vds = 0.4 V (blue). c) SEM image of a graphene transistor with transferred gate stack. d) Cross-sectional TEM image of the device. Figures retrieved/adapted from reference [22].

2.7 CMOS back-end-of-the-line approach

The Damascene process, pioneered by IBM in the 1990's, is now a well-established methodology for chips interconnects made of copper[45]. The additive process consists in the first etch of the substrate, followed by the metal deposition, copper by electroplating in the case of chip interconnects, and lastly chemical-mechanical planarization to remove the excess metal.

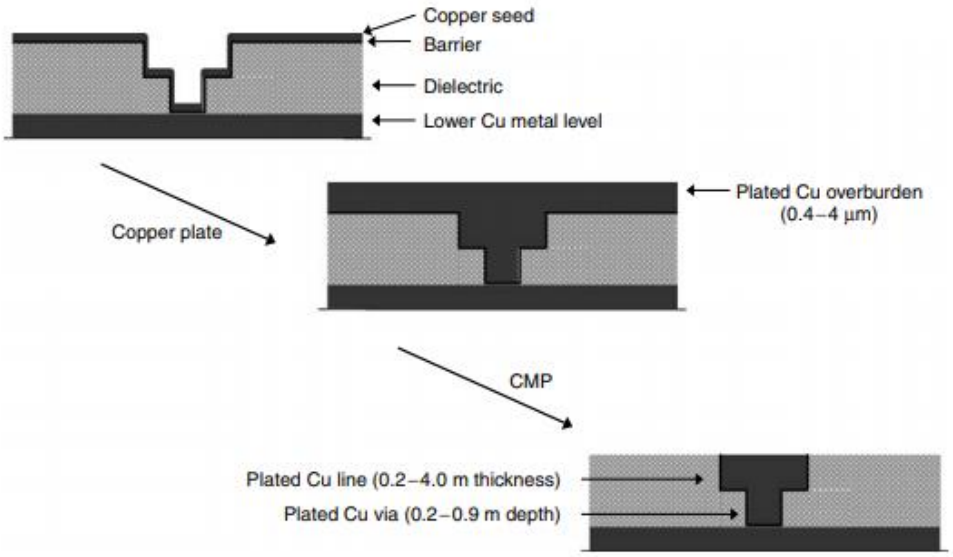

Figure 27: Damascene process flow for chips interconnects made of copper. Figure adapted/retrieved from reference [46].

H. Lyu et al. [47] have utilized the Damascene process to first fabricate the devices pads and lastly transfer the CVD-grown graphene. This fabrication methodology allows for a high depth-to-width ratio and in turn a small gate resistance. By having the graphene placed last on the substrate, fewer process steps are made on top of the material which in turn helps to preserve the graphene properties and achieve higher performances. The CMP process is also beneficial as it guarantees the flatness of the wafer, necessary for a successful graphene transfer process.

An α-Si hard mask of 100 nm was patterned through e-Beam lithography on top of a 5 μm thick layer of PECVD SiO_2. The high selectivity of the reactive ion etching to the SiO_2 used to etch, allows for a high depth-to-width ratio of the buried gates. Source-drain pads and interconnects of tungsten were defined, after the removal of the α-Si, through stepper lithography, followed by CMP to remove the excess tungsten. The gate dielectric of HfO_2 was deposited by ALD with a thickness of 2 nm and the excess was removed, after stepper lithography, with inductively coupled plasma (ICP). Graphene synthesized on Pt foils and transferred by bubbling method was patterned by contact mode contact lithography and the excess graphene removed with oxygen plasma. Source-drain contacts of 40 nm of Pt were lastly patterned with e-Beam lithography and a lift-off process.

Devices fabricated with channel lengths of 200 nm achieved cut-off frequencies of 35.4 GHz and maximum oscillating frequencies of 50 GHz with gate resistances as low as 5 Ω,

even though there was no self-aligned process and the authors reported ungated regions with lengths of 200 nm. Transconductance values, although for a device with channel length of 400 nm, are 0.47 mS/μm.

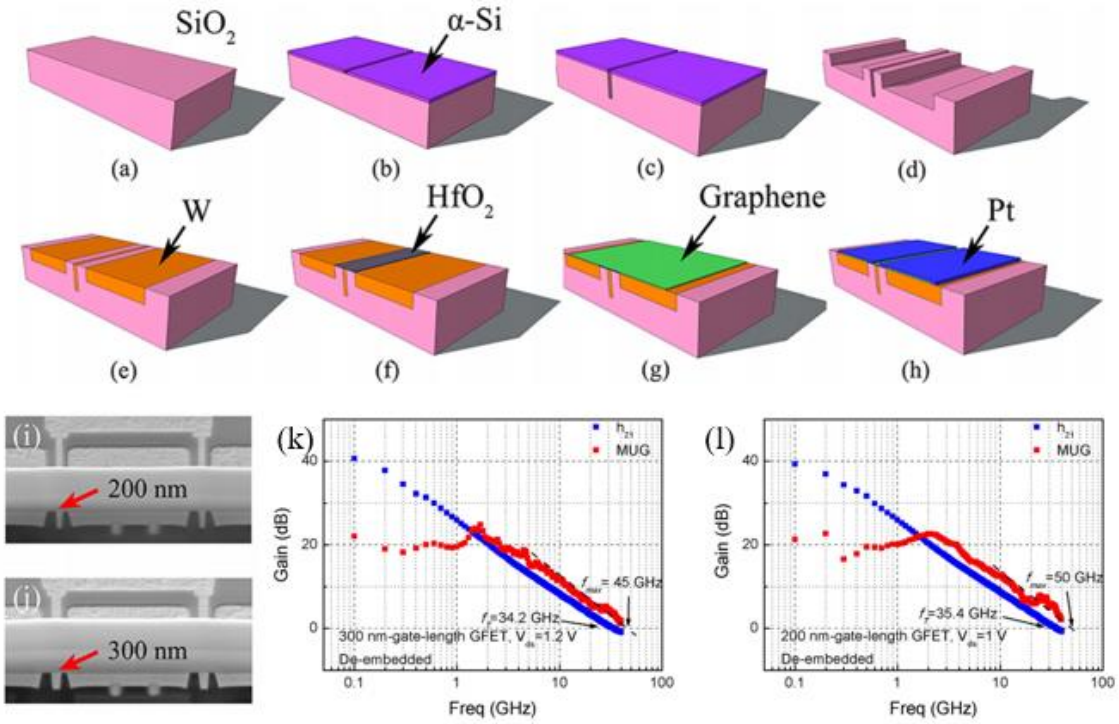

Figure 28: – Buried gate graphene field effect transistor. a) – h) Fabrication schematic of G-FET. i) and j) Cross section SEM images of G-FETs with 200 and 300 nm, respectfully. k) and l) Measured current gain |h21| of G-FETs i) and j). Figures adapted/retrieved from reference [47].

Table 1: Graphene-based field-effect transistors for radio-frequency applications demonstrated in literature

Reference	Graphene Synthesis	f_T (GHz)	Channel length (nm)	Scaled Transconductance (mS/ μ m)	$f_{máx}$ (GHz)	Gate integration
[5]	Mechanical Exfoliation	300	144	1.27	---	Physical transfer of core-shell nanowires
[42]	Mechanical Exfoliation	800-1400	45-100	2.3	---	
[22]	CVD on copper foil	427	67	1.33	---	Physical transfer of gate stacks
		57	220	0.49	29	
[37]	Epitaxial Graphene	210	210	0.32	---	Top-gated devices with dielectric deposition assisted with metal oxide buffer
[13]	CVD on copper foil	255	60	0.59	200	
[40]	Epitaxial Graphene	96	100	0.71	105	
[38]	CVD on copper foil	300	40	---	30	
		30	650	0.038	30	
	Epitaxial Graphene	350	40	---	20	
		30	650	0.045	30	

[47]	CVD on Pt foils	35.4	200	*0.47	50	Buried gate

3 DEVICE DESIGN AND MODELLING

In this chapter, the several methods of graphene transistors fabrication in literature, already discussed previously, will be once more analysed to understand what are compatible with the fabrication techniques available at INL. Once a fabrication process is chosen, modelling of the device will follow. A model of an RF graphene field effect transistor will be selected and configured to match the proposed geometry. Lastly, the physical parameters of the device will be modelled and analysed to design a physical layout that provides a frequency response, at least, up to 8 GHz.

3.1 Introduction

Device design is easier performed with an already established fabrication process, instead of a ground up structuring. The device´s fabricated previously at INL were liquid gate based and back gate configuration graphene transistors.

Liquid gate devices are currently used in biosensing applications [48], [49] while back gate configuration devices serve the purpose of characterization of graphene sheets, providing its carrier mobilities and resistance. Both of these devices follow the fabrication methodology of passive-first active-last inverted process, without the damascene process, where the graphene is placed on the wafer after the patterning of the electrodes, allowing fewer processes to be made on top of the graphene sheet. Although these fabrication methods excel in their applications, these cannot be used for radio-frequency applications. Liquid gate transistors are optimized for the functionalization of the graphene sheet for a specific biomarker and back gate configuration does not allow the control of a single device as the gate voltage is applied to all the devices in the wafer. For these reasons, a new fabrication methodology has to be adopted.

3.2 Transistor proposal

From literature review, already presented in the previous chapter, several promising methods were found available. However, these have to be compatible with fabrication processes already existing and available at INL during this work.

Although several different types of graphene synthesis were presented in the last chapter, many of these are not compatible. At INL, at the moment, the available graphene synthesis is performed through thermal chemical vapor deposition and transfer through a polymer assisted process. This method provides continuous large area monolayer graphene with small amounts of defects introduced to the sheet and is the best suited for electronic devices.

In terms of dielectric integration, it was shown in the last chapter that physical vapor deposition of dielectrics severely damages the graphene sheet, making it unviable for device fabrication, while atomic layer deposition cannot be used without a functionalization step. Utilizing a buffer layer with metal oxides and a T-shaped gate provides the best results seen in literature for radio-frequency graphene transistors, however, both of these methods are not compatible. To the best of the authors knowledge, there are no reports of T-shaped gates being fabricated at INL. These are complex structures which require deep understanding of the e-beam lithography and thus not easy to manufacture. Several studies of metal deposition onto graphene with the existing machines at INL were performed to best assess the damage caused to the sheet by each deposition process. A layer of AlSiCu and aluminium were both deposited by a sputter deposition from different machines onto graphene. Raman spectroscopy, before the deposition and after the metal removal, shows that graphene is severely damaged by the process, discarding the process altogether. The devices presented in literature with metal oxides as a buffer layer were deposited through e-beam evaporation which causes minimal degradation of the graphene, and since this process does not exist at INL, a different method has to be chosen.

The passive-first active-last inverted process and the physical transfer of nanostructures are both complex fabrications methods, each in their own way, but in theory compatible with INL processes. However, physical transfer of nanowires is more appealing as the devices produced have better performance values.

A physical transfer process of core-shell nanowires was the chosen fabrication method to be implemented. The intended fabrication method is based on the work from L. Liao et. al [5]. Nanowires available are electrochemically grown nickel nanowires on an anodized aluminium oxide template, in contrast to the Co_2Si fabricated by vapor transport. As for the gate dielectric (i.e. nanowire shell), nickel oxide, the natural oxide of nickel, silicon dioxide deposited by PECVD, and aluminium oxide deposited by ALD are the available options. As for the metal connections, several different processes and materials can be chosen, that range from lift-off assisted processes to physical etches of materials (e.g., ion milling).

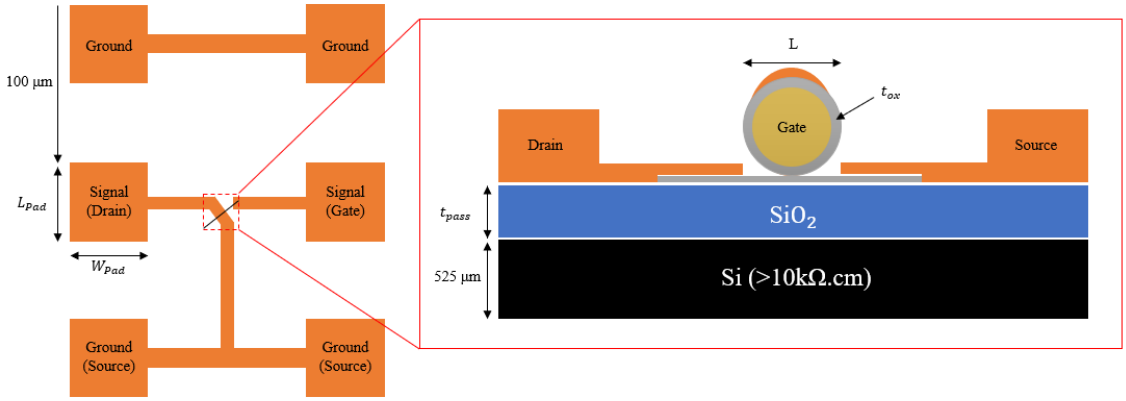

Figure 29: GFET schematic structure a) from top view. b) from cross-section of the channel.

The final device can be divided into two sections, intrinsic and extrinsic. The extrinsic section of the device is composed by the external electrodes which also serve as the contact pads for the radio-frequency probes. The pitch between each pad is set at 100 µm due to the available measuring probes and this value cannot be changed. As for the area of the pads, it was recommended that these were 50 µm * 50 µm. However, the length of the pad (L_{Pad}) can be reduced as the tip of the probe is very small, when compared to the 50 µm, but the width of the pad (W_{Pad}) must remain the same. The substrate and passivation layer are part of both extrinsic and intrinsic devices and are composed of highly resistive silicon (>10 kΩ.cm) with a silicon dioxide layer (t_{pass}), which thickness can be altered. High resistivity silicon was selected for the substrate of the devices due to the smaller dissipation of energy, when compared to regular silicon. As for the intrinsic parameters, channel length (L), channel width (W), the dielectric and its thickness (t_{ox}) are the parameters that can be altered. Channel length is dependant of the synthesis method of the nanowires, while channel width is dependant of the lithography performed to pattern the graphene.

3.3 Transistor Modelling

In order to best model the intended device, a high frequency small signal model must be adopted.

3.3.1 Proposed model

Since, in this work, the intended structure follows the fabrication methodology of L. Liao's device, it is safe to adopt the equivalent circuit topology proposed in that work.

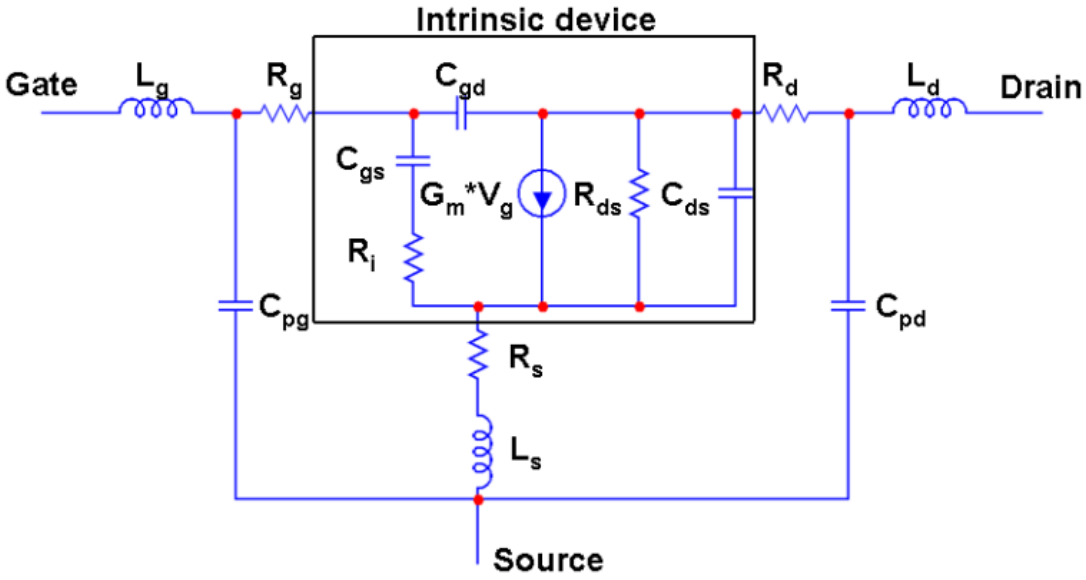

Figure 30: Equivalent circuit topology. Figure adapted/retrieved from reference [5].

O. Habibpour *et. al* [50] have developed a semi-empirical graphene field-effect transistor model that describes the current voltage characteristics of a GFET. From this model, only the current and transconductance equations will be used, as the geometry of the structure that the author compared its work to is very different from our intended one.

The type of majority carriers in the G-FET channel can be determined by the V_{gs}−V_{gd} device bias. The carriers are electrons for ($V_{gs} > 0$,$V_{gd} > 0$), both electrons (near the source) and holes

(near the drain) for ($V_{gs} > 0, V_{gd} < 0$), both electrons (near the drain) and holes (near the source) for ($V_{gs} < 0, V_{gd} > 0$), and holes for ($V_{gs} < 0, V_{gd} < 0$).

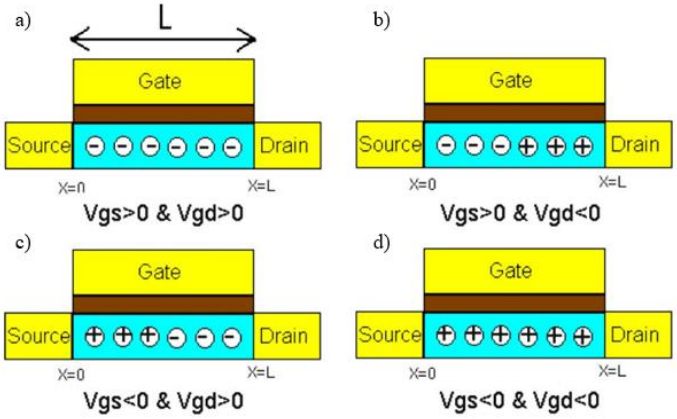

Figure 31: Majority carrier type in a G-FET channel at four different V_{gs}–V_{gd} plane quadrants. Figure retrieved from reference [50].

3.3.2 Drain current

The drain current is given by the following equation:

$$I_{ds} = q\frac{W}{L}\int_0^L n(x)v_{drift}(x)dx \tag{7}$$

Where $n(x)$, $v_{drift}(x)$, L and W are the carrier density, the carrier velocity, the channel length and the channel width. The carrier density in the graphene channel is modeled through the semi-empirical square-root charge-voltage relation [50]:

$$n(x) = \sqrt{n_0^2 + \left(\frac{C * V(x)}{q}\right)^2} \tag{8}$$

Where n_0 represents the residual carrier density and $C = (C_{gs} + C_{gd})/(L * W)$ is the gate capacitance per unit area. Through this model, when the voltage is zero, the carrier density is equal to the residual carrier density and when the voltage is high the carrier density equation is reduced to $n(x) = C * V(x)/q$.

The carrier drift velocity is modeled by the following equation:

$$v_{drift}(x) = \frac{\mu E(x)}{\sqrt[m]{1 + \left(\frac{\mu |E(x)|}{v_{sat}}\right)^m}} \tag{9}$$

Where v_{sat} is the saturation velocity of the carrier and depends on carrier concentration through $v_{sat}(n) = v_F\beta/\sqrt{n}$, v_F is the Fermi velocity, β relates to the optical phonon wavelength of the dominant scattering phonon, μ is the carrier mobility and m is a fitting parameter.

Changing variables from dx to dV by the following relation:

$$dV = E(x)d_x \tag{10}$$

And that the uniform electrical field can be approximated by:

$$|E(V)| = \frac{|V_{gs} - V_{gd}|}{L} \tag{11}$$

The current can be calculated with:

$$\begin{aligned} I_{ds} &= I_{ds1}\Theta(V_{gs} - V_{Dirac})\Theta(V_{gd} - V_{Dirac}) \\ &+ I_{ds2}\Theta(V_{gs} - V_{Dirac})\Theta(-V_{gd} + V_{Dirac}) \\ &+ I_{ds3}\Theta(-V_{gs} + V_{Dirac})\Theta(V_{gd} - V_{Dirac}) \\ &+ I_{ds4}\Theta(-V_{gs} + V_{Dirac})\Theta(-V_{gd} + V_{Dirac}) \end{aligned} \tag{12}$$

Where:

$$I_{ds1} = \frac{\mu_e V_0 Q_0}{1 + \frac{\mu_e |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}) \tag{13}$$

$$I_{ds2} = \frac{\mu_e V_0 Q_0}{1 + \frac{\mu_e |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_h V_0 Q_0}{1 + \frac{\mu_h |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(0, \bar{V}_{gd}) \tag{14}$$

$$I_{ds3} = \frac{\mu_h V_0 Q_0}{1 + \frac{\mu_h |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(\bar{V}_{gs}, 0) + \frac{\mu_e V_0 Q_0}{1 + \frac{\mu_e |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(0, \bar{V}_{gd}) \tag{15}$$

$$I_{ds4} = \frac{\mu_h V_0 Q_0}{1 + \frac{\mu_h |V_{gs} - V_{gd}|}{L\bar{v}_{sat}}} \frac{W}{L} f(\bar{V}_{gs}, \bar{V}_{gd}) \tag{16}$$

With the following relations for simplicity:

$$Q_0 = en_0 \tag{17}$$

$$V_0 = \frac{Q_0}{C} \tag{18}$$

$$f(x,y) = x\sqrt{1+x^2} - y\sqrt{1+y^2} + \ln\left(\frac{\sqrt{1+x^2}+x}{\sqrt{1+y^2}+y}\right) \tag{19}$$

$$\bar{V}_{gs} = \frac{V_{gs} - V_{Dirac}}{V_0}, \bar{V}_{gd} = \frac{V_{gs} - V_{Dirac}}{V_0} \tag{20}$$

Since the model requires continuous high-order derivatives, the step function utilized in I_{ds} is altered to a smooth analytical function.

$$\Theta(x) \approx U(x) = (1 + \tanh(x/V_1))/2 \tag{21}$$

Where V_1 is the fitting parameter.

3.3.3 Transconductance

Lastly, the transconductance is given by the following equation:

$$g_m = \left.\frac{dI_d}{dVgs}\right|_{Vds=const.} \tag{22}$$

$$\begin{aligned} g_m = {} & g_{m1}\Theta(V_{gs} - V_{Dirac})\Theta(V_{gd} - V_{Dirac}) + \\ & g_{m2}\Theta(V_{gs} - V_{Dirac})\Theta(-V_{gd} + V_{Dirac}) + \\ & g_{m3}\Theta(-V_{gs} + V_{Dirac})\Theta(V_{gd} - V_{Dirac}) + \\ & g_{m4}\Theta(-V_{gs} + V_{Dirac})\Theta(-V_{gd} + V_{Dirac}) \end{aligned} \tag{23}$$

$$= \frac{2\mu_e}{1 + \frac{\mu_e |V_{ds}|}{L\bar{v}_{sat}}} \frac{W}{L} * C\left(\sqrt{V_0^2 + (V_{gs} - V_{Dirac})^2} - \sqrt{V_0^2 + (V_{gs} - V_{ds})^2}\right) \tag{24}$$

g_{m1}

$$g_{m2} = \frac{2\mu_e}{1+\frac{\mu_e|V_{ds}|}{L\bar{v}_{sat}}}\frac{W}{L} * C\sqrt{V_0^2+\left(V_{gs}-V_{Dirac}\right)^2} - \frac{2\mu_h}{1+\frac{\mu_h|V_{ds}|}{L\bar{v}_{sat}}}\frac{W}{L} * C\sqrt{V_0^2+\left(V_{gs}-V_{ds}\right)^2} \quad (25)$$

$$g_{m3} = \frac{2\mu_h}{1+\frac{\mu_h|V_{ds}|}{L\bar{v}_{sat}}}\frac{W}{L} * C\sqrt{V_0^2+\left(V_{gs}-V_{Dirac}\right)^2} - \frac{2\mu_e}{1+\frac{\mu_e|V_{ds}|}{L\bar{v}_{sat}}}\frac{W}{L} * C\sqrt{V_0^2+\left(V_{gs}-V_{ds}\right)^2} \quad (26)$$

$$g_{m4} = \frac{2\mu_h}{1+\frac{\mu_h|V_{ds}|}{L\bar{v}_{sat}}}\frac{W}{L} * C\left(\sqrt{V_0^2+\left(V_{gs}-V_{Dirac}\right)^2} - \sqrt{V_0^2+\left(V_{gs}-V_{ds}\right)^2}\right) \quad (27)$$

This model requires a few constants parameters that are intrinsic to the graphene. These will come from literature, prioritizing results from graphene produce at the INL[51]. The following table presents these constants and shows the reference from each was taken.

Table 2: Constant parameters required by the current and transconductance model.

Parameter	Unit	Value	Reference
V_1	V	1/3	[50]
β	cm^{-1}	$4*10^5$	[52]
v_F	$cm.s^{-1}$	$1.1*10^8$	[51]
n_0	cm^{-2}	$1.37*10^{12}$	[51]
V_{Dirac}	V	0.51	[51]
μ_e	$cm^2V^{-1}s^{-1}$	1224	[51]
μ_h	$cm^2V^{-1}s^{-1}$	1042	[51]

The fitting parameter V_1 is set to 1/3 V, the same value as the authors of the model and β which relates to the optical phonon wavelength of the dominant scattering phonon and for

graphene on top of SiO_2 has the value of $4*10^5$ cm^{-1}. The rest of the values come from a recent article where liquid gate graphene field effect transistors were fabricated at INL and characterization of performance parameters took place. Residual carrier density (n_0), the minimum conductivity of the device (V_{Dirac}) and the mobilities of both charge carriers (μ_e and μ_h) were all retrieved from the same device presented in the aforementioned article.

3.3.4 Resistances

Drain-Source resistance (R_{ds}):

The drain to source resistance is a component belonging to the intrinsic device and is the resistance between the drain and source for a specific applied voltage bias to the device. The measurement is made in the ohmic (i.e. linear) region of the device and can be given by the following expression:

$$\frac{1}{R_{ds}} = g_{ds} = \frac{dI_D}{dV_{ds}}\Big|_{Vgs=const.} \tag{28}$$

Charging resistance (R_i):

The last component of the intrinsic device is the charging resistance (R_i). This resistance is due to the charging of the capacitor from gate to source. This value correlates with the dielectric used and its method of deposition, and for this reason, it will be the same as the one retrieved in the article.

3.3.5 Capacitances

Gate capacitance per unit area (C):

The core-shell nanowires possess a cylindrical shape which makes it hard to calculate the total gate capacitance. The approximation of dividing the nanowire into three pieces and assuming that only the middle section is in contact with the graphene and the remaining are a set distance to the channel, simplifies the problem while also still being accurate. Figure 32 shows the SEM cross section image of the fabricated device from [5], and it is clear too see that

only a small section of the wire is in contact with the graphene channel. The author goes on to perform electrostatic simulations of the structure and the result of the total top gate capacitance normalized per unit area is 394 nF/cm^2. The equivalent circuit of the total gate capacitance can then be seen as three parallel capacitors where the dielectric of the middle is the shell of the nanowire and the remaining two have the dielectric shell and a set thickness of air.

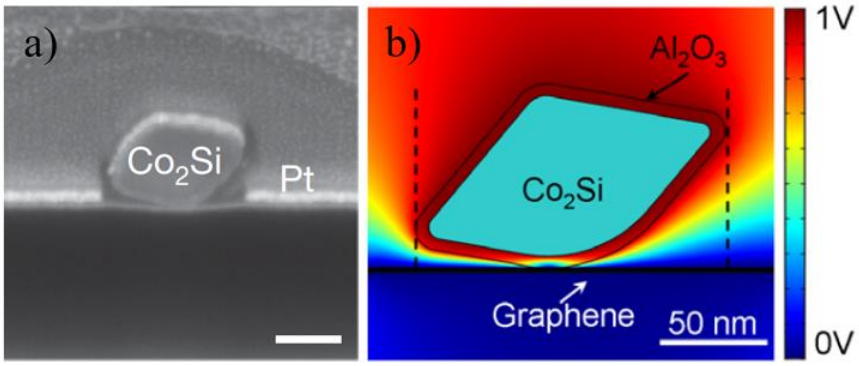

Figure 32: Nanowire placed on top of the graphene channel a) seen from an SEM image and b) the electrostatic simulations of the structure. Images retrieved from reference [5].

The quantum capacitance, a series capacitance with the oxide, is also considered in the electrostatic simulations. However, in the current and transconductance model, this does not factor into the equations as the authors state that it only needs to be considered for ultra-thin high k dielectrics. Figure 33 shows the equivalent circuit of this capacitance and the physical location of each capacitance on the device.

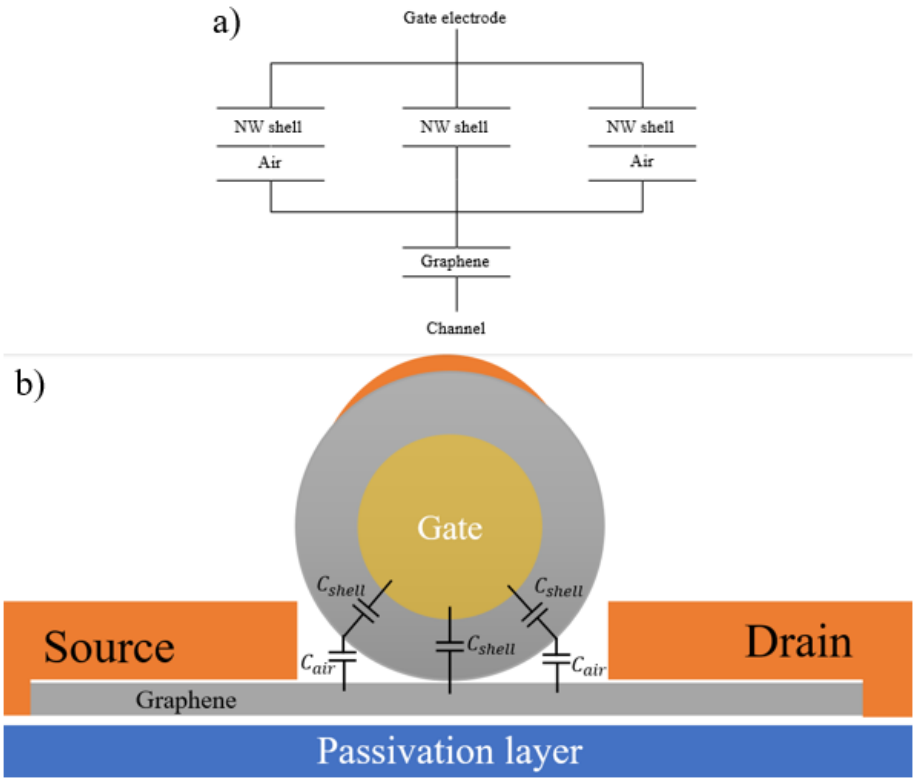

Figure 33: Total gate capacitance of the device. a) Equivalent circuit. b) Cross-section schematic of the equivalent circuit in a).

The Gate Capacitance per unit area (C) can then be calculated through the following equation:

$$C = \varepsilon_0 \varepsilon_{ox} \frac{1}{3} LW \frac{1}{h_{ox}} + \varepsilon_0 \varepsilon_{ox} \frac{2}{3} LW \frac{1}{\varepsilon_{ox} h_{air} + h_{ox}} \tag{29}$$

Where L is the channel length, W the channel width, ε_0 is the vacuum permittivity, ε_{ox} is the dielectric constant of the oxide used, h_{ox} is the thickness of the oxide and h_{air} is the thickness set for the air.

As a side note, there isn't much concern when it comes to the thickness of the air due to the fact that, if we input values for the above equation we can see that the majority of the C_T comes from the first part of the equation and so the air thickness is set to 20 nm.

Gate-Drain (C_{gd}) and Gate-Source (C_{gs}) capacitances:

Using the equation above, it is possible to obtain the values of the Gate-Drain and Gate-Source capacitances through the following equation:

$$C = \frac{C_{gs} + C_{gd}}{L * W} \tag{30}$$

If the wire is perfectly balanced on the structure, we can simply calculate C_{gs} and C_{gd} as:

$$C_{gs} = C_{gd} = \frac{C * L * W}{2} \tag{31}$$

Drain-Source capacitance (C_{ds}):

This capacitance is simply two capacitors in series, one being the SiO_2 substrate and the other is the quantum capacitance of the graphene. As it is explained before, the quantum capacitance will not be taken into account and thus reducing the equation to:

$$C_{ds} \approx C_{SiO2} = \varepsilon_0 * \varepsilon_{pass} * \frac{W * L_{ele}}{h_{pass}} \tag{32}$$

Where $L_{ele}$is the length of the electrode (metal on top of the graphene). L_{ele} will not be modelled and will be set at 2 µm. Figure 34 shows the equivalent circuit of this capacitance and its physical location on the device.

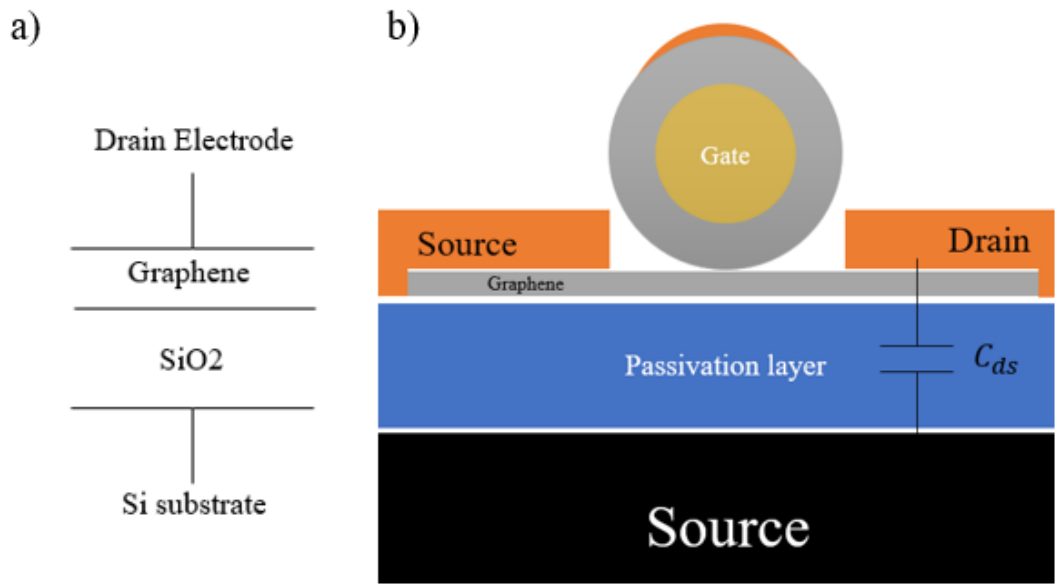

Figure 34: Drain source capacitance. a) Equivalent circuit. b) Cross-section schematic of the equivalent circuit.

Gate (C_{pg}), Drain (C_{pg}) and Source (C_{pg}) parasitic capacitances:

Since the source electrode will be connected to the ground terminal, the parasitic capacitance of the source will zero. In this setup the parasitic capacitances for drain and gate will emerge primarily from the contact pads and since these are identical these capacitances will have similar values. Figure 35 shows the equivalent circuit of these capacitances and its physical location on the device.

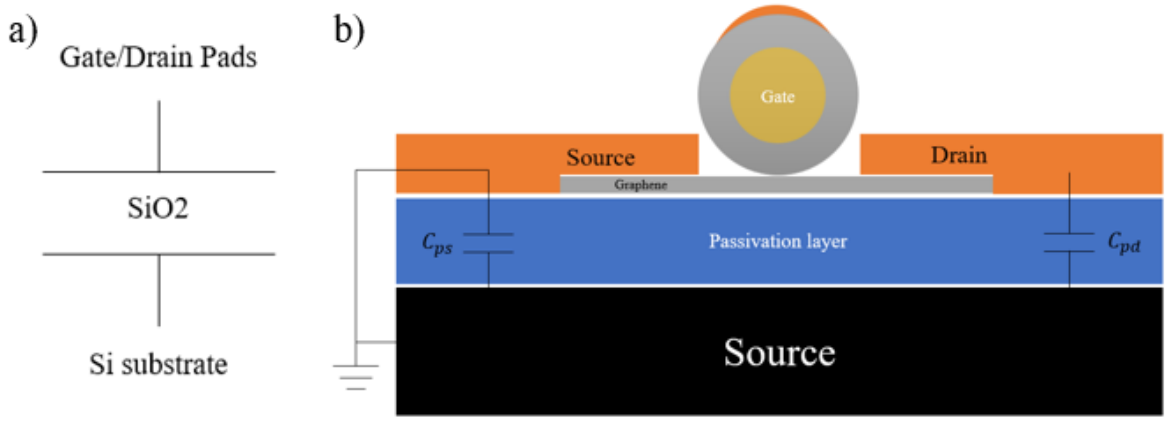

Figure 35: Parasitic drain source and gate capacitances. a) Equivalent circuit. b) Cross-section schematic of the drain and source parasitic capacitances.

As it can be seen from the image, the gate/drain parasitic capacitances are simply a capacitor with an oxide and so the equation can be given by:

$$C_{pg} = C_{pd} = \varepsilon_0 * \varepsilon_{pass} * \frac{W_{Pad} * L_{Pad}}{t_{pass}} \quad (33)$$

Where the ε_{pass} is the dielectric constant for the oxide of the passivation layer, W_{Pad} and L_{Pad} are the width and length of the contact pad, respectfully, and t_{pass} is the thickness of the passivation layer.

3.3.6 Remaining components of the circuit (R_g, L_g, R_D, L_D, R_S and L_S):

The gate, source and drain parasitic resistances and inductances have an additional difficulty in their calculation. Resistances and inductances can arise from, not only every metallic component of the device, but from the measuring system as well.

There is not much concern when it comes to inductances due to the fact that the measured results from [5] show very low values for these components. Since the structures being developed follow closely that work it is safe to assume the same values for these components as the ones measured, provided there are no significant changes to the device when it comes to dimensions.

The resistance associated with a metal layer (if the skin depth is not considered) is a simple equation that involves the geometric shape of the material and the associated resistivity of that material. In a more complex structure, where there's a metal stack and these metals have impurities between them (i.e. photoresist not properly removed in a fabrication process), there's an increase in resistance. The intended device has several sections that fall under these conditions. The connections between the nanowire core and the gate pad and the metal stacks are the primary source of these uncertainties. A guaranteed method to lower these resistances is through the use of metal with low resistivity values such as gold (Au: $\rho = 2.44\times10^{-8}\ \Omega.m$). However, the resistances from the contacts will always dominate over the intrinsic resistances of the metals. For these reasons, the remaining parasitic values used in our model will be the same as the ones measured in the article.

3.4 Performance assessment

This GFET model has the objective of providing a theoretical estimative of the device performance for a given set of physical parameters, and to evaluate the influence of each one on the transistor gain (g_m), cut-off frequency (f_T) and maximum oscillating frequency ($f_{máx}$). The physical parameters under study are shown in the following table. The starting values for these parameters are the ones retrieved in the article [5], as the structure is similar to the one we intended to fabricate.

Table 3: Physical parameters under study with starting values.

Parameters	Unit	Value
W	μ m	3
L	nm	180
t_{ox}	nm	5
L_{ele}	μ m	2
L_{Pad}	μ m	45
t_{pass}	μ m	300

3.4.1 Polarization

The DC polarization of the transistor will influence its gain, and subsequently its cut-off frequency. For this reason, it is necessary to provide the model with a gate-source voltage and a drain-source voltage. Inputting the parameters of the Table 3 into the equations depicted in the section 3.3, we are able to achieve the following transfer curve for the GFET for a constant V_{ds} of 0.5 V.

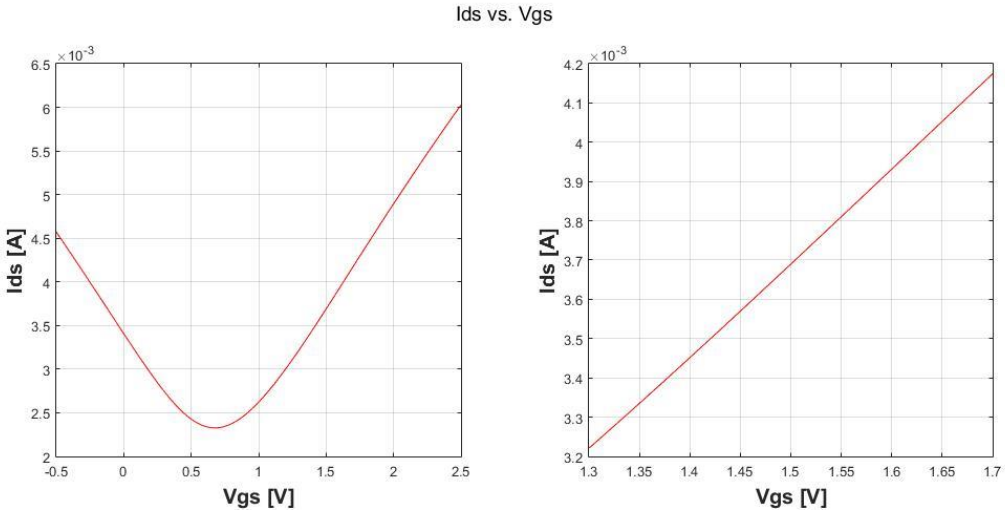

Figure 36: Transfer curve of the modelled GFET with inputted starting parameters and $V_{ds} = 0.5$ V.

Since we want to be working in the linear region of the device and that, for our case, the value of mobility of electrons is higher than holes we will choose a V_{gs} = 1.5 V, a value higher than the V_{Dirac}.

3.4.2 Figures of Merit

To assess the cut-off frequency value of the transistor, both intrinsic and extrinsic, and the maximum oscillating frequency, the following equations will be used:

$$f_{T,int} = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{34}$$

$$f_{T,ext} = \frac{g_m}{2\pi\left[\left(C_{gs} + C_{gd}\right)\left(1 + \frac{R_d + R_s}{R_{ds}}\right) + C_{gd}g_m(R_d + R_s) + C_{pg}\right]} \tag{35}$$

$$f_{máx} = \frac{f_{T,ext}}{2\sqrt{\left(R_g + R_i + R_s\right) * g_{ds} + 2\pi f_{T,ext} C_{gd} R_g}} \tag{36}$$

The values of Table 4, when ran through the model gives the following circuits parameter values with the subsequent figures of merit:

Table 4: Corresponding circuit component values and subsequent figures of merit for the starting parameters.

Parameters	W	L	t_{ox}	L_{Pad}	t_{pass}
Value	3 μ m	180 nm	5 nm	45 μ m	300 nm
This results in circuit components with:					
Components	I_{ds}	R_{ds}	$C_{gs} = C_{gd}$	C_{ds}	$C_{pg} = C_{pd}$
Value	4.208 mA	119 Ω	1.259 fF	0.23 fF	233 fF
With the following device characteristics:					
g_m	$f_{T,int}$	$f_{T,ext}$	$f_{máx}$		
3.38 mS	213.63 GHz	2.280 GHz	0.597 GHz		

Having defined the starting point of our GFET modelling, we will vary each physical parameter and assess its impact on the figures of merit.

3.5 Parametric Analysis

3.5.1 Channel width (W)

Table 5: Corresponding circuit component values and subsequent figures of merit for different values of channel width.

-------		W (μ m)							
		1	2	3	5	7	10	15	20
I_{ds} (mA)		1.403	2.805	4.208	7.013	9.818	14.026	21.039	28.052
R_{ds} (Ω)		356.5	178.2	118.8	71.3	50.9	35.7	23.8	17.8
$C_{gs} = C_{gd}$ (fF)		0.420	0.839	1.259	2.099	2.938	4.197	6.298	8.394
C_{ds} (fF)		0.230	0.460	0.690	1.15	1.61	2.30	3.45	4.602
$C_{pg} = C_{pd}$ (fF)		233							
g_m (mS)		1.127	2.253	3.280	5.633	7.887	11.267	16.900	22.534
f_T (GHz)	Intrinsic	213.63							
	Extrinsic	0.767	1.527	2.28	3.762	5.206	7.290	10.510	13.372
$f_{máx}$ (GHz)		0.348	0.490	0.597	0.763	0.892	1.045	1.229	1.354

The results of the channel width parametric analysis have both an increase in the transconductance, and the extrinsic cut-off frequency, as well as an increase in the maximum oscillating frequency. The higher channel width allows for a higher current to flow through and subsequently, a higher transconductance and a lower channel resistance. Surprisingly, the intrinsic cut-off frequency does not vary as the equation depends on both the transconductance and the total gate capacitance. As there is an increase in one, there is a similar increase in the other.

3.5.2 Channel length (L)

Table 6: Corresponding circuit component values and subsequent figures of merit for different values of channel length.

-------		L (nm)							
		50	75	100	180	300	500	1000	3000
I_{ds} (mA)		6.588	5.942	5.411	4.208	3.155	2.227	1.283	0.476
R_{ds} (Ω)		75.9	84.2	92.4	118.8	158.5	224.5	389.7	1050.3
$C_{gs} = C_{gd}$ (fF)		0.350	0.525	0.700	1.259	2.099	3.498	6.995	20.985
C_{ds} (fF)		0.690							
$C_{pg} = C_{pd}$ (fF)		233							
g_m (mS)		4.858	4.481	4.159	3.380	2.639	1.932	1.158	0.445
f_T (GHz)	Intrinsic	1105.3	679.7	473.1	213.63	100.07	43.97	13.17	1.686
	Extrinsic	3.306	3.044	2.820	2.280	1.767	1.278	0.744	0.257
$f_{máx}$ (GHz)		0.692	0.671	0.652	0.597	0.534	0.460	0.352	0.198

The results from this simulation follows the results published in literature [42]. The smaller the gate length the higher the cut-off frequency, reaching the tera-hertz in ranges of 50 nm.

3.5.3 Gate dielectric thickness (t_{ox}):

Table 7: Corresponding circuit component values and subsequent figures of merit for different values of dielectric thickness.

-------	t_{ox} (nm)							
	5	10	15	20	30	40	50	60
I_{ds} (mA)	4.208	2.940	2.614	2.482	2.374	2.331	2.309	2.295
R_{ds} (Ω)	118.8	170.1	191.3	201.5	210.6	214.5	216.6	217.8
$C_{gs} = C_{gd}$ (fF)	1.259	0.665	0.466	0.365	0.263	0.210	0.177	0.155
C_{ds} (fF)	0.690							

$C_{pg} = C_{pd}$ (fF)		233							
g_m (mS)		3.380	1.501	0.863	0.573	0.322	0.217	0.161	0.128
f_T (GHz)	Intrinsic	213.63	179.57	147.4	124.9	97.5	82.08	72.33	65.678
	Extrinsic	2.280	1.019	0.587	0.390	0.219	0.148	0.110	0.087
$f_{máx}$ (GHz)		0.597	0.320	0.195	0.133	0.077	0.052	0.039	0.031

The thickness of the gate dielectric influences the total gate capacitance, which, when increased, decreases the current in the channel, and subsequently its transconductance. All the figures of merit under study degrades if the gate oxide thickness is raised. It is important to mention that in the simulation the oxide chosen is Al_2O_3, as is the same dielectric used in [5], with a dielectric constant of 7,5. Another interesting study to be conducted is the type of gate oxide. It is easy to predict that the lower k the dielectric has, the lower the figures of merit of the transistor will be.

3.5.4 RF pad length (L_{Pad})

Table 8: Corresponding circuit component values and subsequent figures of merit for different values of pad length.

-------		L_{Pad} (μ m)							
		5	10	20	30	45	55	70	100
I_{ds} (mA)		4.208							
R_{ds} (Ω)		118.8							
$C_{gs} = C_{gd}$ (fF)		1.259							
C_{ds} (fF)		0.690							
$C_{pg} = C_{pd}$ (fF)		26	52	104	155	233	285	362	0.518
g_m (mS)		3.380							
f_T (GHz)	Intrinsic	213.63							
	Extrinsic	18.667	9.834	5.052	3.399	2.280	1.870	1.472	1.033
$f_{máx}$ (GHz)		4.875	2.573	1.323	0.890	0.597	0.490	0.386	0.271

As it can be seen form the simulation, the length and subsequent area of the pads only affect the extrinsic characteristics of the device performance. A smaller length of the pad will translate in a smaller ratio between the parasitic gate capacitance and the gate source capacitance which increases the extrinsic cut-off frequency of the device.

3.5.5 Thickness of the passivation layer (t_{pass})

Table 9: Corresponding circuit component values and subsequent figures of merit for different values of passivation layer thickness.

-------		t_{pass} (nm)							
		100	200	300	500	700	1000	3000	5000
I_{ds} (mA)		4.208							
R_{ds} (Ω)		118.8							
$C_{gs} = C_{gd}$ (fF)		1.259							
C_{ds} (fF)		2.071	1.035	0.690	0.414	0.296	0.207	0.069	0.041
$C_{pg} = C_{pd}$ (fF)		699	349	233	140	100	70	23	14
g_m (mS)		3.380							
f_T (GHz)	Intrinsic	213.63							
	Extrinsic	0.766	1.527	2.280	3.769	5.234	7.387	20.509	31.810
$f_{máx}$ (GHz)		0.201	0.400	0.597	0.987	1.370	1.933	5.354	8.286

This physical parameter, in the same way that the one prior, does not affect the DC characteristics of the device. It can be seen by the simulations that this value has to be increased as much as possible to allow higher extrinsic cut-off frequencies and maximum oscillating frequencies.

3.5.6 Device example

On the following simulation, the best results obtained in the previous ones for each physical parameter, are the ones used. By performing this simulation, we can approximately predict the values of the figure of merit for the fabricated structures.

Table 10: Corresponding circuit component values and subsequent figures of merit for the best values obtained in the simulations prior.

Parameters	W	L	t_{ox}	L_{Pad}	t_{pass}
Value	20 μ m	50 nm	5 nm	5 μ m	5000 nm
This results in circuit components with:					
Components	I_{ds}	R_{ds}	$C_{gs} = C_{gd}$	C_{ds}	$C_{pg} = C_{pd}$
Value	43.921 mA	11.38 Ω	2.332 fF	0.276 fF	2 fF
With the following device characteristics:					
g_m	$f_{T,int}$	$f_{T,ext}$	$f_{máx}$		
32.385 mS	1105.3 GHz	364.9 GHz	29.237 GHz		

This model gives an approximation of the figure of merit values and has a few limitations. For once, the resistances of the device are not being modelled and they play and huge roll, on the cut-off frequency but most importantly in the maximum oscillating frequency. Due to the geometry of the nanowire, the smaller it gets, the higher is its resistance, as it follows the following equation:

$$R = \rho \frac{l}{A} \tag{37}$$

For the device example, the l is increased and the A is decreased which in turn increases the resistance, when compared with starting values. Another down-side of this device is the L_{Pad} which has a value of 5 nm. Although the RF probe can make a connection onto it, the skill of the person operating the probes must also be high, as it is not an easy task to do so. For these reasons, a device with humbler set of physical parameters is shown afterwards:

Table 11: Corresponding circuit component values and subsequent figures of merit for a different device example.

Parameters	W	L	t_{ox}	L_{Pad}	t_{pass}
Value	10 μ m	150 nm	5 nm	20 μ m	1000 nm

This results in circuit components with:					
Components	I_{ds}	R_{ds}	$C_{gs} = C_{gd}$	C_{ds}	$C_{pg} = C_{pd}$
Value	15.302 mA	32.68 Ω	3.498 fF	0.690 fF	31 fF

With the following device characteristics:			
g_m	$f_{T,int}$	$f_{T,ext}$	$f_{máx}$
12.118 mS	275.7 GHz	45.66 GHz	6.233 GHz

With this device we managed to show, an RF graphene transistor operating in the gigahertz range capable of being produced at INL. The next step will be to fabricate the proposed device, in order to be able to compare the simulations with the device operating characteristics, in order to validate the model.

3.6 Conclusions

In this chapter, the fabrication methods of GFET already present at INL were analysed to understand if these were compatible with RF transistor structures. Upon realizing that the methods were not compatible, the several fabrication methods present in literature were analysed with the intent of assessing its compatibility with the processes at INL. A physical transfer of a core-shell nanowire was the selected choice and a model was adopted and altered to match this geometry. Through the modelling of the physical parameters, we were able to project the transconductance, extrinsic and intrinsic cut-off frequencies and maximum oscillating frequency of the intended device while also being able to show the physical parameters impact on these figures of merit. On the following chapter, the fabrication of these structures will be addressed.

4 NANOWIRE SYNTHESIS

4.1 Introduction

Bottom-up synthesis of nanowires can be achieved by a variety of methods. Electrochemical deposition of nickel onto an anodized aluminium oxide template (AAO) is the available method in our case. In this chapter, the several attempts to grow and subsequently transfer the nanowires will be presented, alongside the set-up employed and the requirements for the growth.

4.2 Electrochemical deposition set-up

The set-up employed to electrochemically deposit the nickel onto the AAO template can be seen in the Figure 37. The set-up consists of a DC power source, where one of the electrodes is connected directly to the metallic seed layer (i.e., cathode), and the other is inside the solution (i.e., anode), a set distance from the AAO template. The electroplating solution was a mixture of $NiSO_4$, $NiCl_2$ and H_3BO_3 [53]. The electroplating was carried out in DC mode with a constant current and different currents and times were tested for different lengths of the nanowires.

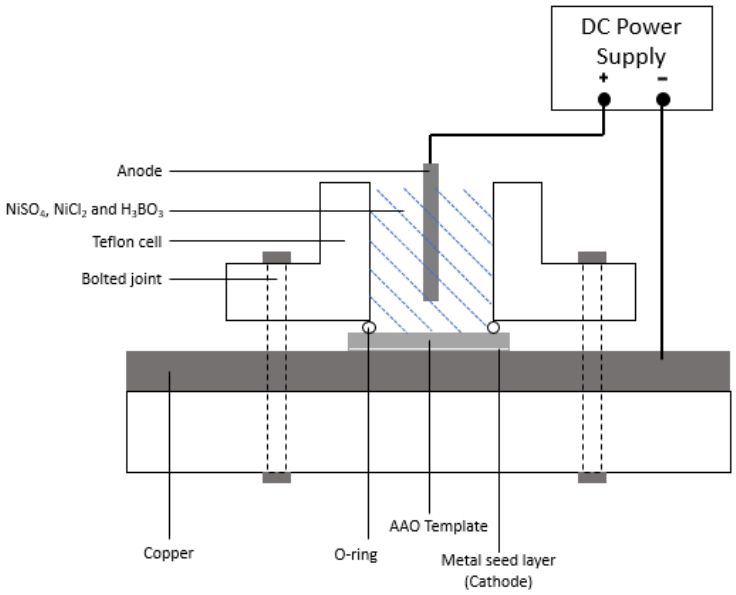

Figure 37: Detailed schematic of the set-up utilized for the electrochemical deposition of nickel. Figure adapted/reproduced from reference [54].

In the schematic presented previously, it is important to note a few key components. The copper serves the purpose of connecting the negative power supply to the metallic seed layer whilst serving as a support for the bolts who tightly hold the structure. The O-ring serves the purpose of not letting the liquid escape the confined space while both the O-ring and the Teflon cell are unaffected by the solution. The O-ring has a diameter of 1 centimetre which is used to calculate the current density applied to the seed layer through the following equation:

$$J = \frac{Current}{Area} \tag{38}$$

In order to perform the electrochemical growth, a seed layer of metal must be deposited first on one side of the AAO template to function as an electrode for the electrochemical deposition. Several metals were deposited to serve as these electrodes, those being nickel (Ni), palladium (Pd), gold (Au).

4.3 Nickel seed layer

4.3.1 Seed Layer deposition

The metallic seed layer of nickel was deposited through magnetron sputtering onto the first 3 templates and had a thickness of 100 nm. However, when placed on the electrochemical set-up the resistance of this film was too high which translates to a high deposition time. For this reason, before starting the deposition, the nickel films had to be thickened. This is achieved through an electrochemical deposition, with the same solution, but with the metal seed layer facing the anode. A tweezer was used to hold the template and to apply the current to the metal seed layer while an electrode was set at a distance from the seed layer which served as cathode. There was no control over the added thickness of the film, and later SEM images taken show that the surface, when compared to the sputter deposition film, became uneven.

Table 12: Growth conditions for the nickel seed layers.

	Pre-treatment	Growth conditions	Wire Length [µm]
1º Template	2 minutes – 20mA	1 hour – 10mA	-------
2º Template	10 minutes -10mA	5 hours – 1mA	49
3º Template	10 minutes – 2mA	-------	-------

The first seed layer was used as a test, as there was no prior information on growing nickel nanowires on the AAO templates, aside from literature, with the previously mentioned set-up. For this reason, both the currents of the pre-treatment and growth were elevated, when compared with further iterations of the process, and that translates into a thick seed layer and an overgrowth of the nanowires (Figure 38).

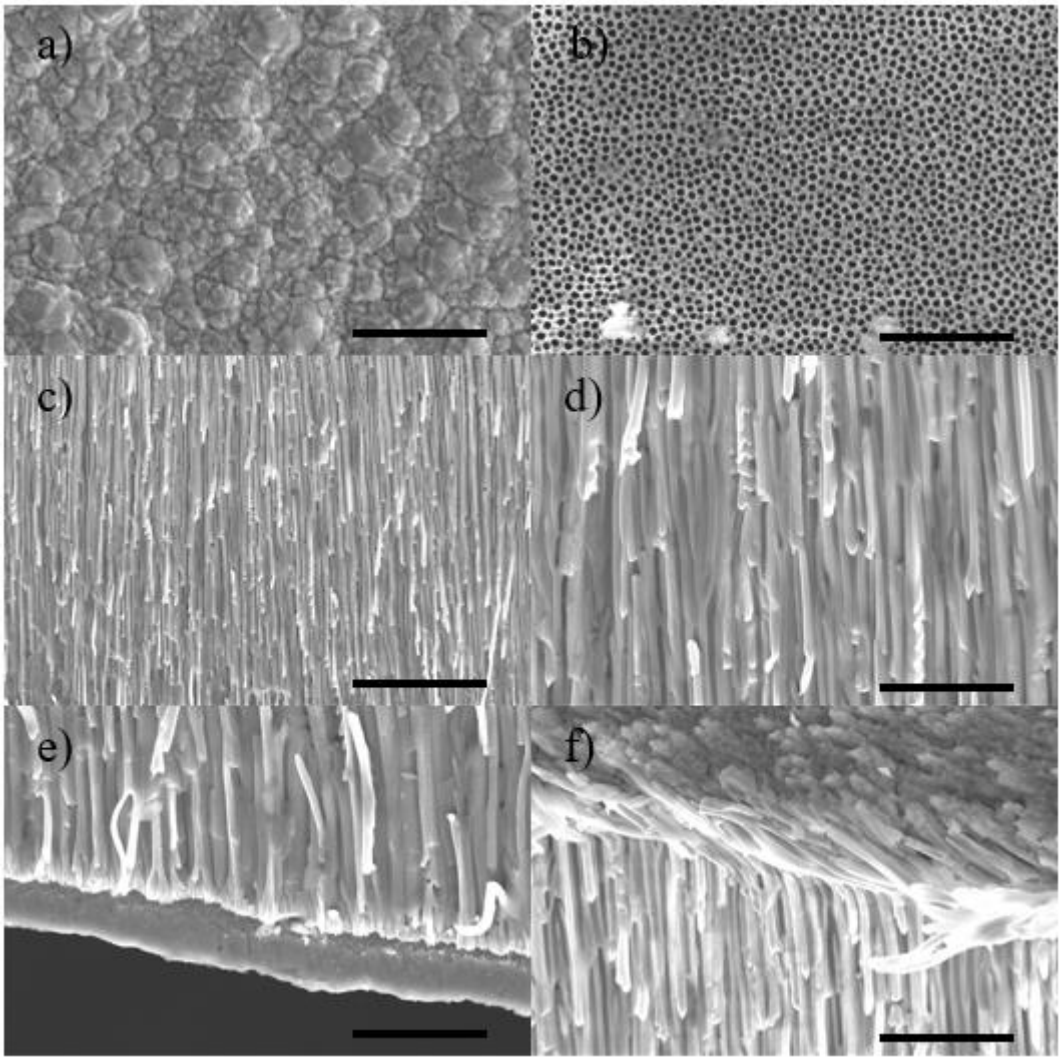

Figure 38: SEM images of cross and top sections of the AAO template with nickel nanowires grown inside. a) top view of AAO template where the nickel nanowires overgrew the pores. Scale bar: 5 μm. b) top view of AAO template covered by the O-ring during deposition. Scale bar: 5 μm c) middle section of the AAO template. Scale bar: 10 μm. d) close-up image of c). Scale bar: 4 μm. e) cross-section view of the AAO template with the nickel seed layer on the bottom. Scale bar: 4 μm. f) cross-section view of the AAO template with overgrown nickel nanowires. Scale bar: 4 μm.

The thickness of the seed layer, as it can be seen from the SEM images, ranges from 1 to 1,4 micrometers. Having in mind that the thicker the seed layer the harder it is to separate it from the wires, a smaller current was employed. As for the electrochemical deposition, the current was also reduced, so that the wires did not overgrew the pores (Figure 39).

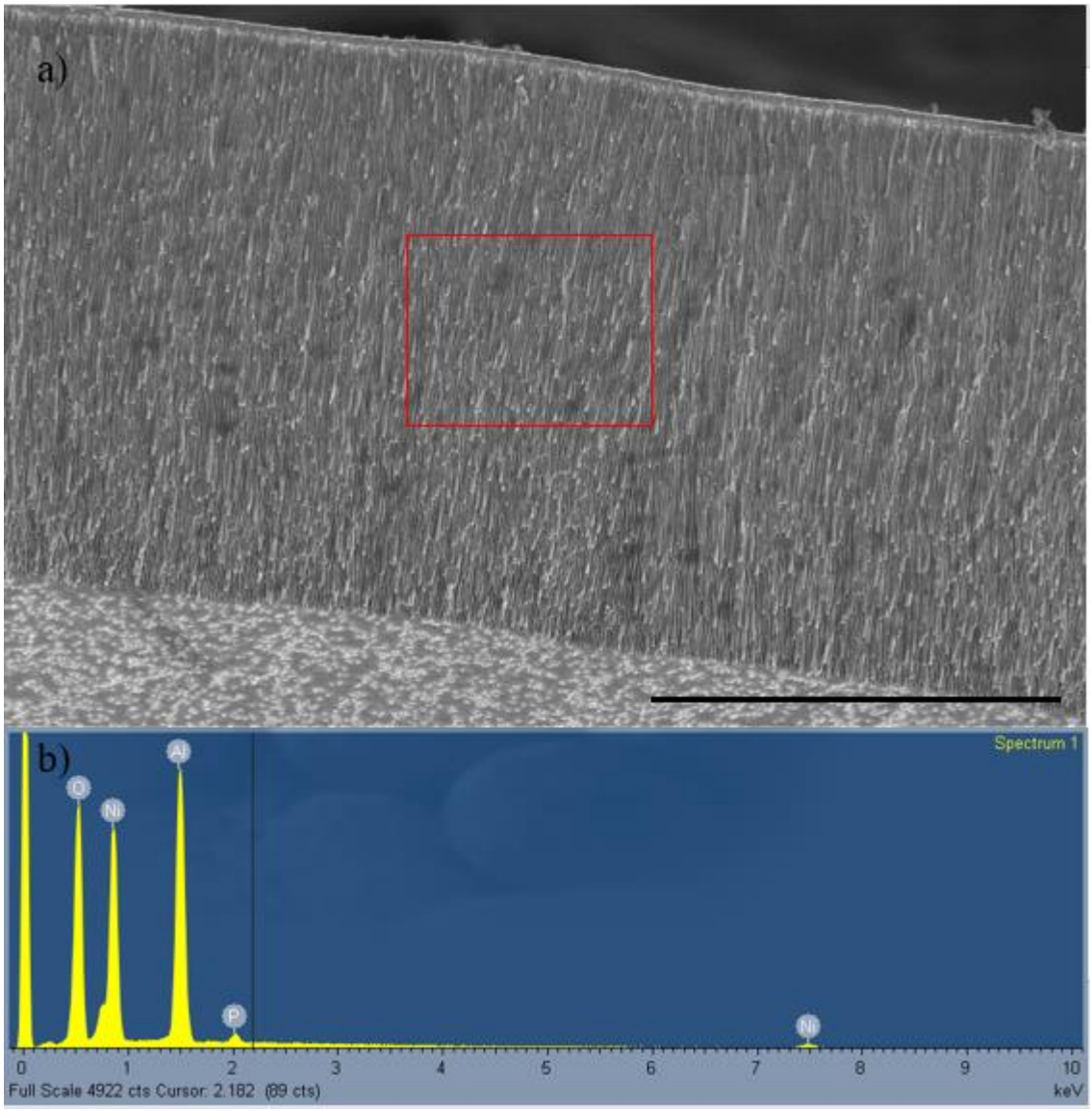

Figure 39: SEM image and EDX results of the AAO template after deposition. a) cross section of AAO template after deposition. Scale bar: 40 μm. b) EDX results of the red area in a).

From the SEM images, it is possible to observe that the thickness of the seed layer was reduced, ranging between 650 and 800 nanometers. In order to obtain an elemental identification of the AAO template and confirm the deposition of nickel into the pores, an Energy Dispersive X-Ray Analyzer (EDX) was employed.

The peaks obtained in the EDX can be explained as such:

- the peaks for aluminum (Al) and oxygen (O) come from the AAO (Anodized Aluminum Oxide) template.
- the peaks of nickel (Ni) are on par with the ones found in literature for the same type of deposition and the same solution [55] with the exception of one peak. The missing peak

is due to the presence of the AAO template, as the peak is small by itself and nonexistent with the template present.

- the peak of phosphorus (P) comes from a process of vacuum performed prior to the deposition. In order to remove gases inside the pores after the solution is placed in contact with AAO template, a small vacuum is employed to remove them, which in turn, increases the number of wires grown from one template. The oven used to perform the vacuum is borrowed from another group, which at the moment of the experiment were working with phosphorus and phosphorus composites which partially contaminated our sample. For this reason, further electrochemical depositions did not employ this process and exchanged it to simply putting the solution in contact with the template and waiting 15 minutes before turning on the DC power supply.

4.3.2 Template removal

Having electrochemically deposited nickel, it is necessary to remove the AAO template. As described in literature, a simple method for removing aluminum oxide without affecting nickel is to use a solution of NaOH [56]. Different concentrations of NaOH have been used, as well as different dissolution times and temperatures. The time chosen to etch the AAO template was 19 hours in a concentration of 1 M and at a temperature of 45ºC. It is important to note that the NaOH solution must be kept inside a plastic flask and not a glass one, as it reacts and may produce silicon contaminations. The temperature is used to speed up the process and there is not much concern when it comes to the etching time, as the NaOH will not affect the nickel nanowires, so as long as the AAO is removed, the template can be left in the etching solution. The EDX results still show peaks of aluminum and oxygen which are parts of the template which were not dissolved. This comes from the fact that the pores are too closer together and subsequently, so are the nanowires grown (Figure 40). This will come as a disadvantage later on the process, when the deposition of a dielectric shell on the nanowires will be needed. The irregularity of the nanowires (Figure 40) is also a concern as the length of the channel is given by this diameter, however, the fabrication process is still achievable.

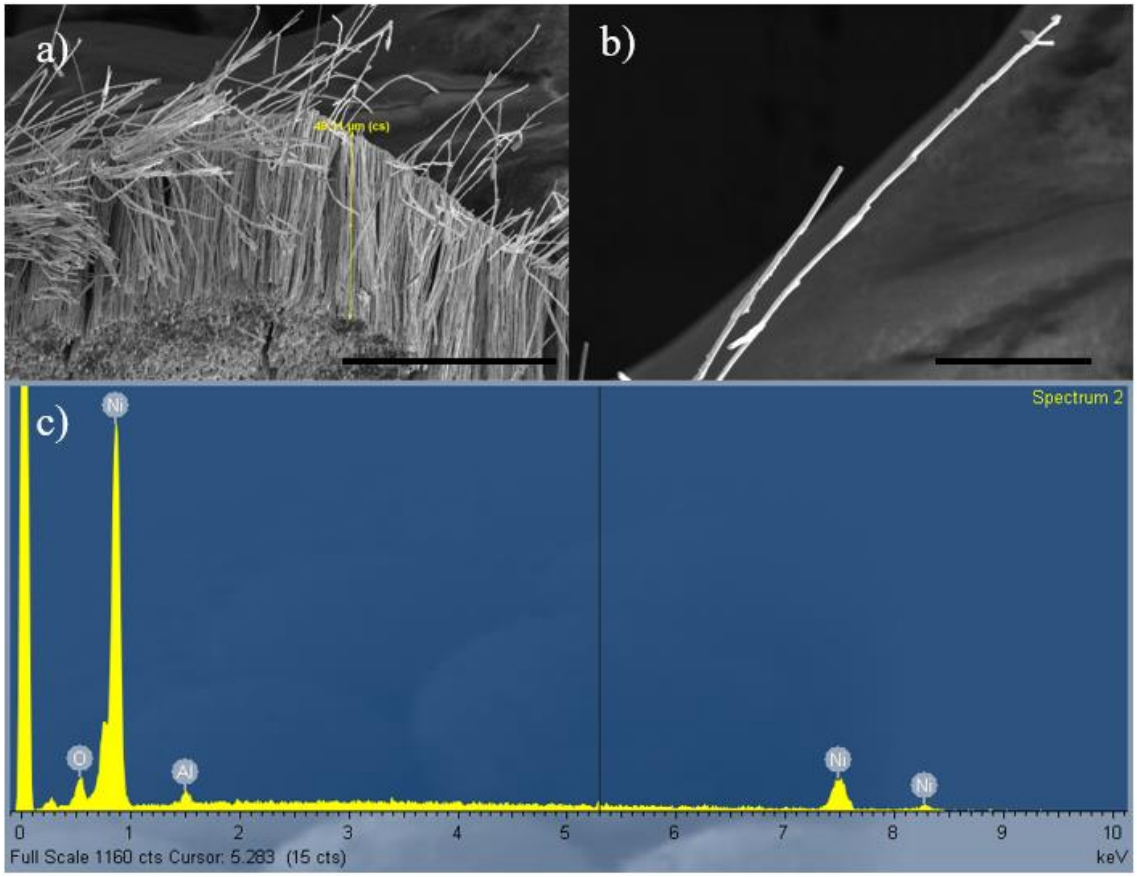

Figure 40: SEM images and EDX results after the template dissolution. a) cross-section SEM image of the AAO template after dissolution with a measurement from top to bottom of the nanowires which indicates a length of 49 µm. Scale bar: 40 µm. b) close-up SEM image of a single nanowire. Scale bar: 10 µm. c) EDX results of the middle section of the template.

4.3.3 Release attempt: Grind Method

In order to remove the nickel nanowires from the seed layer, the first attempt was through the use of a mechanical grind. The grind method was unable to release the nanowires from the seed layer as they simply got crushed into it (Figure 41). The use of ultrasonic bath after the grind was also used, in an attempt to release the nanowires. However, it was impossible to obtain any SEM images of the results as the only particles found were small segments of what we believe to be nickel (Figure 41).

This method of nanowire removal does not provide any results. Opting for a different substrate, where the interaction between the seed layer and the electrochemically deposited nickel is lower, was the strategy adopted next, using palladium as the new seed layer.

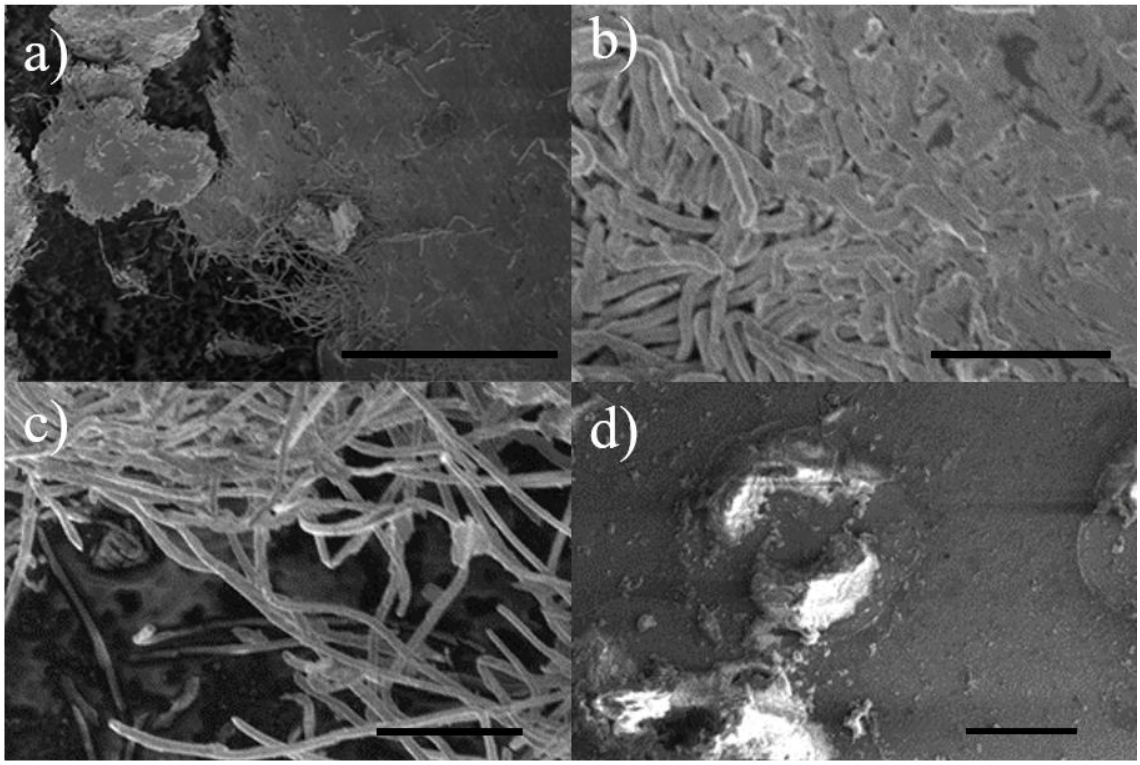

Figure 41: 1st attempt to remove nickel nanowires from nickel seed layer. a) – c) SEM image of the seed layer with the nanowires after mechanical grind. Scale bar: 40 μm,4 μm and 5 μm, respectfully. d) SEM image of the seed layer with the nanowires after 1 hour of ultrasonic bath. Scale bar: 5 μm.

4.4 Palladium seed layer

A thickness of 420 nm of palladium deposited through magnetron sputtering was used as the new seed layer. The electrochemical deposition set-up and solution were the same as the one used in the previous experiment. However, on this run, a shorter deposition time was used in order to achieve nanowires with lengths in range of 20 - 30 μm. Nickel nanowires were gown with a current of 1 mA for 3 hours, achieving nanowire lengths of 18 μm (Figure 42). Pressure washing of the substrate after the AAO dissolution managed to remove some of the wires attached to the seed layer. However, the amount of solution created, coupled with the fact that most of the nanowires did not detach from the seed layer, created a low concentration of wires which made it impossible to find any wire when the solution was drop casted onto a substrate.

An alternative conclusion for the missing nanowires can be that these simply did not grew due to gases and impurities that may already have been inside the template prior to the growth.

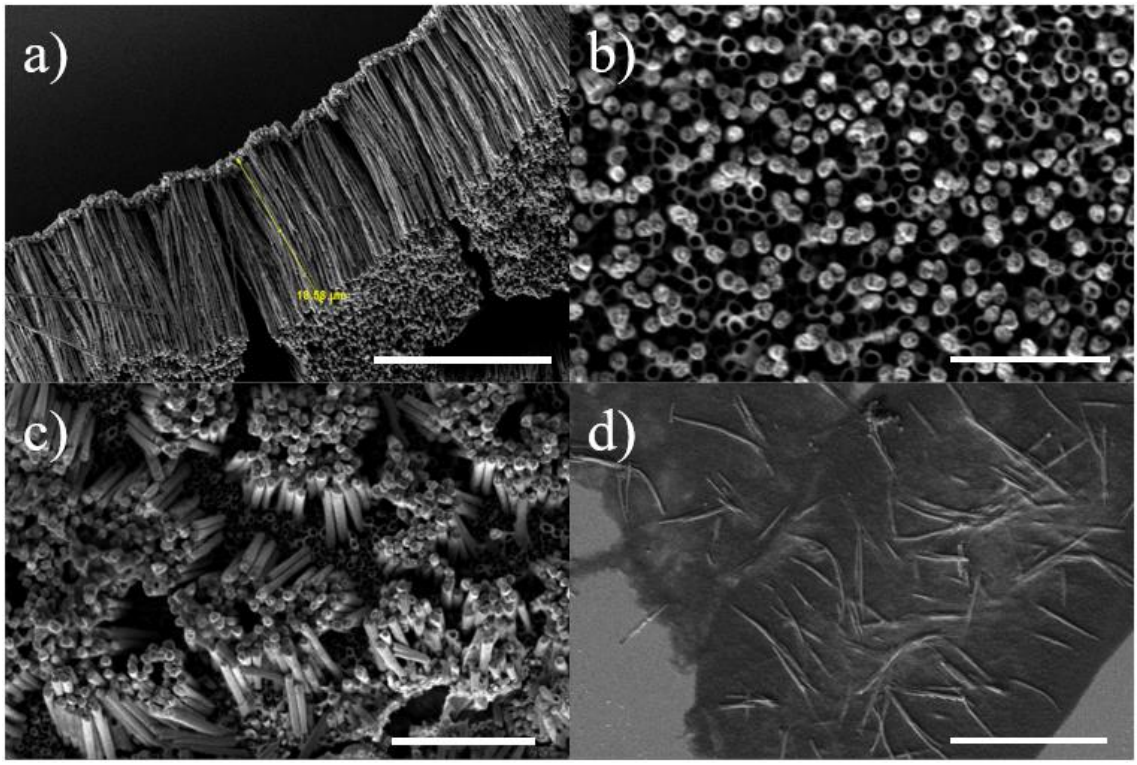

Figure 42: Palladium seed layer results. a) cross-section view at an unknown angle of the palladium seed layer with the attached wires. Scale bar: 20 µm. b) and c) top view of the palladium seed layer with the nanowires attached. Scale bar: 3 µm and 5 µm, respectfully. d) palladium seed layer with nanowires attached to its back side. Scale bar: 10 µm.

4.5 Gold seed layer

4.5.1 Release attempt through sonication bath

Sputter deposited gold with a thickness of 250 nm as a seed layer allowed for different strategies to be used. The first consisted of using ultrasonication of the seed layer with the nanowires on top to release them.

The standard method of growing the nanowires was used. A 30-minute wait after placing the nickel-based solution in contact with the template, a current of 2 mA for 3 hours and a 48

hour bath in 1 M NaOH produced the exposed nanowires on top of the gold seed layer. A larger current of 2 mA was used to achieve the desired 20-30 μm length of the nanowires.

One-hour ultrasonic baths of the gold seed layer with the wires managed to release some of the wires onto the solution but in turn these would bend and aggregate like its shown in the SEM images. It is also worth noting that these method does not remove the gold seed layer as it only destroys it into smaller sizes. In an attempt to separate the wires from one another, after the ultrasonic bath, the solution with the released nanowires was diluted and went through another hour of sonication bath in order to reduce the number of wires per droplet (Figure 43). The results still show a large aggregate of nanowires, so the same steps were taken to further reduced this effect and separate the nanowires (Figure 43). The use of surfactants was also employed, however, the effect was minimal and the nanowires that got separated were covered with the chemical. Not knowing the effects of this chemical on the graphene and subsequent device performance, this method was dropped. The nanowires, after the sonication bath, became bent and destroyed, which for the intended application would not be ideal.

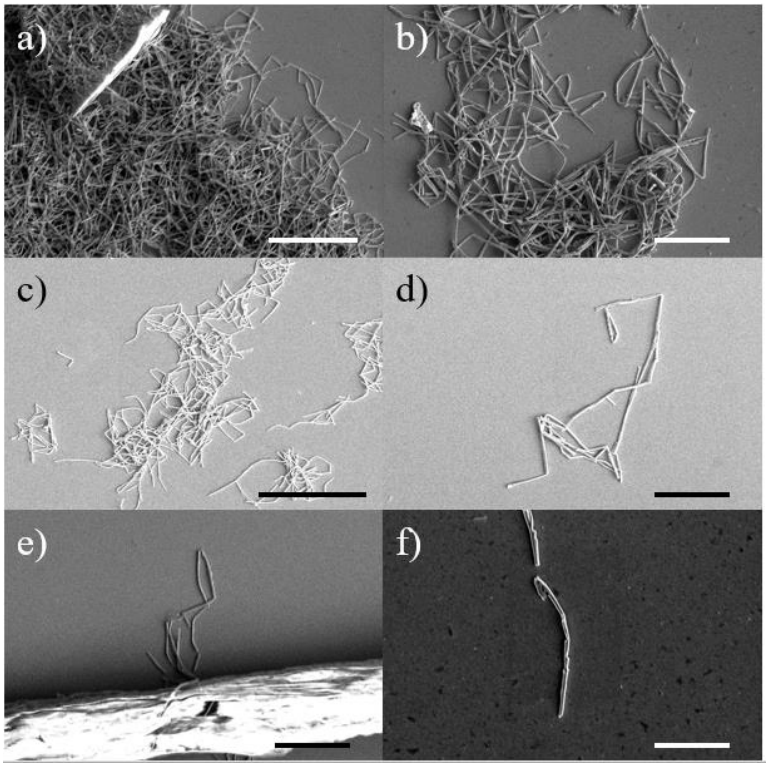

Figure 43: SEM images showing the results of the ultrasonication bath method. a) and b) 1-hour sonication bath. Scale bar: 20 μm and 10 μm, respectfully. c) and d) dilution of a) and b) and 1 more hour of sonication bath. Scale bar: 30 μm and 10 μm, respectfully. f) Dilution of c) and d) and 1 more hour of sonication bath. Scale bar: 10 μm and 50 μm, respectfully.

4.5.2 Release attempt: Seed layer etch first

Another technique to release the nanowires is to remove the gold seed layer with an etchant solution consisting of potassium iodide (KI, 4g) and iodine (I_2, 1g) in a water medium (H_2O, 40 ml). The etchant solution also removes the nickel but does not affect the aluminium oxide and for this reason the gold removal took place prior to the AAO removal.

Nickel nanowires were grown the same method as the previous experiments, with 2 mA for 3 hours. After the growth, the gold was etched with the etchant solution for a period of 10 minutes followed by a DI water rinse and the template was removed with a solution of NaOH 1 M for 24 hours. In literature the etch rate of gold with this solution is in the range of micrometres per minute. However, in our case the gold layer has some impurities in its surface making it harder for the etchant to the reach the metal and thus increasing the etch time. Clusters and chunks of material resulted from the process, still visible at naked eye, were removed from the NaOH solution and transferred to an ethanol based one, as it is easier to use with the drop casting method. As it can be seen from the optical images of the experiment (Figure 44), some parts of the gold seed layer were not removed, however, it is possible to see clusters of nanowires detached from the seed layer.

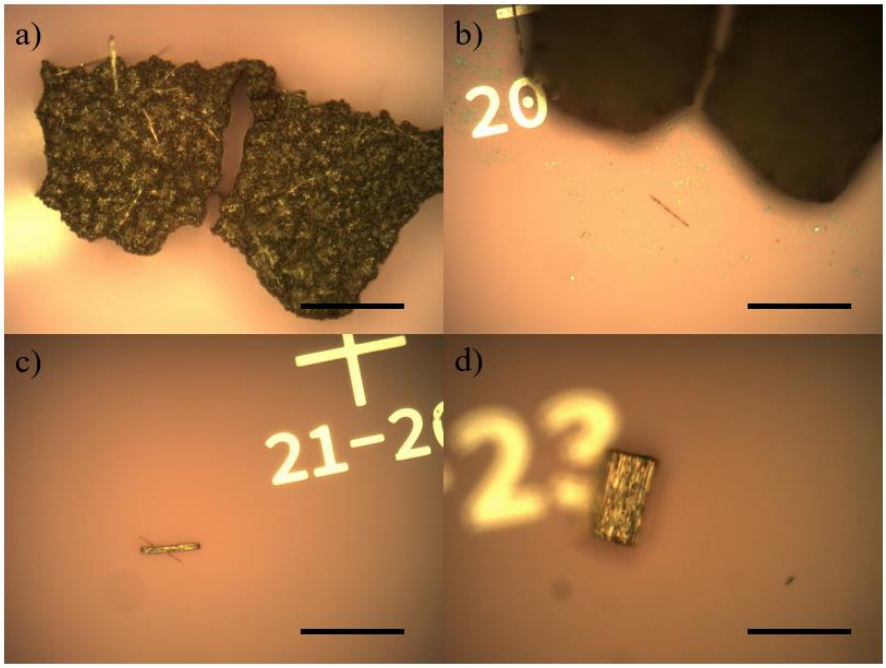

Figure 44: Optical microscopic images after the etch of gold and subsequent AAO dissolution. a) unetched piece of gold seed layer with clusters of nanowires attached to its surface. Scale bar: 60 µm. b) different focus of a) showing cluster of nanowires on the substrate surface. Scale bar: 60 µm. c) and d) different sizes of clusters of nanowires deposited on the surface. Scale bar: 60 µm and 30 µm, respectfully.

The larger pieces of seed layer quickly deposited on the Eppendorf which allows the removal of these cluster on to another solution. Upon transfer, a proposed method to scatter the nanowires is to perform an ultrasonic bath for a duration of 10 minutes. Figure 45 shows the optical images, and corresponding SEM images of the results of this experiment. It is possible to conclude that the 10-minute ultrasonic bath achieves the spread of the clusters. However, it is worth noting that if there is a large number of nanowires in the solution, the sonication bath will bend them as they clash against each other. The sample was taken into the SEM in order to assess if they were single nanowires. Out of 6 positions analysed, only one of them was a double nanowire.

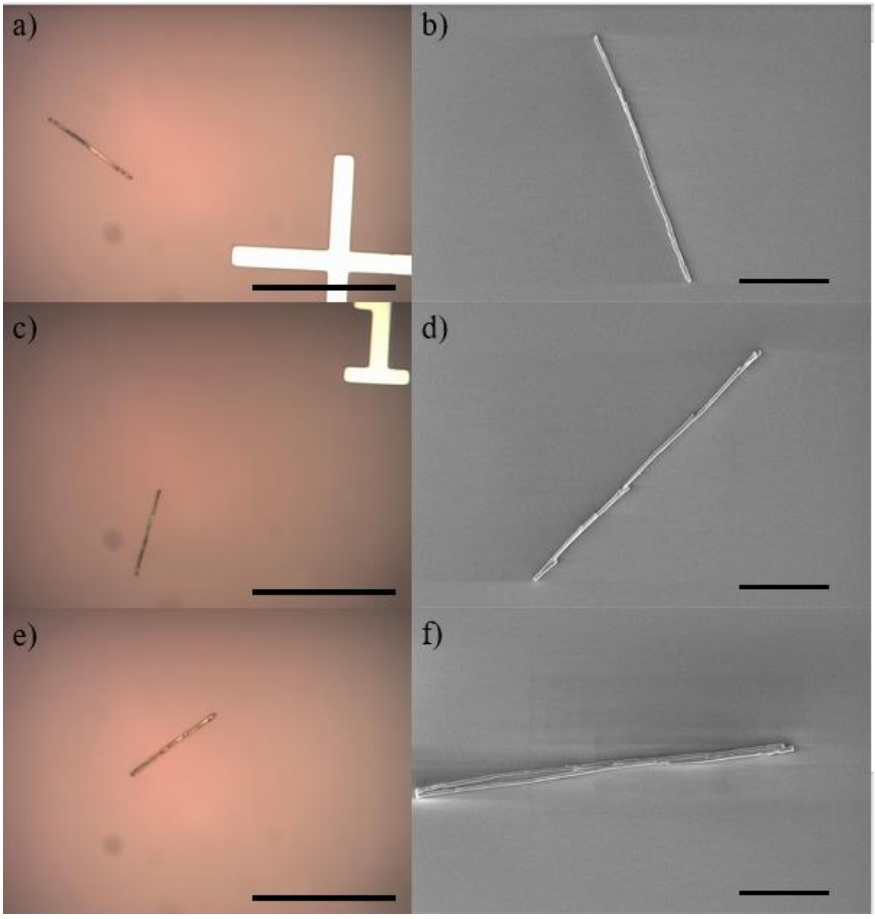

Figure 45: Optical and corresponding SEM images of 3 random nanowires found in the substrate. a), c) and e) Scale bar: 90 μm. b), d) and f) Scale bar: 10 μm.

4.5.3 Releases attempt: Dissolution of the AAO template first

This method of synthesis and handling of nanowires provides a reliable method of achieving spread out nanowires on a surface. However, there is still the requirement of depositing the dielectric shell and it is easier to perform this step when the nanowires are still attached to the seed layer. The gold etch solution, also affects the nickel nanowires, but since it's a reduction agent, it does not affect the aluminium oxide and other oxides. With this in mind, the following process was tested. Nanowires were grown in the exact same conditions as before and the template dissolve afterwards leaving the nanowires attached to the seed layer. In an intermediate step of oxidation, the seed layer with the nanowires was taken into an oven for one hour at 250ºC. This method of oxidation, has been reported in literature to provide, on nickel nanoparticles, a 5 nm thick shell of nickel oxide[57]. To assess the nickel/nickel oxide nanowires resistance to the gold etchant, both oxidized and non-oxidized nanowires were left in the etchant solution for 12 hours. The results showed that the solution with the oxidized nickel nanowires still contained several nanowires while in the other we had found none. This leads us to conclude that the nickel oxide is not affected by the gold etchant solution. However, the ethanol solution left some impurities on the substrate, which could be removed with a simple DI water wash.

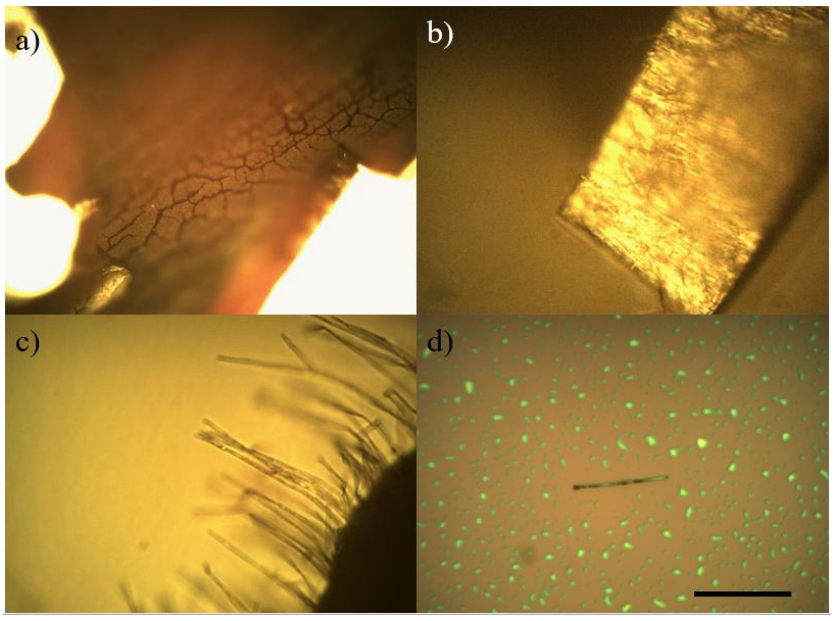

Figure 46: Optical microscope images of the nanowire oxidation process. a) metal seed layer with the nanowires after the template dissolution. b) and c) close up images of a). d) nickel/nickel oxide nanowire after being realised from the seed layer. Scale bar: 30 μm.

4.6 Results and Discussion

Nanowire synthesis can be performed by a variety of methods. A simple synthesis method is through electrochemical deposition onto a template and was the pursued methodology in this work. The nanowires grown in this work were made of nickel on a commercial AAO template, with diameters varying, within the nanowires, between 200 and 400 nm. The diameters of the nanowires are dependent of the template used and different diameters can be achieved by this method if different templates are used. The length of the nanowires is dependent on the templates thickness and the electrochemical deposition time. The number of nanowires grown depends on both the template and the electrochemical deposition set-up. The electrochemical deposition set-up had the O-ring of 1 centimetre in diameter in order for the solution used to be confined to that space. In turn, this will only allow the nanowires to grow within that space. The number of nanowires is also dependant on how close together the pores of the template are. The distance between each pore in the template used was 0.07-0.12 μm. Assuming the widest pore diameter (i.e., 400 nm) and the widest pore inter-distance (i.e. 0.12 μm) which for the 1 centimetre translates into roughly 4.7E8 nanowires per template used.

The fact that the template had its pores so close to each other translated into the nanowires growing too close to each other, resulting in their aggregation after the removal of the template. For this reason, the nanowires had to be released from the template in order to deposit the required shell.

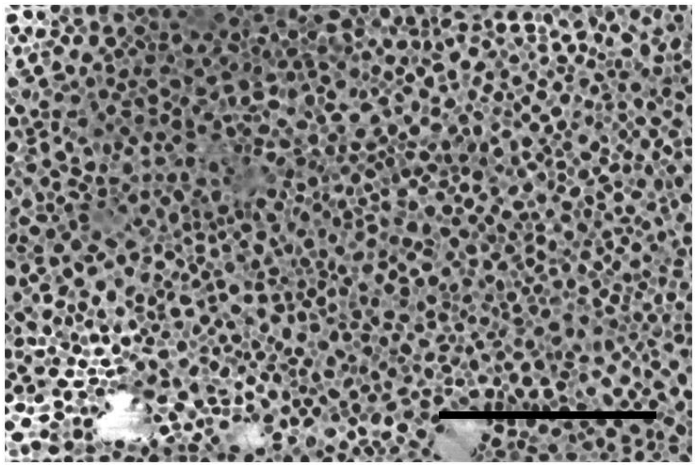

Figure 47: SEM image of the templates used. Scale bar: 5 μm.

The results obtained in this experiment are in agreement with the ones reported in literature. The aggregation of the nanowires was also seen in [58], [59] after the dissolution of the AAO template. The nanowire length on those reports ranges from 50 nm to 50 μm which is dependent on the electrochemical deposition time and the diameter dependant on the template used.

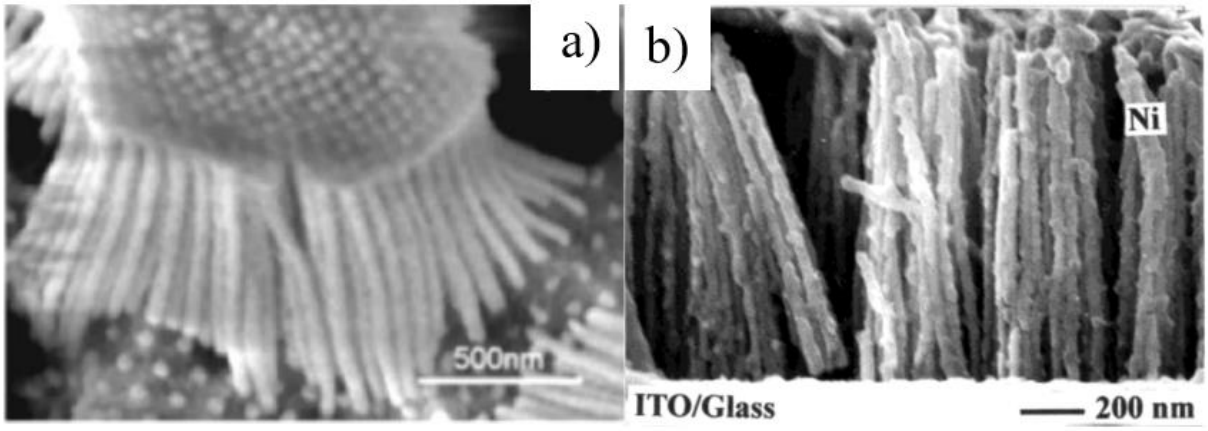

Figure 48: Aggregation of nickel nanowires reported in literature. Figures adapted/retrieved from references [58] and [59], respectively.

4.7 Conclusion

In this chapter, the methods of nanowire synthesis and removal from the metallic seed layer were presented. Through the use of a gold seed layer and the gold etchant solution, different methods of removal of the nanowires were tested for implementation in the fabrication process. Of all the tested strategies, only two showed promising results. The method of first removing the gold seed layer achieves spread out nanowires, however, the dielectric must still be deposited on the nanowire. The method of removing the seed layer after the deposition of the oxide, enables a better approach for the synthesis of core-shell nanowires. Be that as it may, the AAO template has its pores too close together, and subsequently after the electrochemical deposition, the nanowires will aggregate, which becomes challenging to deposit any material on the nanowire surface

5 GRAPHENE FIELD-EFFECT TRANSISTOR WITH NICKEL/NICKEL OXIDE CORE-SHELL NANOWIRE GATE

5.1 Introduction

In the previous chapter, nickel nanowires were synthesised through an electrochemical deposition (bottom-up approach), assisted with an aluminium oxide template and two different techniques were developed to release the nanowires. In this chapter, nickel nanowires will be oxidised, to form core-shell nanowires, and the fabrication and characterization of the graphene field effect transistor will be presented.

5.2 Nickel oxide shell

Nickel oxide, the natural oxide of nickel, was the dielectric chosen to serve as the gate dielectric in the first run of the experiment. Nickel is a self-oxidising material and when exposed to air, a 5 nm thick layer of oxide is formed [60]. In our experiment, however, we utilized an oven to promote the creation of this layer. In the previous chapter, we already oxidized the nickel nanowires in one of our release methods. However, to ensure that no gaps in the oxide were formed, we increased this thickness to 15 nm, following the results obtained in literature[61]. Nickel nanowires were electrochemically grown, with the method described in the previous chapter, followed by an oxidation in an oven at 250ºC for 3 hours. The nanowires were released from the seed layer with the gold etchant solution and transferred into an ethanol-based solution.

In order to assess the thickness of the ultra-thin oxides and dielectrics, Transmission Electron Microscopy (TEM) is the tool of choice, however in this work, this tool was not available. Atomic Force Microscopy (AFM) was employed to assess the oxide thickness

resulting from the oxidation. Since the nanowires have irregular shapes, it is important to characterize the same nanowire in the same position before and after oxidation. For this reason, the nanowires on top of the gold seed layer, were first oxidized with 5 nm of nickel oxide (1 hour at 250ºC), to withstand the gold etch solution, and transferred to a silicon dioxide substrate to perform the characterization. The oxidation to be characterized was performed in the same oven at 250ºC for a duration of 3 hours. AFM results show an increase in 15 nm before and after the second oxidation. These results are consistent with the literature, as the oxidation did not take place where the nanowire was in contact with the silicon dioxide. If the nanowire would have been standing in the metal seed layer, this increase show be expected to be 30 nm. AFM was performed in contact mode, rather than drag mode which would cause the nanowire to be dragged and change its position. However, contact mode, in theory, could provide the same outcome but special care was taken when performing the AFM to look out for any irregularities in the measurements. Also, the AFM images taken show no change of position of the nanowire, before and after oxidation.

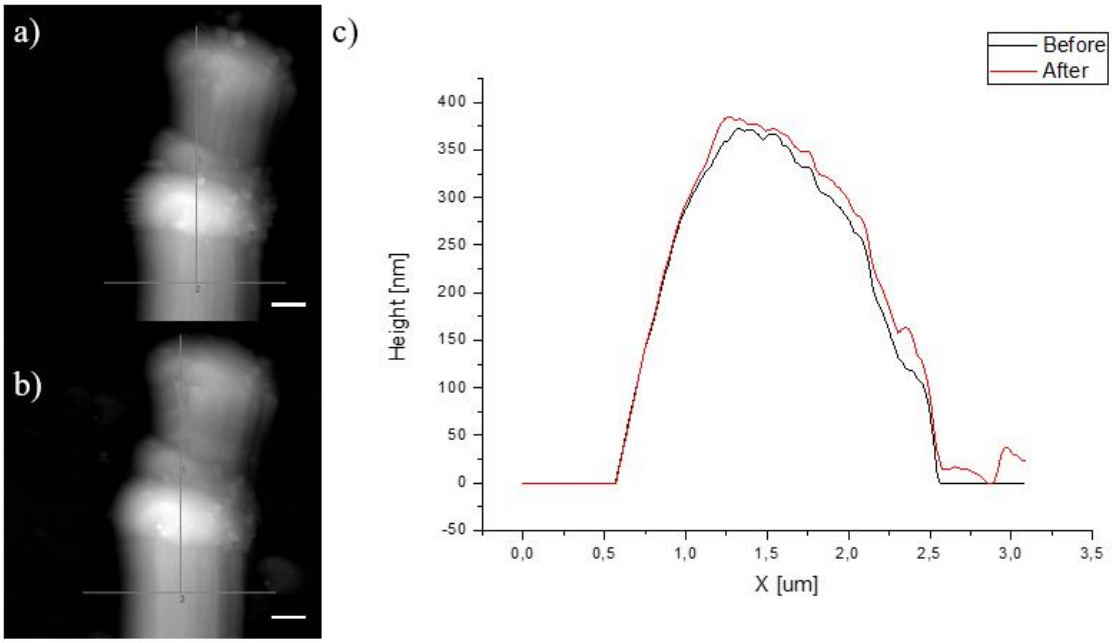

Figure 49: Nickel oxide thickness characterization. a) AFM image before oxidation. Scale bar: 0,5 µm. b) AFM image after oxidation. Scale bar: 0,5 µm. c) Comparison of the AFM results before and after oxidation.

5.3 Fabrication

The graphene field-effect transistors were fabricated on a highly resistivity silicon substrate (>10 kΩ.cm) with 2 cm by 2 cm of size.

5.3.1 Passivation layer

A passivation layer of silicon dioxide was deposited by plasma enhanced chemical vapor deposition (PECVD) with a thickness of 1 μm. In order to characterize the thickness of the silicon dioxide, a spectrometer was used. Measurements from the middle section of the substrate gave a value of 992 nm while from sections closer to the edges, the values were higher, in the order of 1043 nm. This discrepancy is due to the molecule accessibility to the specific area, outer surfaces have larger area of access in contrast to the middle which has a confined access area.

5.3.2 Matrix of optical markers

Optical markers will be required, in a later part of the fabrication process, to assist in the subsequent lithographies. However, these have to be deposited prior to the graphene transfer, in order to not damage it. A lift-off assisted process was used to pattern the TiWN optical markers with a thickness of 30 nm. The lithography starts with the process of vapor prime, which at a temperature of 150 ºC, coats the surface with HDMS (*hexamethyldisilazane*) promoting the adhesion of photoresist to the surface by turning it hydrophobic. Photoresist AZ1505 is spin coated at 3500 rpm on top of the substrate to achieve a thickness of 600 nm and undergoes a bake at 100 ºC for 60 seconds to remove the solvent in which the photoresist was in. The exposed pattern was a matrix of 23 by 23 crosses with the corresponding position number, each of them separated by 500 μm from each other. The exposure type was clear,

which means that the exposed sections are inside the shapes. Due to the fact that the photoresist is positive, after the development, the photoresist patterning is similar to trenches. The development is performed with AZ 400K 1:4 in a puddle development for 60 seconds. TiWN was deposited through magnetron sputtering with a duration of 62 seconds. The substrate holder of the machine is moving throughout the deposition in order to have a uniform deposition of the alloy.

The substrate was then placed on an acetone bath for 2 hours, in order for the photoresist beneath the film to be dissolved. An ultrasonic bath of 5 seconds was afterwards used to completely removed the film. The substrate was transferred onto another acetone beaker without letting the acetone dry on the surface and another ultrasonic bath of 1:30 minutes was performed to ensure the removal of any films that were not previously removed.

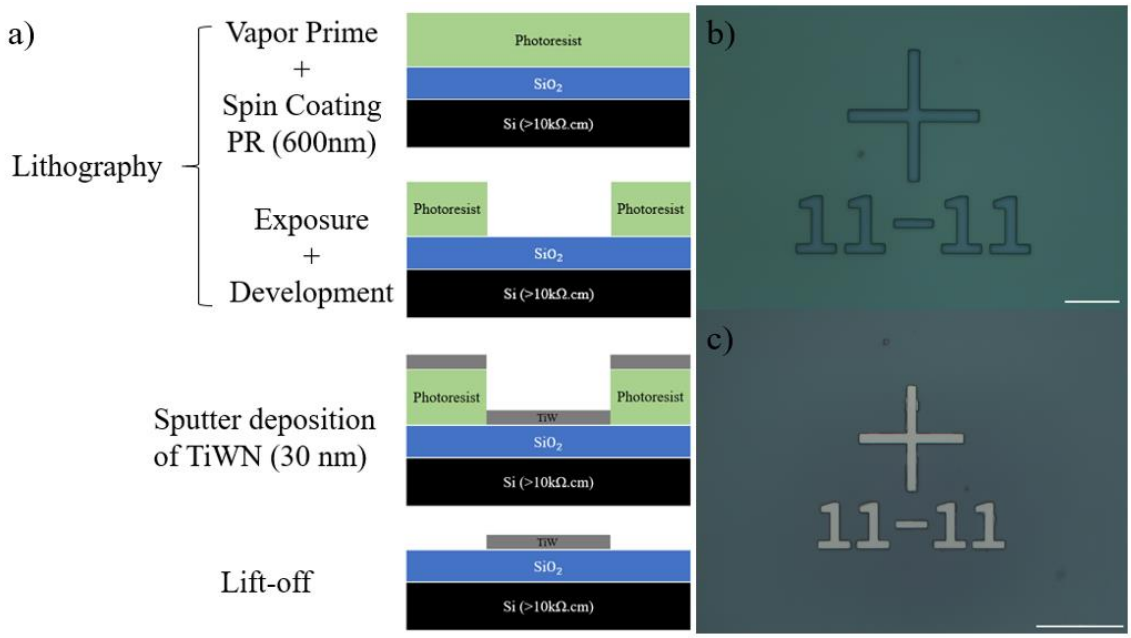

Figure 50: Optical markers matrix patterning. a) Cross-section schematic of the fabrication process flow. b) Optical image of the middle marker after development. Scale bar: 25 μm. c) Optical image of the middle marker after lift-off. Scale bar: 50 μm.

5.3.3 Graphene growth and transfer

Graphene is grown through a thermal chemical vapor deposition on a copper foil (Alfa Aesar, purity 99.8%), functioning as a metal catalyst. The copper foil is transferred to the CVD chamber and throughout the growth processes the temperature is stably kept at 1020 ºC. During the growth process, the gas mixture of hydrogen (80 sccm), methane (4 sccm) and argon (240 sccm) were introduced into the chamber where the reaction pressure was set at 6,5 Torr for a duration of 40 minutes. Graphene grows on both sides of the copper foil, and to allow its transfer for another substrate, PMMA is spin coated onto one side of the copper foil. The graphene on the back side is removed with an oxygen plasma step and the copper dissolved in a FeCl3 solution (0.5 M) for 3 hours. The sample is fished out of the solution and transferred onto a DI water beaker and left for 20 minutes. Afterwards, the sample is fished out again onto another beaker with clean DI water. The iron chloride (FeCl3) will leave Fe3+ radicals adhered onto the graphene. Since the intention of this graphene is to be used in electronics, these radicals have to be removed. Not removing them will cause the device to have a Dirac point in the 20-40-volt range. A solution of 2% HCl is used to remove this doping effect. After the doping balance, the graphene/PMMA substrate is fished out and placed on a DI water beaker for another 20 minutes. Lastly, the graphene/PMMA is fished out and transferred onto the silicon dioxide substrate and left for 12 hours to dry with the substrate placed vertically. After the transfer, the PMMA on top of the graphene is removed with an acetone bath of 12 hours followed by an IPA bath of 1 hour and DI water rinse and lastly blow dried with N_2 gun.

During the transfer, it was possible to see the delamination of the silicon dioxide layer. This was due to the thick layer of oxide deposited and the mechanism of deposition of this dielectric. By using a high frequency plasma, we obtain a better dielectric, however, the stress of this film is high and consequently, its delamination occurs when high thicknesses are deposited.

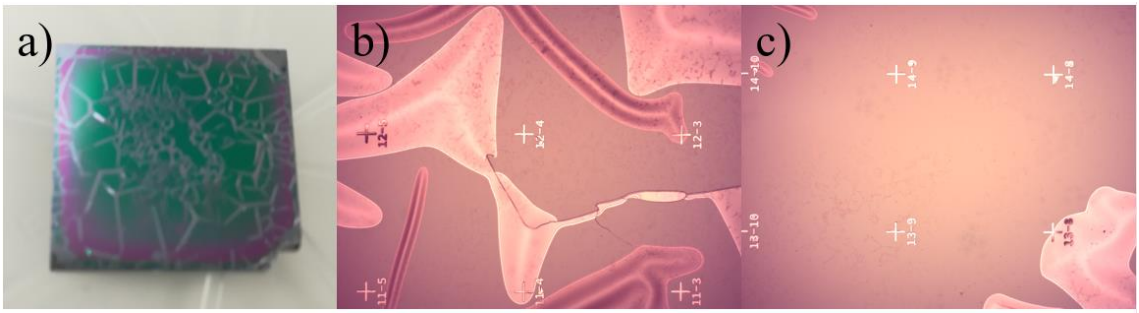

Figure 51: Optical images of the substrate after the graphene transfer. a) Top view of the overall substrate. b) and c) optical microscope images of two random areas of the substrate.

Raman spectroscopy was employed to assess the quality of the grown and transferred graphene. It was possible to see, from the results, that the graphene quality varied from the zones analysed, but overall, we were able to achieve monolayer, continuous and with small defects graphene sheet.

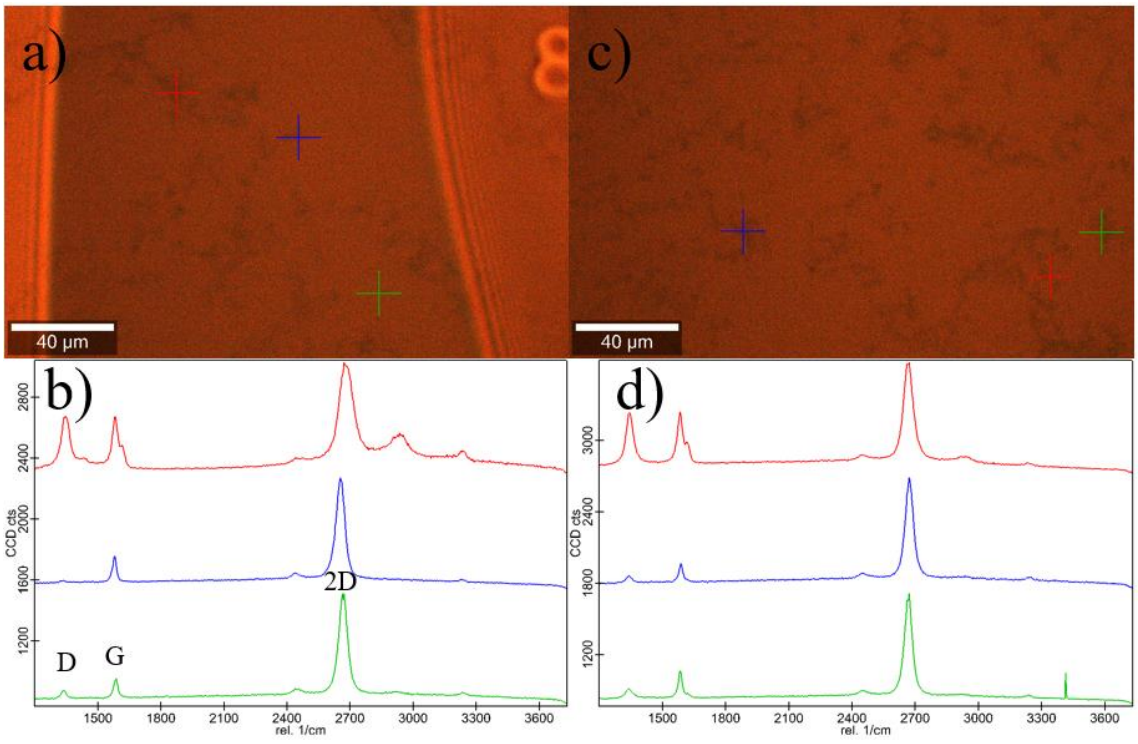

Figure 52: Raman characterization of the transferred graphene. a) and c) analysed sites. Scale bar: 40 µm. b) and d) corresponding Raman spectrums of a) and c), respectfully.

5.3.4 Core-shell nickel/nickel oxide nanowire transfer

Core-shell nickel/nickel oxide nanowires grown with the method described in the prior chapter and oxidised with the method described in this one, were drop casted onto the graphene. Beforehand, nanowire concentration per droplet was investigated, in order to only deposit a small number of nanowires. The method of investigation was by depositing a droplet of the solution with the nanowires suspended and observing its concentration. If needed, a dilution process would take place, and would be repeated until the nanowire concentration was the desired one. The desired concentration required the nanowires to be spread out when deposited on the substrate, not having two or more nanowires in the vicinity of each other.

After transferring the nanowires onto the substrate, optical images where the nanowires deposited were taken. These images were inserted into the AutoCAD program and with the assistance of the optical markers, these images were aligned, allowing for the drawing of masks for the remaining lithographic processes. It is worth noting that the delamination of the silicon dioxide substrate made this task harder and some result patterns were off due to this misalignment. For all intents and purposes, the devices 6-16 are going to be the ones followed throughout this section of the thesis.

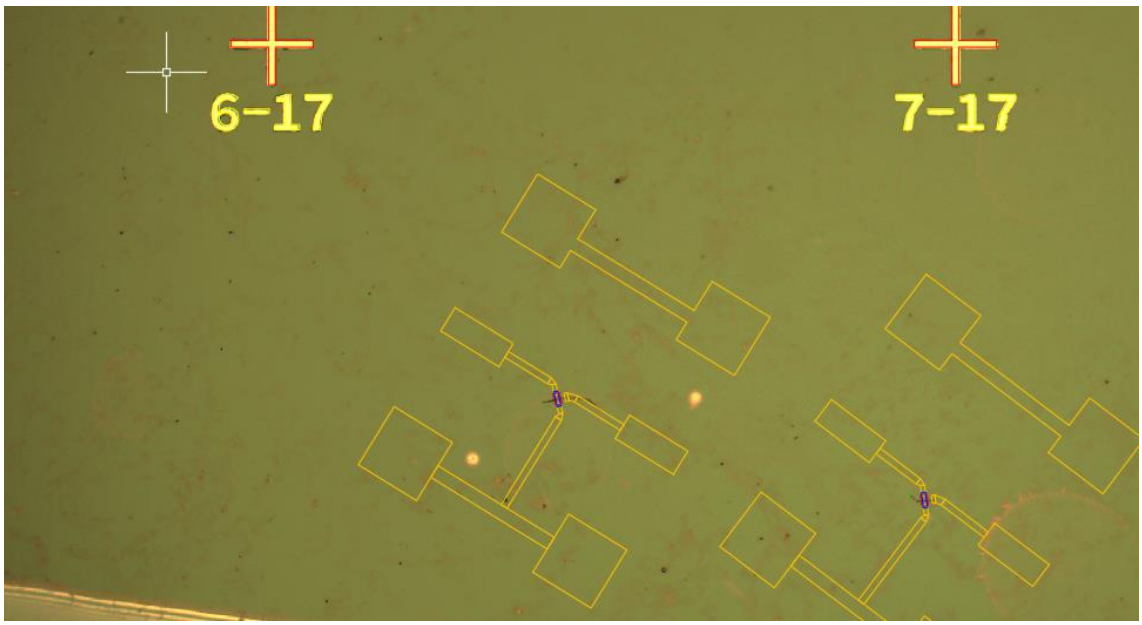

Figure 53: AutoCAD drawings with the overlaid image of the substrate containing the nanowires.

5.3.5 Channel Patterning

After the nanowire transfer, the excess graphene must be removed. For this reason, masks with 5 µm (channel width) by 8 µm were draw over the nanowire for the lithography. The lithography steps were the same as the previous ones, with a few exceptions. The photoresist thickness was increased to 1 µm as it will also be removed in the oxygen plasma process and to ensure it does not get removed completely. The exposure type was changed to dark as the process now is an etching one, requiring the material to be left on the substrate to be covered.

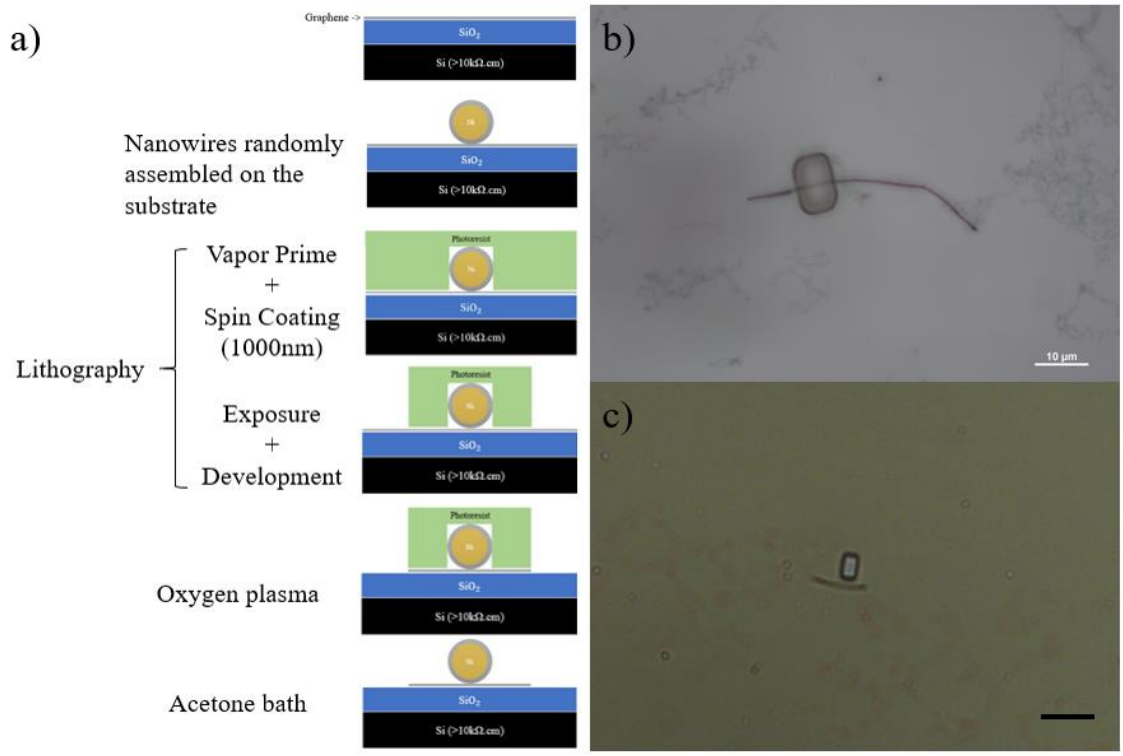

Figure 54: Channel patterning of the devices. a) Cross-section schematic of the process. b) Optical microscope image of device 6-16. Scale bar: 10 µm. c) Example of a misaligned lithography. Scale bar: 24 µm.

Afterwards, exposed graphene is removed with oxygen plasma with 250 W of power and a flux of oxygen and nitrogen without temperature control over a period of 4 minutes. To ensure that the graphene was removed, contact profilometer over a misaligned structure was employed, showing a decrease of 200 nm in the photoresist film, indicating that the graphene

was also removed. Raman characterization after the oxygen plasma steps showed no signal of graphene in the exposed section, which leads us to conclude that the process was successful. To remove the photoresist on top of the graphene channel, an acetone bath of 2 hours was employed. Afterwards, Raman characterization of the graphene channel of the device 6-16 showed graphene with minimal defects. However, the graphene signal possessed a continuous signal which bends the spectrum. This effect was attributed to photoresist not fully removed in the acetone bath process and on further iterations of the fabrication process, this bath duration should be increased.

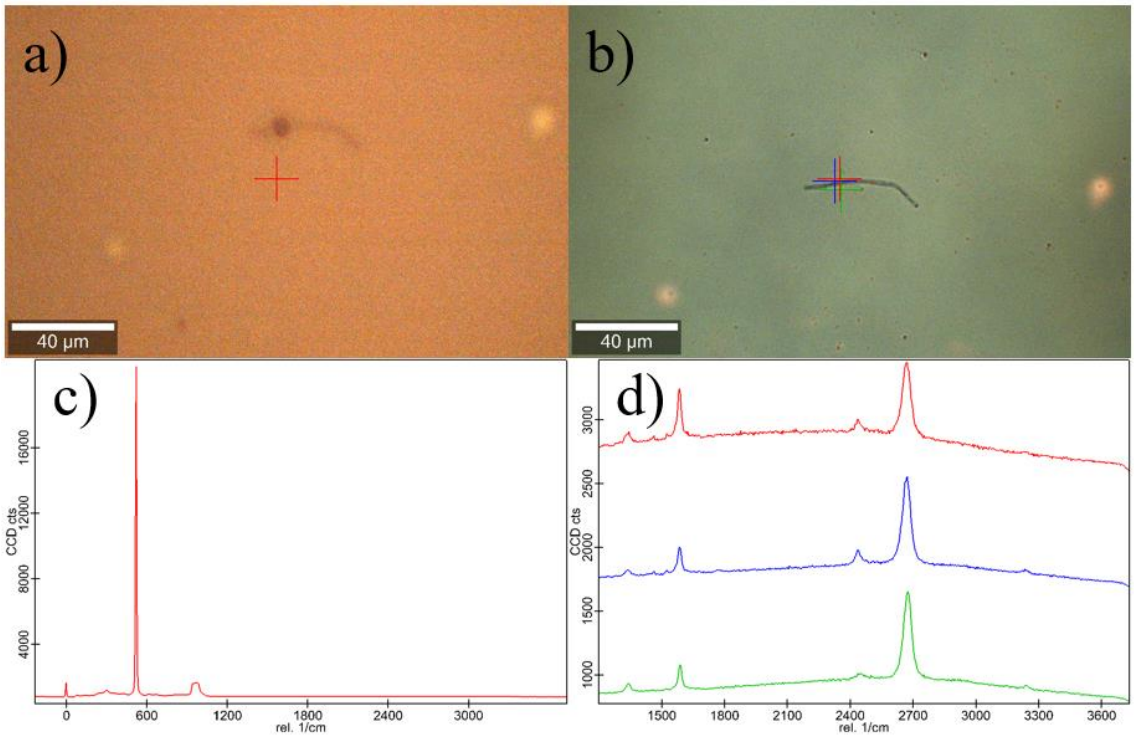

Figure 55: Raman characterization a) after oxygen plasma with corresponding spectrum (c) and b) after acetone bath with corresponding spectrum (d).

5.3.6 Self-aligned source-drain metal contacts

The self-aligned source-drain metal contacts were patterned with the assistance of a physical etching process. The metal stack of 3 nm of chromium (adhesion layer) and 30 nm of palladium was deposited, throughout the whole substrate, using a magnetron sputtering technique, followed by the lithography step. Due to a concern of graphene underneath the

nanowire not being removed in the oxygen plasma step, the metal chosen for this deposition had to be in the target rightly on top of the substrate. Upon checking the targets display in the machine, palladium fitted this description. Vapor prime, for the better adhesion of photoresist, spin coating of 600 nm of photoresist, dark type exposure and development patterned photoresist of our intended structure. Lastly, an ion milling step removed the chromium/palladium metallic film exposed. The ion milling machine possesses a feature of displaying the materials being removed from the substrate. The etch of the metals was stopped when the signal of chromium was vanishing and the overall etch time was 114 seconds. However, since the substrate has to be mounted on a wafer in order for the machine to be used, there is a poor heat transfer from the substrate to the wafer and consequently, the photoresist, used as mask, got burnt. Further steps of the fabrication process were not taken due to the unremovable burnt photoresist. On further iterations of the fabrication process this step has to be tweaked or altered. A different method of patterning metals should be used (i.e. lift-off assisted process), a wafer scale substrate to better dissipate the heat or partitioning the etch time to allow heat dissipation in between them are available alternatives for this process.

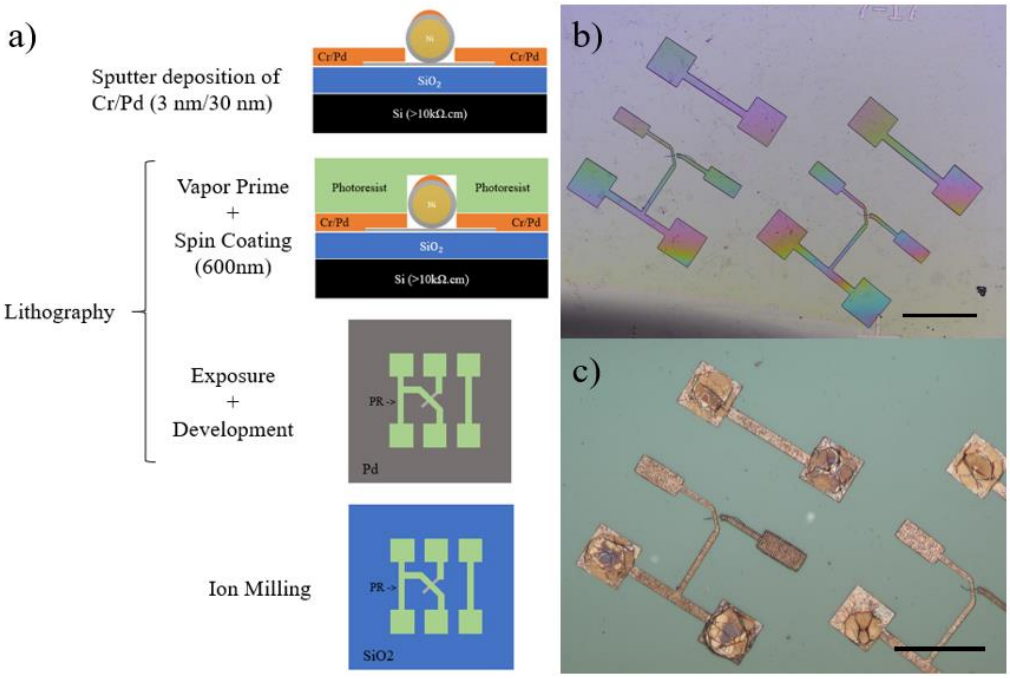

Figure 56: Self-aligned source drain metal contacts. a) Cross-section/top view schematic of the metal patterning. b) Optical microscope image of the device 6-16 after the development process. Scale bar: 100 µm. c) Optical microscope image of the device 6-16 after the ion milling process. Scale bar: 100 µm.

5.4 Characterization

Characterization of the devices was still pursued, in order to obtain information relative to the graphene resistance and the self-aligned process. Standard DC measurement probes were first used, in an attempt to measure the devices. These were unsuccessful as the pads were too small and easily destroyed by the probes. On further iterations of the fabrication process, these pad sizes will be bigger while having a protective layer on top such as TiWN. The RF probes were thus used to make the connection to the device pads and managed to pierce through the burnt photoresist and did not destroy the metal underneath.

A device where the nanowire was removed, served as a short measurement of the source-drain contacts. Characterization through current-voltage curves, gave a resistance value of 486 Ω. A device where there was a misalignment of the source-drain contacts lithography, served the purpose of measuring the metal contacts plus the graphene channel. Characterization of this device gave a resistance value of 690 Ω. With these two values, one can measure the resistivity of the graphene channel, thought the following equation:

$$\rho_{graphene} = R_{graphene} * \frac{W}{L} \tag{39}$$

Where, W and L are the channel dimensions. Graphene resistivity for this particular device is 2.06 kΩ$_{\square}$. This value, when compared to previous devices fabricated at INL [51] which the mean resistance was 650 Ω, is too high of a value. This is attributed to the unremoved photoresist in the channel patterning process, which could be seen in the Raman spectrum.

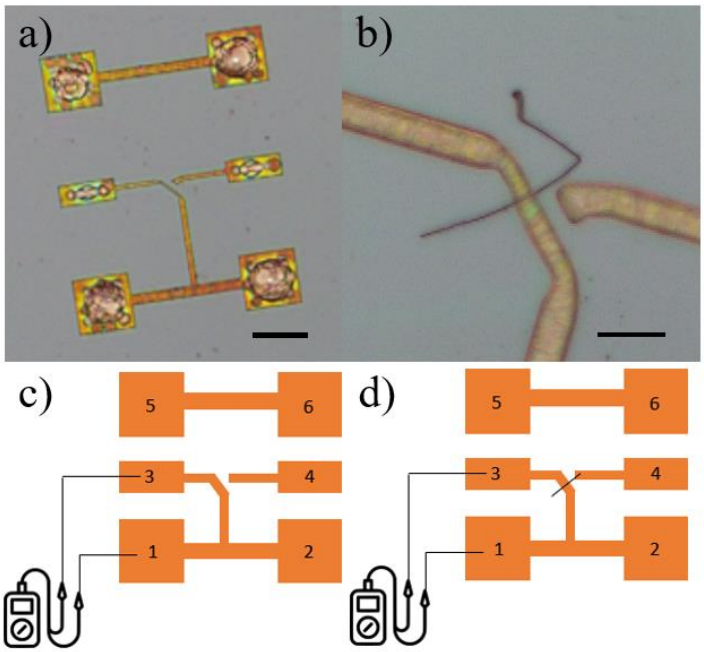

Figure 57: Resistance measurements of the device. a) Device with no nanowire and corresponding measuring set-up (c). Scale bar: 50 μm. b) Device with misaligned lithography step and corresponding measuring set-up (d). Scale bar: 10 μm.

On devices where the lithography steps worked properly, an attempt was made to measure the transfer curve of the transistor. Having in mind that, no oxide was removed prior to the metal deposition, only AC measurements would show any results. However, on all the devices measured, there was a low resistance between the gate and the channel. At first, this was thought to have come from the unetched graphene underneath the nanowire, but measures were taken to prevent this scenario. A closer look into the oxide shell, revelled that, this was in fact conducting current through it.

A dielectrophoretic process, which aligns the nanowires on top of two electrodes, was performed to better characterize the nanowire shell. The thought process was to perfectly place the nanowire between the electrodes, and then pattern a third structure on the middle of the nanowire and measure the current flowing through. On a typical dielectric, this current should be in the order of 10^{-9}, however, results show currents in the order of 10^{-3}, which is unacceptable in this type of devices.

For the dielectrophoretic process, the solution in which the nanowires were stored was changed from ethanol to DI water. This was due to the ethanol fast evaporation time and spread

throughout the substrate. The number of nanowires per droplet was also increased as the nanowires have to be in suspension when the droplet is placed on the substrate. When the droplet is placed, some nanowires adhere onto the substrate, others remain above surface level, unable to break surface tension, and some remain suspended in the solution. Since the probability of the nanowires being on either three of the previously mentioned state is random, increasing the nanowire count per droplet is a way to ensure suspended nanowires in the solution. Suspended nanowires align themselves with the imposed electric field and progressively come closer to the electrodes until they are connected.

Different frequencies and amplitudes of the applied AC signal were tested, and the results showed that the higher the frequency the more aligned the nanowires would be, while the higher the signal amplitude, the easier it is to connect the wires. A frequency of 1 GHz and an amplitude of 10 Vpp were used on this sample. Since the electrodes have a width of 2 µm over a distance of 0,5 cm, its resistivity is high, allowing for the use of high voltages for the nanowire placement without breaking the nanowire on contact.

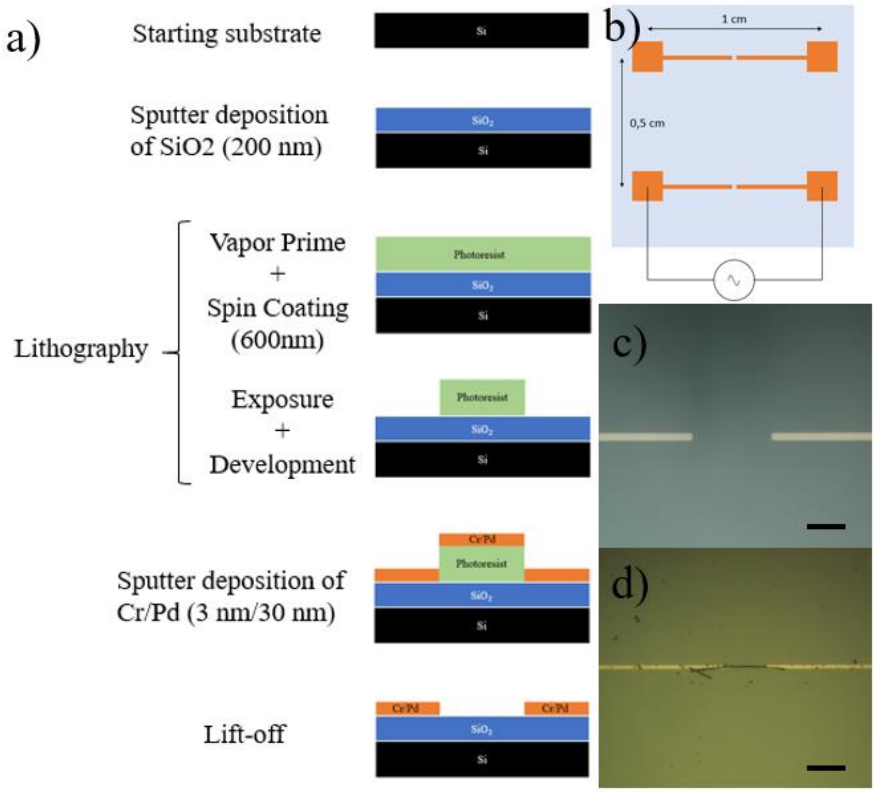

Figure 58: Dielectric assembly of nanowires. a) Cross-section schematic of the fabrication process flow of the electrodes. b) Top view of the structure. c) Optical microscope image of the ends of a pair of electrodes. Scale bar: 10 µm. d) The electrodes of c) with an aligned nanowire between them. Scale bar: 20 µm.

5.5 Conclusion

In this chapter, we tested a fabrication method for self-aligned graphene field-effect transistors. This process failed to deliver working transistors due to insufficient insulation obtained between the gate and channel of the device, derived from the selected dielectric material. Even though the fabrication process failed, relevant information was obtained about the method, to be used on further iterations of the process, the main one being the dielectric choice. Lastly, we tested a method of self-assembly of nanowires, which can be used for other application due to its versatility.

6 GRAPHENE FIELD-EFFECT TRANSISTOR WITH NICKEL/SILICON DIOXIDE CORE-SHELL NANOWIRE GATE

6.1 Introduction

In the previous chapter, the fabrication process of a graphene field effect transistor with a nickel/nickel oxide core-shell nanowire gate was presented alongside each part that could be improved. In this chapter, a similar fabrication method to the previous one will be presented considering the improvements proposed in the previous.

6.2 Silicon dioxide shell

The main flaw of the previous fabrication process was the gate dielectric material chosen. In this iteration, nickel nanowires were coated with SiO_2. Several different methods of dielectric deposition were proposed. However, dielectric characterization was still a present issue.

Dielectric deposition onto the nanowires while they were still attached to the seed layer was the most convenient method. However, and as shown before, nickel malleability and subsequent aggregation the nanowires invalidate this method. Even though, this method seamed unreliable, several attempts were made and showed promising results.

Nickel nanowires were grown with the set-up shown in chapter 4, under a constant current of 2 mA for 2 hours. After the template dissolution, a section of the metal seed layer was etched and the nanowires released, showing a length ranging from 19 μm to 23 μm. Another piece of the seed layer was duck taped onto a silicon dioxide substrate and SiO_2 was deposited through PECVD with an intended thickness of 15 nm. SEM analyses of the resulting structure shows the nanowires coated with lighter shade material, assumed to be SiO_2 and confirmed through EDX measurements. However, only the top section of the nanowires could be seen, and we

were unable to confirm full deposition of the material on the inner sections of the substrate. SEM analyses of the nanowires, after release from the seed layer, and compared to bare nickel nanowires, showed no difference, proving once again the poor characterization technique.

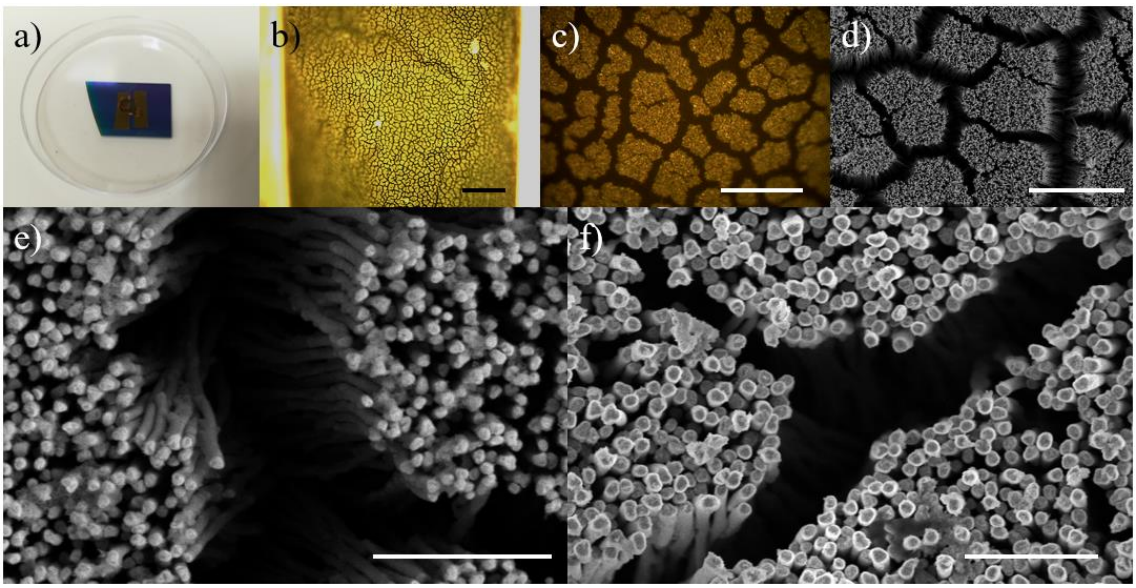

Figure 59: Dielectric deposition of SiO_2 onto nanowires still attached to the seed layer. a) Optical image of the seed layer duck taped to an SiO_2 substrate before deposition. b) and c) Close-up optical microscope image of a). Scale bar: 120 μm and 30 μm, respectfully. d) and e) SEM images of the nanowires before SiO_2 deposition. Scale bar: 20 μm and 4 μm, respectfully. f) SEM image of the nanowires after SiO_2 deposition. Scale bar: 3 μm.

A different technique was employed, where the nickel nanowires were deposited onto a silicon dioxide substrate and the dielectric material deposited afterwards. With this method we guarantee the partial oxidation of the entire length, except for the section in contact with the substrate. After the oxidation, two distinct methods of nanowire transfer can be used. Either through contact printing, where the substrate containing the nanowires and the substrate containing the graphene are merged and the nanowires transferred or using ultrasounds to remove the nanowires from the first substrate to an ethanol-based solution and then drop casting them into the graphene. In the first method, there is a certainty that the dielectric material is facing the graphene, however, this process would destroy the graphene sheet and render it useless for device fabrication. On the other hand, the second method has a few draw backs as well. There is no guarantee that the nanowires, when drop casted onto the graphene, will have the dielectric material facing the graphene and in order to perform the ultrasounds, a large

amount of solution has to be used, significantly reducing the nanowire concentration per droplet.

6.3 Fabrication

In this fabrication process, the starting substrates used are the same as the ones used in the first run, highly resistive silicon (> 10 kΩ.cm) with 2 cm by 2 cm in size. Even though, in the previous chapter, it was stated that by using a larger substrate that could better dissipate heat so that photoresist would not burn, this solution was not available. To solve this problem, the physical etch process was exchanged, when possible, by a lift-off assisted process.

6.3.1 Passivation layer

The first modification, in the fabrication process, was the passivation layer thickness. In the previous run, this layer possessed a thickness of 1 μm and started to delaminate halfway through the fabrication process. For this reason, in this one, this thickness was reduced to 300 nm and deposited with the same recipe as the previous one and no delamination was seen throughout the fabrication process.

6.3.2 Matrix of optical markers

Similarly, to the previous fabrication process, a matrix of optical markers was required. These, however, were fabricated with a physical etch process instead of a lift-off process, because we intended to measure the graphene resistance after patterning. Because TiWN is a hard material and difficult to remove, the total etch time was 138 seconds which consequently burned the photoresist. A process of oxygen plasma followed by a resist strip with Microstrip

assisted with ultrasounds were used in an attempt to remove the photoresist. Since these were optical markers there was not much concern with the burnt photoresist on top of them. However, the graphene resistance measurement devices, left with residues of photoresist, became useless as the graphene resistance measurements, after patterning, showed only open circuits.

The intended structures had to be pattern through ion milling due to the slope that it creates between the top section of the film and the substrate, if an angle is applied to the process. Graphene transferred to these structures will follow the slope of the structure, lowering the likelihood of breaking due to the smooth interface between the two levels.

A thickness of 20 nm of TiWN was deposited through magnetron sputtering in the same conditions as in the first fabrication process. The lithography process followed the same steps as the previous fabrication apart from the mask. Dark type exposure was used in order to cover the material not intended to be removed. Ion milling followed with an etch time of 138 seconds, time required for the signal of the material to vanish. Lastly, the processes of oxygen plasma and resist strip were used to remove the residues of photoresist.

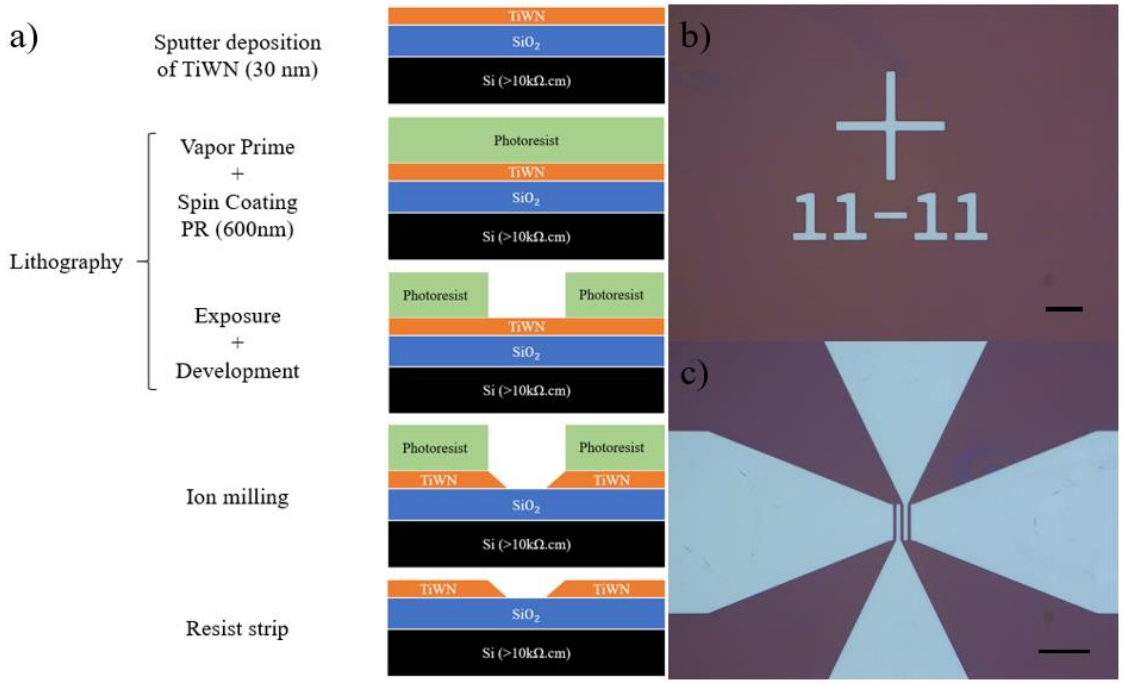

Figure 60: Patterning of the matrix of optical markers. a) Cross-section schematic of the fabrication process flow. b) Centre optical marker after the resist strip process. Scale bar: 20 µm. c) Graphene resistance measurement device after the process of resist strip. Scale bar: 30 µm.

6.3.3 Graphene growth and transfer

Graphene growth and transfer were performed in the exact same manner as the previous fabrication process. Grown on a copper foil and transferred with the assistance of PMMA, after the dissolution of PMMA, the graphene synthesis and transfer are completed. The transferred graphene, however, showed some discontinuities on some of the regions, which later on, delaminated even further. Raman spectroscopy of the transferred graphene shows, aside from the teared parts, continuous monolayer graphene with minimal defects.

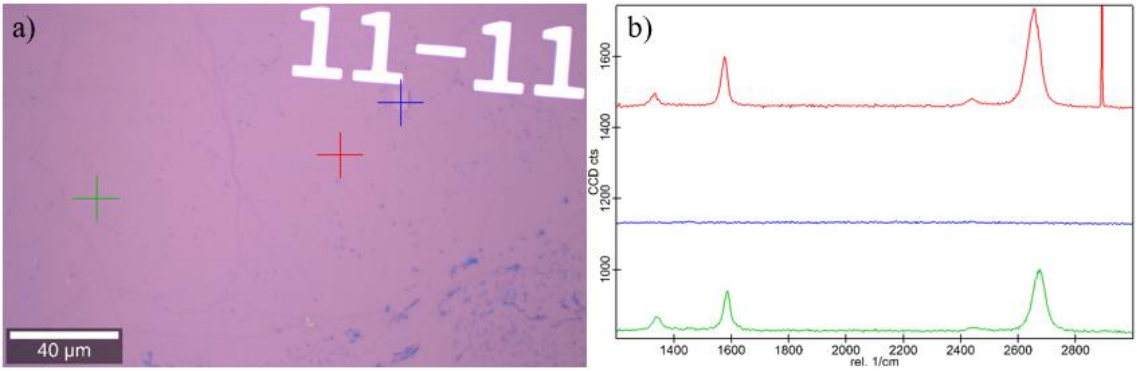

Figure 61: Characterization of the transferred graphene. a) Raman spectroscopy sites. Scale bar: 40 µm. b) Corresponding Raman spectrum.

6.3.4 Core-shell nickel/silicon dioxide nanowire transfer

Core -shell nickel/silicon dioxide nanowires, synthesised through the method explained previously, were on a small concentration in the ethanol-based solution. Concentration of nanowires was below 1 nanowire per 15 µL of solution which substantially increased the number of droplets required to transfer the nanowires. An unknown reaction took place, when the droplets were drop casted onto the graphene which turned the surface green. This had been seen before but we were able to remove it with a simple wash of the substrate. However, since in this run, the graphene possessed discontinuities, these were spots were the graphene could delaminate even further. A possible explanation of this unknown material was a poor wash of the gold etch solution. To better assess the nature of this material EDX spectroscopy was

performed in an area where an increase in this effect could be seen. However, the only peaks showing in the results were the silicon and oxygen, resulting from the substrate, and carbon. No peaks of gold, iodine and potassium (i.e. gold seed layer and chemicals of the gold etch solution) were found in the spectrum, leading us to the conclusions that this effect came from a reaction of ethanol. Another side effect of the low concentration of nanowires was the number managed to drop cast into the solution, only being able to transfer 4.

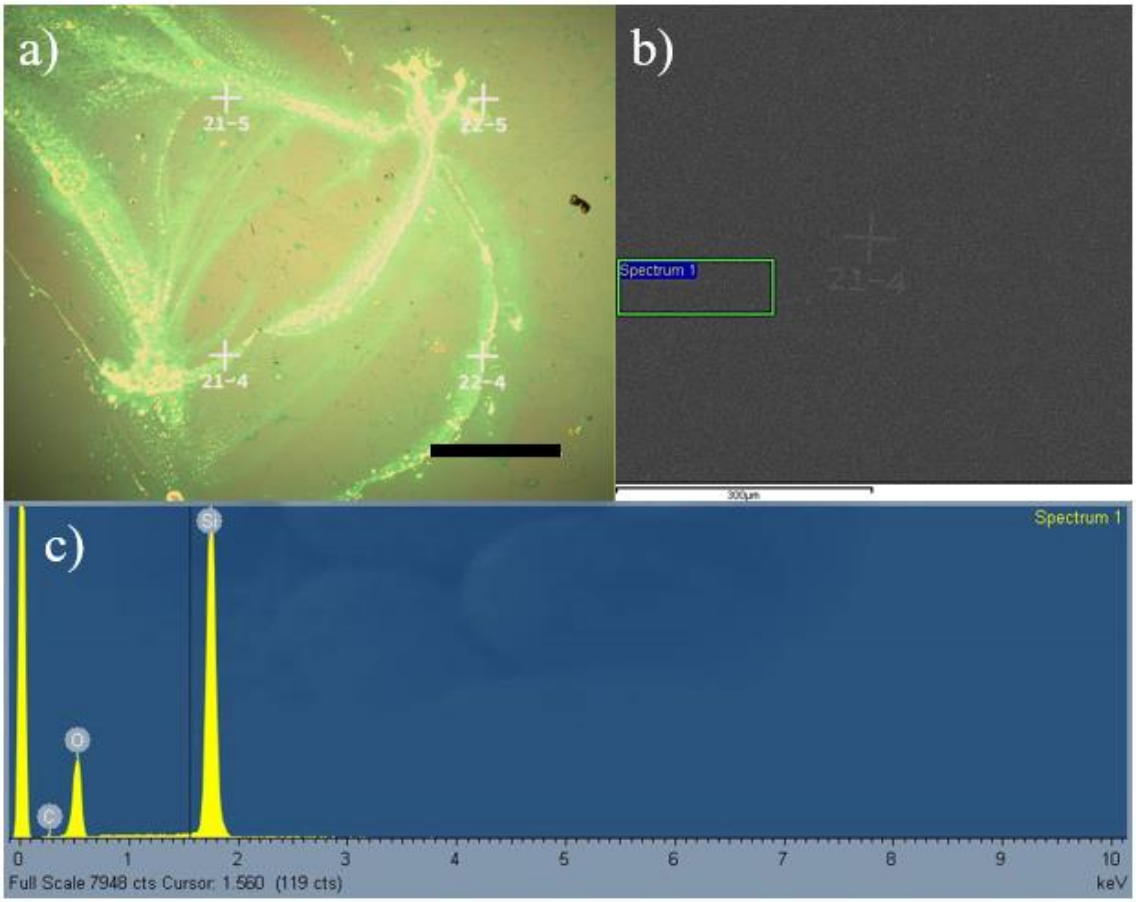

Figure 62: Characterization of the unknown material. a) Optical image showing the effects. Scale bar: 250 µm. b) SEM image showing the stop for the EDX spectroscopy. Scale bar: 300 µm. c) EDX results of the spot in b).

In an attempt to remove this material a gentle wash was performed where the substrate was left 30 minutes in acetone, 30 minutes in IPA, 30 minutes in DI water and gently blow dry with the N_2 gun. Significant reduction of this effect was seen, however, further delamination of the graphene was also seen. For this reason, no further attempts of washing were performed on this substrate.

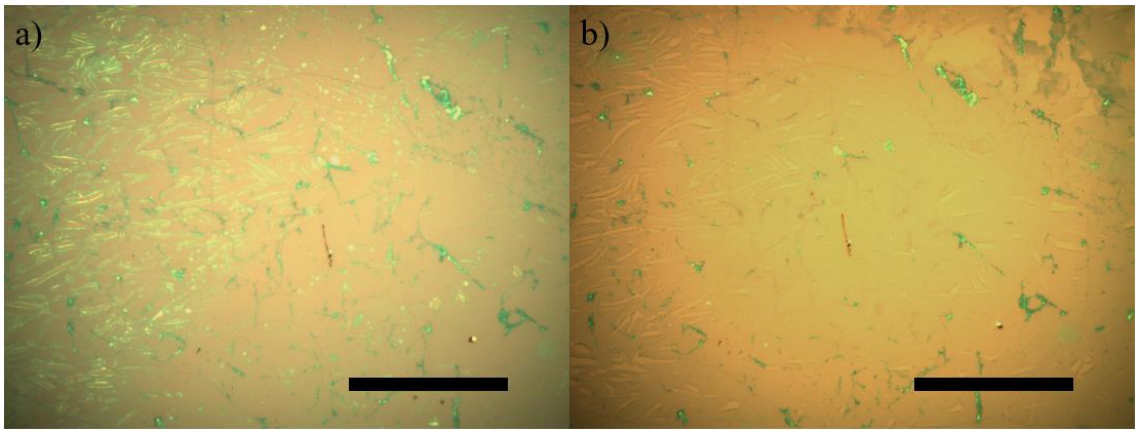

Figure 63: Optical images of device 21-4 before a) and after b) cleaning process. Scale bar: 60 μm.

6.3.5 Channel Patterning

Channel patterning was performed in the same manner as the previous fabrication process. Optical images of the 4 nanowires and subsequent masks were produced followed by the standard lithography steps. Vapor prime, spin coating, exposure and development defined the mask for the graphene channel (Figure 64). Oxygen plasma removed the exposed graphene and an acetone bath of 12 hours exposed the graphene channel. Raman spectroscopy of the graphene channel, when compared to the previous fabrication process, shows no bends in the signal, further validating that the bend was produced by the unremoved photoresist. The Raman spectrums also show continuous graphene with minimal defects.

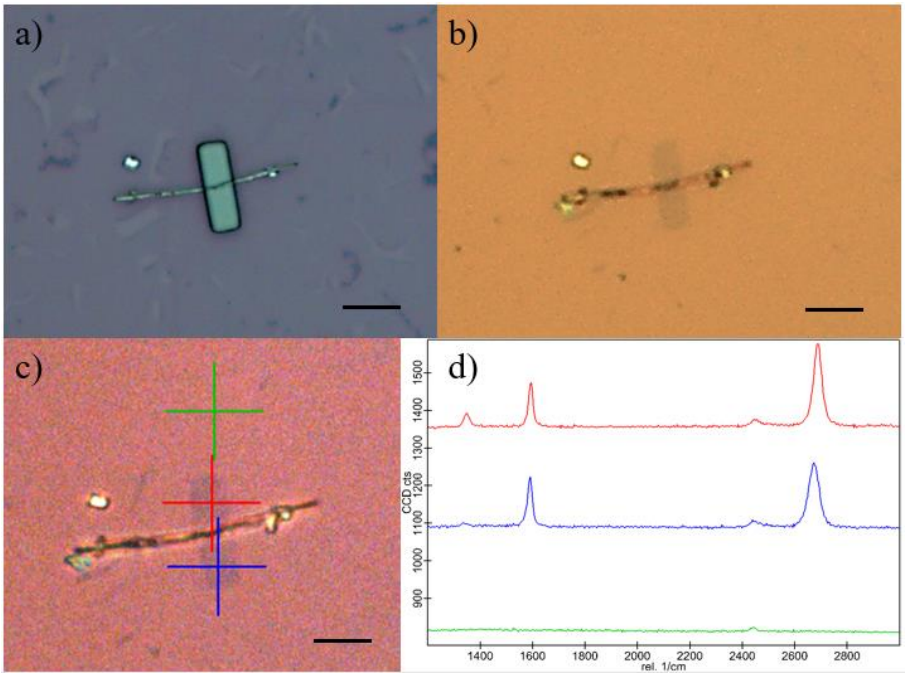

Figure 64: Channel patterning and subsequent graphene characterization of the device 3-11. a) Optical image after development process. Scale bar: 6 µm. b) Optical image after removal of photoresist. Scale bar: 6 µm. c) Raman spectroscopy sites. Scale bar: 5 µm. d) Corresponding Raman spectrums.

6.3.6 Self-aligned source-drain metal contacts

Source-drain metal contacts were patterned, in this fabrication run, with a lift-off process instead of the physical etch through ion milling, which caused the photoresist to burn in the last iteration. Palladium was exchanged by a more conductive material, gold, while chromium remained as the adhesion layer with a thickness of 3/10 nm. The thickness of the film was reduced due to the exchange in the fabrication method, as thinner layers are easier to remove than thicker ones. Standard lithography was used starting with vapor prime, spin coating of 1 µm to assist in the process, a clear type exposure and development patterned the photoresist with the intended mask. The chromium/gold metals were then deposited through magnetron sputtering and an acetone bath of 18 hours was employed to dissolve the photoresist. Afterwards, a plastic pipette was used to assist in the lift-off process providing a flux to the

substrate, as the ultrasounds, frequently used for these types of processes, would remove the graphene and the nanowires. Optical images after the process showed that parts of the metal film deposited on the surface possible creating shorts between the contacts.

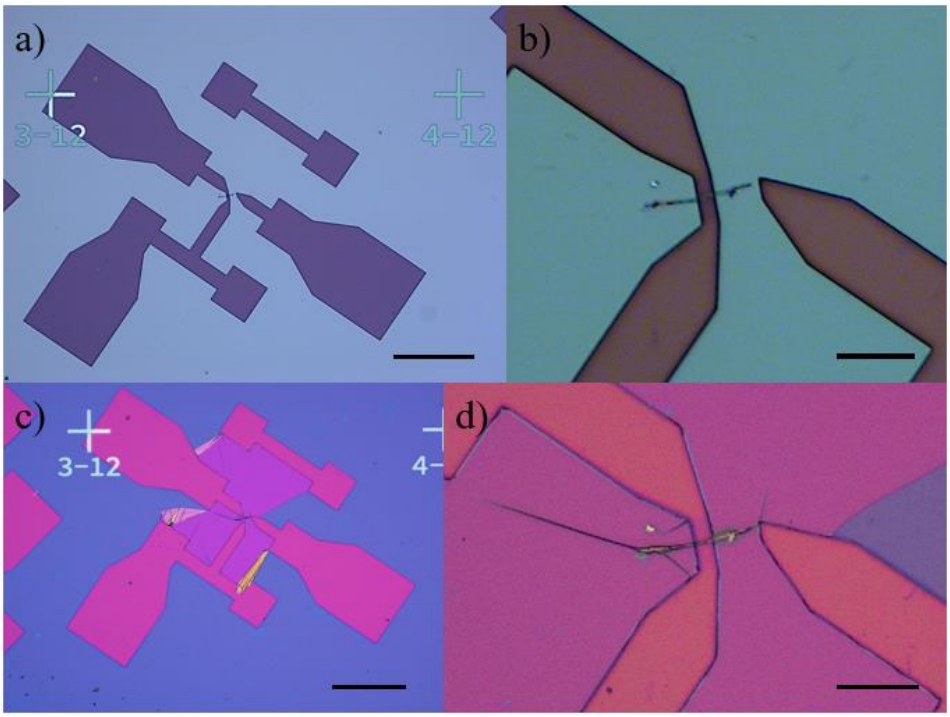

Figure 65: Self-aligned source-drain metal contacts of device 3-11. a) Optical image of the device after development and amplified image of the nanowire b). Scale bar: 100 μm and 15 μm, respectfully. c) Optical image of the device after lift-off and amplified image of the nanowire d). Scale bar: 100 μm and 15 μm, respectfully.

In an attempt to remove these films, a physical etch through ion milling was used. Lithography using the same mask as the one prior was used with the exposure type inverted, meaning that after the lithography, the devices were covered with photoresist. Ion milling was used to remove the exposed films, however these were not large enough to create a signal to be seen by the machine so the etch time had to be calculated. This ion milling process was also used for opening up a via to the core of the nanowire to enable a metal connection. Etch rates given for SiO_2 and Au were 16.67 nm/min. and 33.33 nm/min., respectfully. The thickness of SiO_2 film to be removed was the one deposited on the nanowire as a shell, 15 nm, and the thickness of gold to be removed was the deposited 10 nm. Chromium did not factor into the calculations as it easily oxidizes and ceases to conduct. The values of etch of each material were added and as a safe measure, 20 % of the total etch number was added to ensure full removal of the materials, resulting in an etch time of 84 seconds. The ion milling process, which in the

previous attempts managed to burn the photoresist, was used in a different manner. The etch time was divided into 3 equal sections with 7 minutes in between them, in order to let the substrate, cool down. However, even with this measure, photoresist on top of the device got burnt.

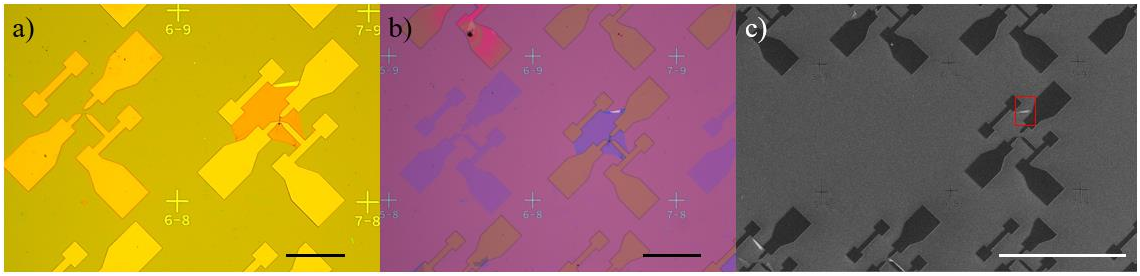

Figure 66: Physical etch of the unremoved gold film in the lift-off process. a) Optical image after development process. Scale bar: 200 µm. b) Optical image of the same site as a) after ion milling. Scale bar: 200 µm. c) SEM image of the same site as a) after ion milling and the red square showing unremoved gold layer. Scale bar: 500 µm.

Comparing the optical and SEM image, after the ion milling process, it is clear to see that the different shades in the exposed areas are just different thicknesses of SiO_2. However, a lighter shade can also be seen in the exposed zones. These are parts of the gold film that rolled on itself and subsequently possessed a higher thickness, thus not being removed in the ion milling process. EDX was employed (not shown) to characterize each zone and proved the assumptions made previously.

In order to remove the burnt photoresist, several attempts were made. In a first attempt was an acetone bath of 3:30 hours. This step had no severe impact on the photoresist film however.

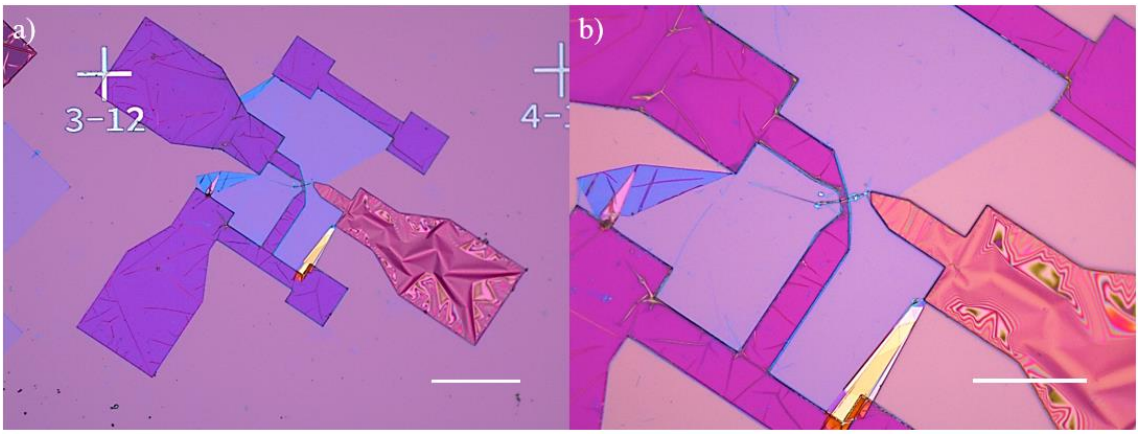

Figure 67: Optical images of the device 3-11 after the acetone bath. Scale bar: 100 μm and 50 μm, respectfully.

Afterwards, Microstrip was used. Microstrip manufacture advises, in its run sheet, heating it up to 60ºC to 90ºC for added effect on burnt photoresist. The process was performed in 80ºC but after 10 hours minimal changes occurred, so a plastic pipette, to provide a flux against the substrate, was employed. 20 more hours in the heated Microstrip bath ensued with the flux being created every 30 minutes. At the end of the 20 hours, it was visible that some parts of the gold film started tearing, so the process was stopped. However, a thin layer of residues was still seen on top of the devices, which later on will have an impact on the device's performance.

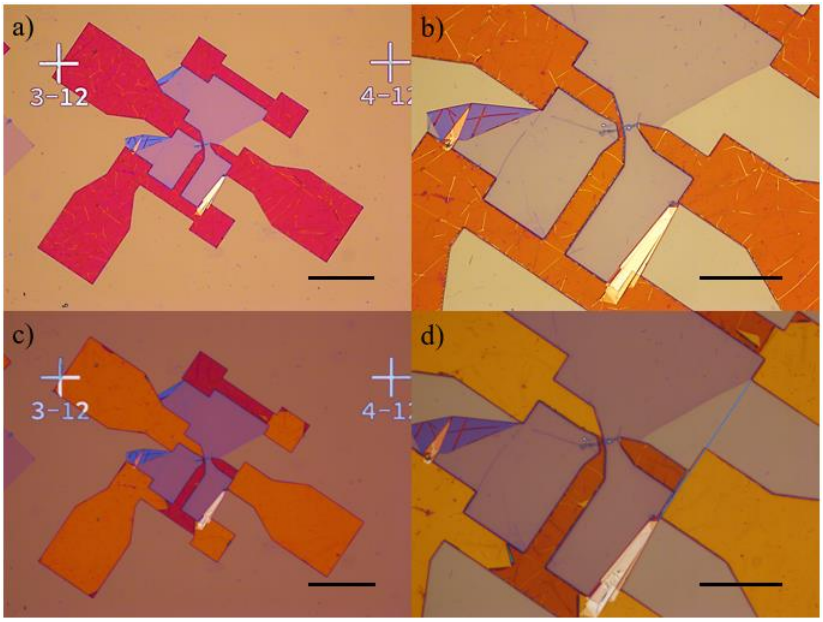

Figure 68: Removal attempts of the burnt photoresist on device 3-11. a) and b) Optical images after 10 hours in the heated Microstrip bath. Scale bar: 100 μm and 50 μm, respectfully. c) and d) Optical images after 20 hours in the heated Microstrip bath with pipette flux. Scale bar: 100 μm and 50 μm, respectfully.

6.3.7 Core connecting contact

The last step of the fabrication process consists in the deposition of metal stack, which not only thickens the already existing contacts but also connects the gate pad to the nanowire core. The metal stack, deposited through magnetron sputtering, consisted of 5 nm of TiWN, to serve as adhesion layer, 100 nm of AlSiCu and another 5 nm of TiWN to prevent the oxidation of the AlSiCu. The metal stack patterning was assisted with a lift off process. The same lithography steps as before were used, where a 1 µm thick layer of photoresist was patterned with a clear type exposure. Afterwards, the metal stack deposition took place followed by an acetone bath f 18 hours where the substrate was left vertically. The vertical placement of the substrate was to ensure no deposition of the metal film on the substrate took place. The lift off process was assisted with flux from the plastic pipette, which in this lift off process, achieved the desired results.

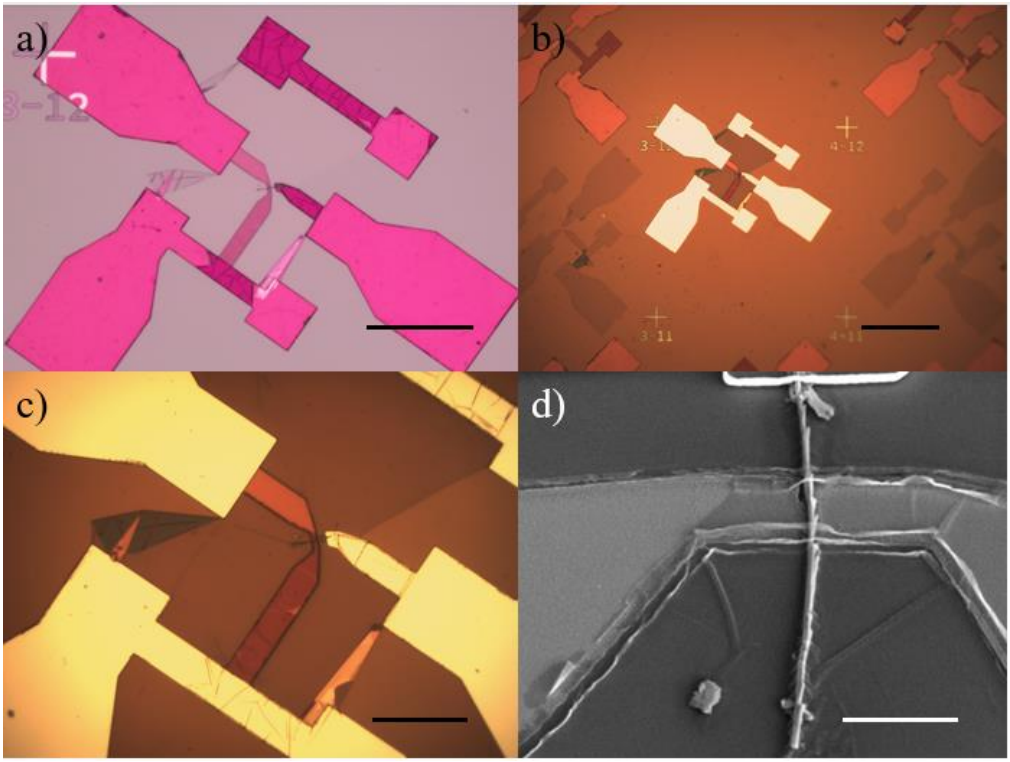

Figure 69: Patterning of the core connecting metal stack of the device 3-11. a) Optical image after development step. Scale bar: 100 µm. b) and c) Optical image after the lift off process. Scale bar: 200 µm and 50 µm, respectfully. d) Close-up SEM image at 40º of the nanowire. Scale bar: 5 µm.

6.4 Characterization

The devices fabricated, when compared to the previous, had enhanced size measurement pads. In the previous fabrication process, the devices when attempted to place the DC probes were completely removed as the material and thickness would not withstand. By enlarging these pads and placing a hard material on top (TiWN), we were able to make the connection. However, due to the photoresist residues still left in between the gold layer and the metal stack, the contact resistances of the devices were greatly increased. Furthermore, connections made initially onto the devices, after removing and placing the probes back in the device, were lost. This made the characterization of the devices impossible as only the first measurements were able to be made. Out of the four devices, on three of them we were able to measure the graphene resistance, possessing values of 38 kΩ, 1,7 MΩ and 17 GΩ. These values, in and on themselves are unacceptable for these types of devices as the cut-off frequency and maximum oscillating frequency depend on these. No further attempts were made to characterize these devices, as stated before, connections onto them seemed impossible to establish after the first one.

6.5 Conclusions

Another fabrication attempt with the physical transfer of core shell nanowires was performed taking into account the flaws of the previous one. A different dielectric was chosen with a subsequent different deposition. While attempting to avoid the ion milling process, which in the previous fabrication process rendered the devices useless, this was impossible as the lift-off process did not render the results desired. Although the first lift-off process did not succeed, the second managed to achieve perfect results implementing a new strategy. Although, no working devices were able to be achieved, this fabrication run presented new flaws and new solutions for the fabrication of graphene field-effect transistor with physically transferred core-shell nanowire gate.

7 CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

Graphene is seen as a potential enabler of future electronics. Due to its outstanding properties it can be used in a multitude of applications that range from biomedical, due to its sensing abilities, to radio-frequency applications, due to its electronic properties.

In this work, literature review was firstly performed to better understand the devices fabricated to date and its compatibility with the available tools for the author. Several different fabrication methods that provide field-effect transistors operating in the gigahertz range were discussed and a physical transfer of a core-shell self-aligned process of the fabrication method chosen.

Modelling of the physical structure took place to better understand how the physical parameters influenced the devices figures of merit. From the simulations, the proposed structure showed that devices could operate in the gigahertz range and a set of physical parameters for the structure, possible to fabricate with the available tools, was proposed.

Nickel nanowires were electrochemically grown with the assistance of anodized aluminium oxide templates. Synthesised nanowires had lengths of 20 to 50 microns and diameters ranging between 200 and 400 nanometres. A dielectrophoretic process was also developed, parallel to the remaining of the dissertation, in order to precisely placed the grown nanowires and further characterize them.

Two iterations of the fabrication process were performed. The first fabrication process used nickel/nickel oxide as the gate and gate dielectric, but it was later found that nickel oxide provided poor isolation between the gate and channel and the devices fabricated did performed as usual field-effect transistors. Due to the nature of graphene and the nanowires, ultrasounds could not be used in the fabrication of the devices. This alone difficults the fabrication process as pattern of structures assisted by a lift-off process was a liability. Physical etch was then used to replace the lift-off process, however this process would in turn burn the photoresist on top of the structures and its removal was nearly impossible.

The second fabrication took into consideration the flaws of the first one, and solutions for each were presented. By exchanging nickel oxide with silicon dioxide, the problem of poor isolation was resolved. The pattern of structures, however, had to be performed through a lift off assisted process and in the first metal deposition several pieces metal adhere onto the surface. To remove these, we had to resort back into the physical etch of the materials. Precautions were taken to avoid the heating of the substrate and subsequent burnt of the photoresist on top of the intended structures. However, the photoresist still got burnt but not as much as in the first fabrication process. Several processes were performed to remove this photoresist such as an acetone bath and microstrip with the assistance of a flux provided by a plastic pipette. Severe improvement of the structures was obtained, but it was shown later on in the process that metal contacts deposited on top of the devices had poor electrical connection onto it. The last patterning of metals was assisted by a lift-off process and the results achieved were the desired ones. Characterization of these devices, as stated prior, were made impossible due to the lack of electrical connection. Only the resistance of graphene was retrieved, however, these results were influenced by the left-over photoresist on the structures.

7.2 Future Work

Several solutions were proposed throughout the fabrication process to overcome the flaws resulting from the processes used. The use of the physical etch to patterned the structures was successfully exchanged by the lift-off assisted one through the use of a flux by a plastic pipette. These small increments are to be implemented on further iterations of the fabrication process.

The use of the anodized aluminium template with the distance between the pores so close to each other is that can be adjusted. By utilizing a template with large pore distance, it is possible to achieve, after the template dissolution, nanowires standing straight and not aggregated, which in turn would enable the dielectric deposition throughout the entire structure.

Different types of templates can also be considered. By altering the shape of the pores, different types of geometrical shapes can be achieved. Shapes, such as triangular nanowires,

when deposited on the graphene, will have a larger area of contact which in turn increases the gating effect of the transistors, allowing for higher value of the figures of merit.

Different types of metals can also be deposited using the same set-up as the one used in this work. Although the nickel nanowires have a small resistance, metals such as gold and silver, which have lower resistivity values, would translate to an even lower resistance for these structures.

The gate dielectrics attempted in this work were nickel oxide and silicon dioxide. It was shown that nickel oxide does not meet the requirements for these types of devices and silicon dioxide has a small dielectric constant, which influences the gating effect of the channel. By exchanging these for higher k oxides, such as Al_2O_3 and HfO_2 which possess k values of 10 and 22, respectfully, the gating effect would increase and subsequently the values of the figures of merit. ALD deposition of these materials would also allow control over the dielectric thickness. As shown by the simulations the lower the thickness of the dielectric the higher the gating effect and subsequently higher the values of the figures of merit.

The dielectrophoretic process developed in this work can also be used to scale up the fabrication process. By combining the fabricated structures with microfluidic, precise placement of several nanowires can be achieved and enable the fabrication of RF circuits.

Other different types of fabrication processes can also be experimented with. One such example is the buried gate approach. Patterning of the contacts is firstly performed with the assistance of the Damascene process and only after is the graphene transferred. Gate contacts, while buried, can extend further into the substrate and in turn reduce its resistance. This process also opens up the possibility of the dielectric deposition be performed through sputtering, as it is not directly onto the graphene sheet.

Another fabrication approach revolves around the traditional top gated devices. By exchanging the PMMA, in the graphene transfer process, by a layer of chromium and gold, direct contact to the as grown graphene has shown lower contact resistances. Gold can be etched with the etchant solution used in our process nanowire release and thus enabling a wet etch method to be implemented in the fabrication process. Chromium when exposed to air quickly oxidizes into chromia, which is an insulator. This can be used in the same way as the polymer buffer layer to shield the graphene from the dielectric deposition. Having the chromia between the graphene channel and the dielectric will have the same as the polymer, which reduces the gating effect of the top gate. However, it has been shown in literature that chromia has a

dielectric constant similar to that of the Al_2O_3. Top-gated field effect transistors can thus be developed and further improvements such as T-shaped gates can also be experimented upon.

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