Efficiency Comparison of a dc-dc Interleaved Converter Based on SiC-MOSFET and Si-IGBT Devices for EV Chargers

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Abstract— **The charging process is one of the main factors for the widespread dissemination of electric mobility, therefore, the use of optimized power electronics converters is of utmost importance. In addition to innovative topologies, the use of emerging technologies of semiconductors is also crucial. In this context, using a three-phase interleaved dc-dc topology, a comparison between the use of SiC-MOSFET and Si-IGBT is presented in this paper, mainly in terms of operating efficiency. Two cases have been presented: 1) with the same inductor, where only power device losses have been considered; 2) with the same inductor current ripple, where different inductors have been considered and the analysis included also the inductor design and losses. The simulations were carried out in LTspice simulation tool on realistic dynamic models of power switch modules obtained from the manufacturer's experimental tests. The results validate the use of SiC-MOSFET for the three-phase interleaved dc-dc topology showing lower losses for both the power devices and inductor and, most important, prove the advantages of its use in terms of efficiency for a wide range of operating powers.**

Keywords— SiC-Mosfet, Efficiency, Interleaved dc-dc Converter, EV chargers.

I. INTRODUCTION

Electric mobility is expanding its engagement in the transportation sector, offering several technologies prospecting the sustainability of this area [1], not only in the perspective of the vehicle, but also in the perspective of the power grid [2][3]. Moreover, the cooperative mixture with renewables prospecting power management for the power grid side can also be seen as a key challenge offered by the flexibility of the electric mobility in terms of random connection to the power grid [4][5]. In this context, the incorporation in the paradigms of microgrids [6], smart grids and smart cities is of paramount importance [7]. Among the different technologies, the most emblematic is the plug-in battery electric vehicle (EV), reflected by the models commercially available. As a common feature, all of them have an on-board EV charger and are equipped with an interface for an off-board charger. For both on-board and off-board approaches, advantages and disadvantages are recognized, mainly the required charging time and the influence caused in the battery lifetime [8]. Although the advantages of on-board chargers in terms of facility of charging in different points, the off-board charger is seeming as a key future technology aiming to reduce the charging time, since the charging is performed as fast as possible with benefits for the user and helping to contribute to disseminating the electric mobility.

In order to perform the charging from the power grid, the conversion of ac voltages to dc voltages is required, where conventional passive and active solutions can be considered [9][10][11]. Analyzing in more detail, off-board chargers are constituted by two controlled power stages: an ac-dc and a dc-dc [12]. The ac-dc stage is responsible for ensuring the operation with high levels of power quality (e.g., sinusoidal and balanced currents) for all the range of operation, while the dc-dc is responsible for ensuring a high level of controlled stages of constant current and voltage on the battery-side. Both power stages are relevant, however, from the perspective of preserving the EV battery lifetime, a special emphasis must be considered in the design of the dc-dc stage. Moreover, it is also important to consider emerging switching devices in the perspective of maximize energy efficiency as well as advanced topologies for the dc-dc stage.

Regarding switching devices, silicon carbide (SiC) and gallium nitride (GaN) are seen as viable and dominating technologies for a wide range of power electronics applications in the next decades. These technologies offer the possibility to design power electronics applications with high efficiency, high power density, and high lifecycle. Based on the state of developing, SiC technology is seen as the most promising, in the mid-term, to substitute the conventional technologies (e.g., Si-IGBTs) in industrial and automotive applications [13]. As the main advantages, SiC devices offer high thermal conductivity, high blocking voltage, and low on-state resistance. SiC devices are used in different applications of power electronics, such for example, electric mobility [14], UPS modules [15], advanced power conversion concepts [16], electrical aircraft [17], and future data centers [18].

Regarding dc-dc topologies, a bidirectional interleaved dc-dc converter, flexible in terms of buck-boost operation according to the dc-link voltage is proposed in [19], in order to optimize the EV battery. A modular three-phase dc-dc interleaved converter is proposed in [20] for EV fast charging applications, aiming to obtain a zero current ripple in the battery-side for a typical output voltage ranges. A new interleaved current-source resonant converter is proposed in [21] for EV applications. An interleaved dc-dc converter based on a three-phase structure is proposed in [22] for EV off-board chargers with the objective to minimize the current ripple on the battery-side.

Based on these different possibilities of interleaved dc-dc converters, the main objective of this paper is to present a comprehensive efficiency comparison between SiC-MOSFET and Si-IGBT devices when applied to a three-phase dc-dc interleaved converter. The interleaved topology was considered for the dc-dc power stage due to its relevance for EV chargers from the perspective of reducing the voltage and current ripple in the battery-side.

After this introduction, a description of the dc-dc interleaved converter, considered in the performed analysis, is presented in section II, while the efficiency analysis is established in section III. The illustrative simulation results of both technologies (SiC-MOSFET and Si-IGBT) are presented and discussed in section IV and the final conclusions in section V.

II. DC-DC Interleaved Converter

The EV fast charger topology, considered in this work, consists of a three-phase ac-dc converter connected to an interleaved dc-dc chopper (with a three-phase structure) as shown in Fig. 1. The interleaved dc-dc converter is composed of different basic elements connected in parallel. Each element consists of a standard two-level three-phase converter with an output inductor L_{out} and an input (DC) capacitor C, as shown in Fig. 1. In the perspective of EV fats charger, these elements provide high modularity, robustness, and scalability to the dc-dc converter. Moreover, a higher output power rating can be achieved by adopting more elements [23][24].

The ac-dc converter is connected to the power grid and it regulates the dc-link voltage V_{DC}. The interleaved dc-dc converter provides the desired output current by properly controlling the output voltage. The output current is evenly shared among the legs and a reduction of the output current ripple can be achieved. In particular, by introducing a phase-shift among the carriers, equal to 360° divided by the number of legs, the minimum output current ripple can be achieved. Moreover, having the possibility to modify the dc-link voltage and properly controlling the duty-cycle, zero output current ripple can be also accomplished. More details about the operation, the control and the ripple minimization for this topology can be found in [20][22].

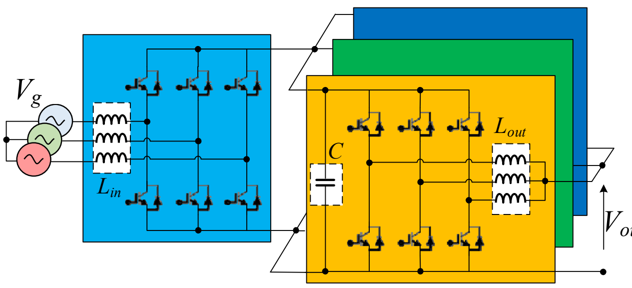

Fig. 1. EV fast charger topology consisting of a three-phase ac-dc converter and an interleaved dc-dc converter (with a three-phase structure).

As mentioned in the introduction, this work focuses on the efficiency analysis of the interleaved dc-dc converter, considering SiC-MOSFET and Si-IGBT switching devices and the application for EV chargers. The conduction and switching losses are firstly evaluated considering 1200 V SiC modules *SCT3080KLHR Rohm* with SiC Schottky anti-parallel diodes *SCS220KG Rohm*. The losses are then compared with the ones achieved by using 1200 V Si-IGBT modules *RGS50TSX2DHR Rohm*. The main parameters of the two switching devices are given in Table I.

III. Efficiency Analysis

In this section, the efficiency analysis is provided for the dc-dc converters and for the output inductors. The main losses in a power electronic converter are due to the switching devices, namely, the conduction and switching losses. Their evaluation is different depending on the adopted device and the topology. On the other hand, the inductor losses can be divided into winding and core losses. In the following, the different losses are evaluated for SiC-MOSFET and Si-IGBT devices, as well as inductors.

TABLE I. Switching Device Parameters

	Rohm Device parameters		
	SiC MOSFET SCT3080KLHR	***Si IGBT RGS50TSX2DHR***	***SiC Schottky diode SCS220KG***
V_{ds}	1200 V	1200 V	1200 V
I_{ds} (@25 °C)	31 A	50 A	-
I_{ds}/I_c (@100 °C)	22 A	25 A	20 A /133°C
$R_{ds,on}$ (@25 °C)	80 mΩ	N/A	N/A
$V_{ce\text{-}sat}$ (@25 °C)	N/A	1.7 V	N/A
Q_g	60 nC @18V	67 nC @15V	N/A
T_j	175 °C	175 °C	175 °C
P_{diss} (@25 °C)	165 W	395 W	210 W
r_{jc}	0.7 °C/W	0.38 °C/W	0.62 °C/W

A. Converter Conduction and Switching Losses

1) Conduction Losses

The conduction losses in the Si-IGBT are mainly due to the dynamic on resistance $R_{on,IGBT}$ and the zero on-state voltage V_{on}. They also depend on the average current I_{av} and the rms current I_{rms} that flow in the device, as shown in (1):

$$P_{con,IGBT} = V_{on} I_{av} + R_{on,IGBT} {I_{rms}}^2 \quad (1)$$

On the other hand, the SiC-MOSFET conduction losses are due to the on-resistance $R_{DS(on)}$ and the rms current I_{rms} that flows in the SiC-MOSFET:

$$P_{con,MOSFET} = R_{DS(on)} {I_{rms}}^2 \quad (2)$$

The anti-parallel diode exhibits conduction losses dependent on the threshold voltage V_T, the dynamic on-resistance $R_{on,diode}$, and both I_{av} and I_{rms}:

$$P_{con,diode} = V_T I_{av} + R_{on,diode} {I_{rms}}^2 \quad (3)$$

2) Switching Losses

At this point, the switching losses must be evaluated. They depend on the switching frequency, the turning on and the turning off dissipated energy, respectively, $E_{on,device}$ and $E_{off,device}$,:

$$P_{sw,device} = f_{sw} \frac{1}{T} \int_{0+\varphi}^{\frac{T}{2}} \left(E_{on,device} + E_{off,device}\right) dt \quad (4)$$

where f_{sw} is the switching frequency, φ the phase angle and $E_{on,\ device}$ and $E_{off,\ device}$ are the energy dissipated during the turn-on and the turn-off time, respectively.

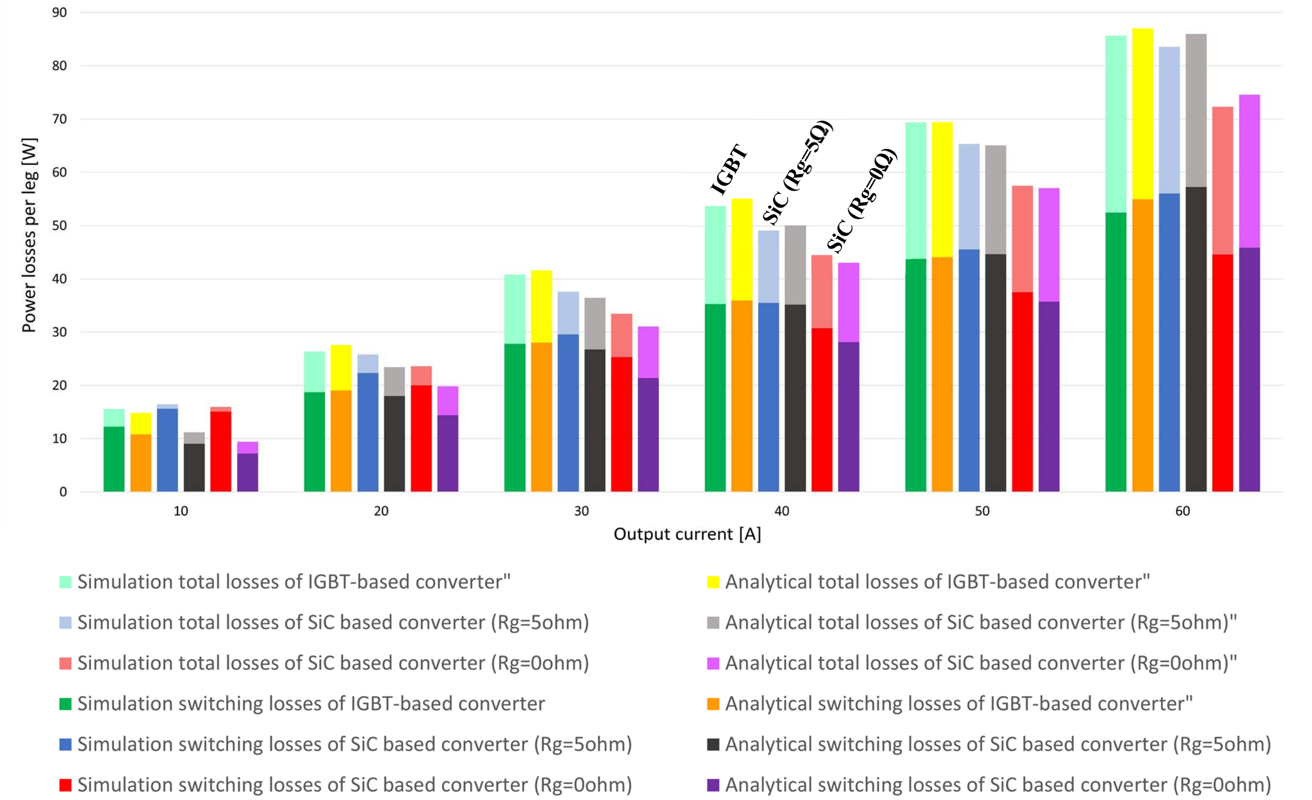

Fig. 2. Analytical and simulation total one leg power device losses of the inverters with different values of the output current.

3) Losses in the Interleaved dc-dc Converter

The conduction and switching losses of the interleaved dc-dc chopper can be firstly analysed by considering one leg of the converter. The output current consists of a DC value I_0 plus a ripple component Δi_o. The rms value of the current in the upper switch can be written as:

$$I_{rms,up} = \sqrt{R_{sw(on)} D I_o^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_o}{I_o}\right)^2\right]} \quad (5)$$

In the same way, the rms current value of the bottom switch is:

$$I_{rms,down} = \sqrt{R_{sw(on)}(1-D) I_o^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_o}{I_o}\right)^2\right]} \quad (6)$$

Then the conduction losses of the Si-IGBT, the SiC-MOSFET and the diode are:

$$P_{con,IGBT} = V_{on} I_o D' + R_{on,IGBT} D I_o^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_o}{I_o}\right)^2\right] \quad (7)$$

$$P_{con,MOSFET} = R_{DS(on)} D I_o^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_o}{I_o}\right)^2\right] \quad (8)$$

$$P_{con,diode} = V_T I_o D' + R_{on,diode} D' I_o^2 \left[1 + \frac{1}{12}\left(\frac{\Delta i_o}{I_o}\right)^2\right] \quad (9)$$

where D is the duty-cycle and $D' = (1\text{-}D)$. On the other hand, the switching losses can be evaluated as in the following:

$$P_{sw,device} = f_{sw} E_{sw,device} \left(\frac{I_{avg}}{I_{ref}}\right)^{K_I} \left(\frac{V_{sup}}{V_{ref}}\right)^{K_V} \quad (10)$$

where I_{avg} is the average output curreny, V_{sup} is the device supply voltage, I_{ref}, V_{ref} are reference current and voltage of the switching loss measurement available in the device's datasheet, K_I, K_V, G_I are the coefficients defined in [25].

B. *Inductor Losses*

1) Winding Losses

The power dissipation occurs in the inductor due to the DC resistance (R_{DC}) of the windings, but also phenomena such as skin effect and proximity effect when ac current is applied. The latter two will be neglected due to the simplicity. The losses due to the DC resistance can be determined using:

$$P_{LW} = R_{DC} {I_{rms}}^2 \quad (11)$$

where I_{rms} is the rms current through the inductor.

2) Core Losses

Energy losses due to the changing magnetic energy in the core during a switching cycle can be calculated based on the difference between magnetic energy put into the core during the on time, and the magnetic energy extracted from the core during the off time.

By using Ampere's & Faraday's Law, the energy in the core can be expressed as:

$$E = \int H dB \quad (12)$$

where B is the magnetic flux density and H is the magnetic field intensity. The power loss can be estimated as the energy multiplied by the switching frequency. Another way is to use Steinmetz equation:

$$P_{LC} = K f^{\alpha} B_{pk}^{\beta} \quad (13)$$

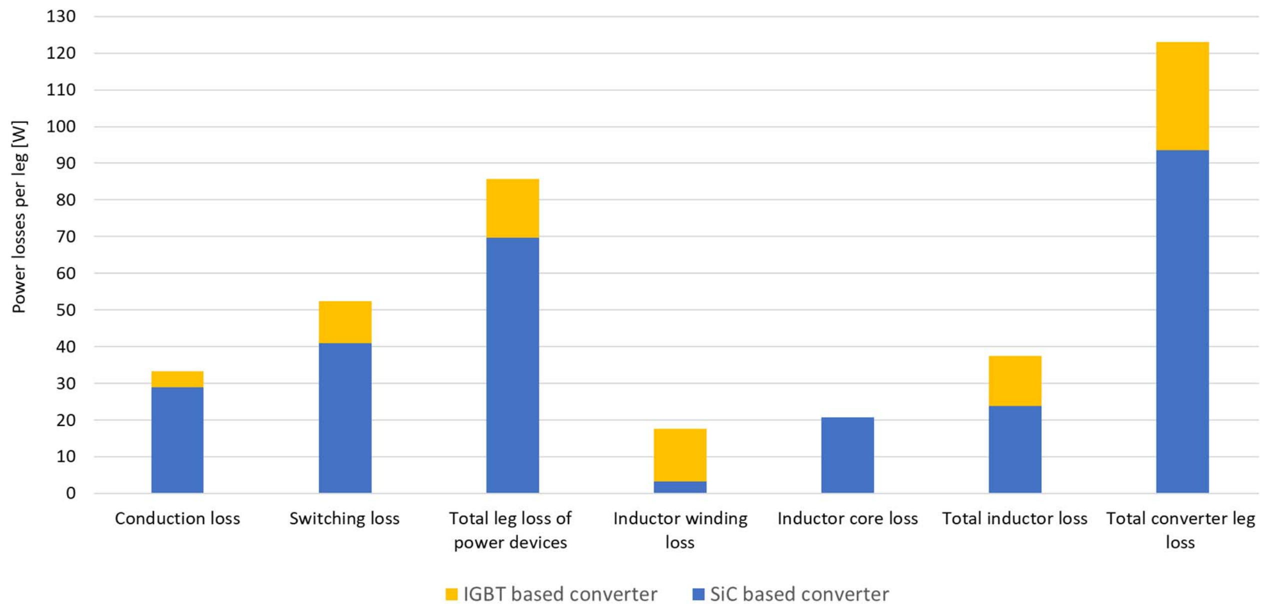

Fig. 3. Power devices and inductor losses of the converter leg

where P_{LC} is the core loss (hysteresis and eddy current loss), f is the frequency, B_{pk} is peak flux density of a sinusoidal excitation, K, α and β are the constants, which depend on core material, magnetic induction and switching frequency operating range and, if not given in datasheets of magnetic cores, can be obtained from [26]. Core loss can also be estimated by using a core loss curves for a specific flux density (e.g., as given in [27] for different core sizes and shapes).

IV. Simulation Results

TABLE II. Simulation Parameters

PARAMETERS	*SiC based converter*	*IGBT based converter*
V_{dc} [V]	800	800
f_{sw} [kHz]	80	20
R_{gate} [Ω]	0 ; 5	10
L_{out} [mH]	1.73 ; 0.45	1.73
D	0.5	0.5

The interleaved dc-dc converter, shown in Fig. 1, has been simulated using the LTspice software, considering 2 different cases. Firstly, the case with a different inductor ripple is given where only 1 inductor value for SiC-MOSFET based and IGBT based converter, i.e., a fixed value of L_{out}=1.73 mH, is considered. Secondly, the case with the same output current ripple is analyzed. Two different inductors were used with SiC-MOSFET based (L_{out} = 0.45 mH) and IGBT based (L_{out} = 1.73 mH) converters, due to the fact that different switching frequencies have been employed for two converters, i.e., 80 kHz for the SiC MOSFET based converter, and 20 kHz for the Si IGBT based converter. The other main simulation parameters are given in Table II.

The power losses have been compared considering both the losses obtained in LTspice simulation tool (by using the LTspice instantaneous power dissipation function) and the ones obtained analytically by considering equations (1) to (13). In order to have the same output voltage capabilities, the two converters were supplied by a nominal dc link voltage of V_{DC} = 800 V. The power modules' real models from the main producers were used for this analysis, as aforementioned in Section II. The control reference was compared with three shifted carriers in order to obtain the pulse-width modulation (as explained in Section II) for the switching devices, providing a fixed switching frequency, which is used in the evaluation of the losses established in this Section.

A. Losses with the Same Inductor

Fig. 2 shows the simulation and analytical power losses comparison for one leg of the two converters (SiC-MOSFET based and Si-IGBT based), and with different values of the output current, *i.e.*, 10 A, 20 A, 30 A, 40 A, 50 A, and 60 A. The analytical values were evaluated as described in Section III. The simulation losses are the result of the LTspice simulation using the two technologies in the converters: SiC-MOSFET based and Si-IGBT based. Firstly, it can be noted the good agreement between analytical and simulation results in almost all cases. The losses of the Si-IGBT based converter are similar to the losses of the SiC-MOSFET based converter, when considering the gate resistance of 5 **Ω**, even though the switching frequency of SiC-MOSFET based converter is 4 times the one of the Si-IGBT based converter. Moreover, in order to take the advantage of the SiC-MOSFET fast switching operation, the case with no additional external gate resistance (0 **Ω**) has also been considered. The device's internal resistance is of 12 **Ω** (from datasheet), but also the gate driver itself has its own internal resistance (~few **Ω**). From Fig. 2, it can be noted that the SiC-MOSFET based converter with the gate resistance of 0 **Ω** shows the lowest losses, being 16% lower when compared to Si-IGBT based converter, when the analysis is performed for the highest value of current (60 A). As it can be seen also in Fig. 2, similar results were obtained considering the other values of output current.

B. Losses with the Same Inductor Current Ripple

In this case only the highest value of the output current has been considered, *i.e.*, 60 A. The same core was selected for the two inductors, model T520-63 from Micrometals [28]. In the case of the 0.45 mH inductor, the number of turns was evaluated to be 87 and wire size AWG 3 was selected, while for the 1.73 mH inductor the number of turns was evaluated to be 195, with wire size AWG 7. These considerations were made by keeping almost the same mass of copper for the two inductors.

The inductor ohmic losses have been calculated according to equation (11), where the resistance was calculated according to:

$$R_{DC} = \frac{\rho\, N\, mlt}{A_{winding}} \quad (14)$$

where ρ is the specific copper resistivity, *mlt* is the mean length per turn given in the datasheet, N is the number of turns, and $A_{winding}$ is the cross-sectional area of the winding. On the other hand, the core losses were estimated according to the power losses curves given in the [28]. First, the peak flux density can be calculated as:

$$B_{pk} = \frac{E_{rms}\, 10^8}{4.44\, A_e\, N\, f_{sw}} \quad (15)$$

where E_{rms} is the rms voltage across the inductor, and A_e is the cross-sectional area. After knowing B_{pk}, it is possible to utilize the Core Loss curves given in [28], for the specific switching frequency.

Fig. 3 shows different losses for the power devices, as well as for the inductor, considering the same value of the inductor current ripple. The power device losses are obtained directly from the simulation tool LTspice, while the inductor losses are evaluated as explained previously. The best case for the SiC-MOSFET converter from Fig. 2 has been considered, i.e., when the gate resistance is 0 Ω. It can be noted that the Si-IGBT based converter shows both higher power device losses and inductor losses (mainly winding losses). The core losses are practically the same for the two inductors. The total converter leg losses of the SiC-MOSFET based converter are 24% lower than the IGBT based converter, with lower both power device losses (19%) and inductor losses (37%).

V. CONCLUSIONS

In this paper, an investigation of a three-phase interleaved dc-dc topology for EV fast chargers was considered. In particular, a comparison has been made considering two technologies for the converter, based on SiC-MOSFET power devices and other based on Si-IGBT power devices. Two cases have been presented: 1) when the two converters have the same inductor and only power device losses have been taken into account; 2) when the two converters have the same inductor current ripple, where different inductors have been considered and the inductor design and losses have been also included in the analysis. The simulations were carried out in LTspice simulation tool on realistic dynamic models of the power switching modules obtained from the manufacturer's experimental tests. Good agreement has been verified also with the theoretical analysis. The obtained results validate the use of SiC-MOSFET for the three-phase interleaved dc-dc topology, showing 24% lower total converter losses when considering the same inductor current ripple.

REFERENCES

[1] C. C. Chan, "The State of the Art of Electric, Hybrid, and Fuel Cell Vehicles," Proc. IEEE, vol.95, no.4, pp.704-718, Apr. 2007.

[2] Sagar K. Rastogi, Arun Sankar, Kushagra Manglik, Santanu K. Mishra, Saraju P. Mohanty, "Toward the Vision of All-Electric Vehicles in a Decade," IEEE Consumer Electronics Magazine, pp.103-107, Mar. 2019.

[3] Ali M. Bazzi, Yiqi Liu, Daniel S. Fay, "Electric Machines and Energy Storage: Over a century of technologies in electric and hybrid electric vehicles," IEEE Electrification Magazine, pp.49-53, Sept. 2018.

[4] Iban Junquera Martinez, Javier Garcia-Villalobos, Inmaculada Zamora, Pablo Eguia, "Energy Management of Micro Renewable Energy Source and Electric Vehicles at Home Level ," SPRINGER Journal of Modern Power Systems and Clean Energy, vol.5, no.6, pp.979-990, Nov. 2017.

[5] Tian Zhang, Wei Chen, Zhu Han, Zhigang Cao, "Charging Scheduling of Electric VehiclesWith Local Renewable Energy Under Uncertain Electric Vehicle Arrival and Grid Power Price," IEEE Trans. Veh. Technol., vol.63., no.6, pp.2600-2612, July 2014.

[6] Mingrui Zhang, Jie Chen, "The Energy Management and Optimized Operation of Electric Vehicles Based on Microgrid," IEEE Trans. Power Del., vol.29, no.3, pp.1427-1435, June 2014.

[7] Marcelo Masera, Ettore F. Bompard, Francesco Profumo, Nouredine Hadjsaid, "Smart (Electricity) Grids for Smart Cities: Assessing Roles and Societal Impacts," Proc. IEEE, vol.106, no.4, pp.613-625, Apr. 2018.

[8] Mohamed Yehia Metwly, Fadi Adel Maximos, et. al., "Design Case Study of A Nine-Phase Integrated On-Board Battery Charger," MEPCON International Middle East Power Systems Conference, 2018.

[9] Bhim Singh, Brij N. Singh, Ambrish Chandra, Kamal Al-Haddad, Ashish Pandey, Dwarka P. Kothari, "A Review of Three-Phase Improved Power Quality AC-DC Converters," IEEE Trans. Ind. Electron., vol.51, no.3, pp.641-660, June 2004.

[10] Johann W. Kolar, Thomas Friedli, Jose Rodriguez, Patrick W. Wheeler, "Review of Three-Phase PWM AC–AC Converter Topologies," IEEE Trans. Ind. Electron., vol.58, no.11, pp-4988-5006, Nov. 2011.

[11] Krishna Kumar Gupta, Alekh Ranjan, Pallavee Bhatnagar, Lalit Kumar Sahu, Shailendra Jain, "Multilevel Inverter Topologies With Reduced Device Count: A Review," IEEE Trans. Power Electron., vol.31, no.1, pp.135-151, Jan. 2016.

[12] Vitor Monteiro, Joao C. Ferreira, Andres A. Nogueiras Melendez, Carlos Couto, Joao L. Afonso, "Experimental Validation of a Novel Architecture Based on a Dual-Stage Converter for Off-Board Fast Battery Chargers of Electric Vehicles," IEEE Trans. Veh. Tech., vol.67, no.2, pp.1000-1011, Feb. 2018.

[13] Luciano F. S. Alves, Ruan C. M. Gomes, Pierre Lefranc, Raoni de A. Pegado, Pierre-Olivier Jeannin, B. A. Luciano, Filipe V. Rocha, "SiC Power Devices in Power Electronics: An Overview," IEEE COBEP Brazilian Power Electronics Conference, pp.1-8, Nov. 2017.

[14] Kimimori Hamada, Masaru Nagao, Masaki Ajioka, Fumiaki Kawai, "SiC—Emerging Power Device Technology for Next-Generation Electrically Powered Environmentally Friendly Vehicles," IEEE Trans. Electron Devices, vol.62, no.2, pp.278-285, Feb. 2015.

[15] Sungjae Ohn, Jianghui Yu, Paul Rankin, Bingyao Sun, Rolando Burgos, Dushan Boroyevich, Harish Suryanarayana, Christopher Belcastro, "Three-Terminal Common-Mode EMI Model for EMI Generation, Propagation, and Mitigation in a Full-SiC Three-Phase UPS Module," IEEE Trans. Power Electron., vol.34, no.9, pp.8599-8612, Sept. 2019.

[16] Samir Hazra, Ankan De, Lin Cheng, John Palmour, Marcelo Schupbach, Brett A. Hull, Scott Allen, Subhashish Bhattacharya, "High Switching Performance of 1700-V, 50-A SiC Power MOSFET Over Si IGBT/BiMOSFET for Advanced Power Conversion Applications," IEEE Trans. Power Electron., vol.31, no.7, pp.4742-4754, July 2016.

[17] Mattia Guacci , Dominik Bortis , Ivana F. Kovačević-Badstübner, Ulrike Grossner, Johann W. Kolar, "Analysis and Design of a 1200 V All-SiC Planar Interconnection Power Module for Next Generation More Electrical Aircraft Power Electronic Building Blocks," CPSS Trans. Power Electron. Appl., vol.2, no.4, pp.320-330, Dec. 2017.

[18] Daniel Rothmund, Thomas Guillod, Dominik Bortis, Johann W. Kolar, "99% Efficient 10 kV SiC-Based 7 kV/400 V DC Transformer for Future Data Centers," IEEE J. Emerg. Sel. Topics Power Electron., vol.7, no.2, pp.753-767, June 2019.

[19] Ahmed M. Omara, M. Sleptsov, "Bidirectional Interleaved DC/DC Converter for Electric Vehicle Application," IFOST-2016: Mechatronics, Electrical Engineering and Power Electronics, pp.100-

104, June 2016.

[20] M. Hammami, A. Viatkin, M. Ricco, G. Grandi, "A DC/DC Fast Charger for Electric Vehicles with Minimum Input/Output Ripple Based on Multiphase Interleaved Converters," IEEE ICCEP International Conference on Clean Electrical Power, pp.187-192, July 2019.

[21] Dongok Moon, Junsung Park, Sewan Choi, "New Interleaved Current-Fed Resonant Converter With Significantly Reduced High Current Side Output Filter for EV and HEV Applications," IEEE Trans. Power Electron., vol.30, no.8, pp.4264-4271, Aug. 2015.

[22] Klemen Drobnic , Gabriele Grandi, Manel Hammami, Riccardo Mandrioli, Mattia Ricco, Aleksandr Viatkin, Marija Vujacic, "An Output Ripple-Free Fast Charger for Electric Vehicles Based on Grid-Tied Modular Three-Phase Interleaved Converters," IEEE Trans. Ind. Appl., vol.55, no.6, pp.6102-6114, Nov. 2019.

[23] J. C. G. Justino, T. M. Parreiras, B. J. Cardoso Filho, "Hundreds kW charging stations for e-buses operating under regular ultra-fast charging," IEEE Trans. Ind. Appl., vol.52, no.2, pp.1766–1774, Mar./Apr. 2016.

[24] M. Jung, G. Lempidis, D. Holsch, J. Steffen, "Control and optimization strategies for interleaved dc-dc converters for EV battery charging applications," Proc. IEEE Energy Convers. Congr. Expo., Montreal, QC, Canada, pp.6022–6028, 2015.

[25] Semikron: Application Manual Power Semiconductors. Available online: https: //www.semikron.com/service-support/downloads/ (accessed on 17 January 2020).

[26] Magnetics "Curve fit equations for ferrite materials," Technical Bulletin, BULLETIN FC-S7, Magnetics, Inc., 1999.

[27] MicroMetals. Available online: https://www.micrometals.com (accessed on 17 January 2020).

[28] MicroMetals. Available online: https://micrometalsarnoldpowdercores.com/pdf/T520-63-DataSheet.pdf (accessed on 17 January 2020).