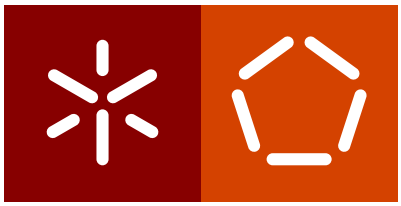

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Rectification, amplification and switching capabilities for energy harvesting systems

Power management circuit for piezoelectric energy harvester

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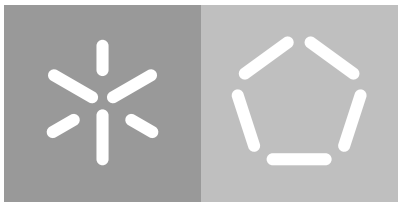

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Power management circuit for piezoelectric energy harvester

Master dissertation
Master Degree in Biomedical Engineering

Dissertation supervised by
Tao Dong
José Correia

July 2020

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Thank you!

Tusen takk!

Obrigada!

STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

RESUMO

Para combater a dependência dos dispositivos eletrónicos relativamente ás baterias é necessário um novo sistema energético, que permita prolongar o tempo de vida útil dos mesmos. Energy Harvesting é uma tecnologia promissora utilizada para alimentar dispositivos sem bateria. Este trabalho consiste na realização de componentes empregáveis num circuito global para extrair energia a partir ds vibrações de um piezoelétricos com baixo consumo de energia e alta eficiência. Os níveis de potência e voltagem gerados pelo transdutor piezoelétrico são relativamente baixos, especialmente em sistemas de pequena escala, por isso requerem cuidado extra relativamente ao consumo de energia e eficiência dos circuitos.

A principal contribuição deste trabalho é um sistema apropriado para amplificar, retificar e alternar o sinal instável proveniente de uma fonte de energy harvesting. Os componentes do sistema são implementados com base na tecnologia CMOS com $0.13\,\mu m$.

Um interruptor analógico capaz de modelar a frequência do sinal entre $1\,Hz$ e $1\,MHz$ e estável perante variações de temperatura, é implementado. O circuito tem um excelente isolamento de $-111.24\,dB$, devido a uma resistência OFF de $520.6\,M\Omega$.

O amplificador implementado é apto a amplificar um pequeno sinal com um ganho de $42.56\,dB$ e baixo consumo. O sinal de saída é satisfatoriamente amplificado com uma voltagem de offset de $8\,\mu V$.

Um retificador ativo de dois estágios com uma nova arquitetura é proposto. A eficiência de conversão de energia atinge os 40.4%, com uma eficiência de voltagem até 90%. O retificador consome pouca energia, apenas $17.7\,\mu W$, incorporando um comparador de $113.9\,nW$.

Os resultados validam as exigências energéticas do circuito, que pode ser usado para outras aplicações similares no campo biomédico, industrial e comercial.

Palavras-chave: Interruptor analógico, CMOS, Energy Harvesting, Rectificador, Amplificador.

ABSTRACT

A new energy mechanism needs to be addressed to overcome the battery dependency, and consequently extend Wireless Sensor Nodes (WSN) lifetime effectively. Energy Harvesting is a promising technology that can fulfill that premise. This work consists of the realization of circuit components employable in a management system for a piezoelectric-based energy harvester, with low power consumption and high efficiency. The implementation of energy harvesting systems is necessary to power-up front-end applications without any battery. The input power and voltage levels generated by the piezoelectric transducer are relatively low, especially in small-scale systems, as such extra care has to be taken in power consumption and efficiency of the circuits.

The main contribution of this work is a system capable of amplifying, rectifying and switching the unstable signal from an energy harvester source. The circuit components are designed based on $0.13\,\mu m$ Complementary Metal-Oxide-Semiconductor (CMOS) technology.

An analog switch, capable of driving the harvesting circuit at a frequency between $1\,Hz$ and $1\,MHz$, with proper temperature behaviour, is designed and verified. An OFF resistance of $520.6\,M\Omega$ and isolation of $-111.24\,dB$, grant excellent isolation to the circuit.

The designed voltage amplifier is capable of amplifying a minor signal with a gain of $42.56\,dB$, while requiring low power consumption. The output signal is satisfactorily amplified with a reduced offset voltage of $8\,\mu V$.

A new architecture of a two-stage active rectifier is proposed. The power conversion efficiency is 40.4%, with a voltage efficiency of up to 90%. Low power consumption of $17.7\,\mu W$ is achieved by the rectifier, with the embedded comparator consuming $113.9\,nW$.

The outcomes validate the circuit's power demands, which can be used for other similar applications in biomedical, industrial, and commercial fields.

Keywords: Analog Switch, CMOS, Energy Harvesting, Rectifier, Voltage Amplifier.

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ACRONYMS

A

AC Alternating Current.

ADC Analog-to-Digital Converters.

ASIC Application-Specific Integrated Circuit.

ASSH Adaptive Synchronized Switch Harvesting.

B

BBM Break-Before-Make.

BICMOS Bipolar CMOS.

BJT Bipolar Junction Transistor.

BR Bulk Regulation.

C

CMOS Complementary Metal-Oxide-Semiconductor.

CPU Central Processing Unit.

D

DC Direct Current.

DRC Design Rule Check.

DSSH Double Synchronized Switch Harvesting.

DTMOS Dynamic Threshold Voltage MOSFET.

E

EDA Electronic Design Automation.

ESD Electrostatic Discharge.

ESSH Enhanced Synchronized Switch Harvesting.

EU European Union.

EVC External V_{th} Cancellation.

F

FET Field Efect Transistor.

G

GBW Gain Bandwidth.

I

IC Integrated Circuit.

IO Input and Output.

IVC Internal V_{th} Cancellation.

J

JFET Junction gate Field-Effect Transistor.

L

LVS Layout Versus Schematic.

M

MBB Make-Before-Break.

MBPD MOSFET Bypass PMOS Diode.

MEMS Microelectromechanical Systems.

MIM Metal-Insulator-Metal.

MOS Metal-Oxide-Semiconductor.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

MR-SSHI Synchronized Switch Harvesting on Inductor using Magnetic Rectifier.

N

NVC Negative Voltage Converter.

O

OP-AMP Operational Amplifier.

P

P-SSHI Parallel Synchronized Switch Harvesting on Inductor.

PCE Power Conversion Efficiency.

PEG Piezoelectric Electrical Generator.

PS-SECE Phase Shift Synchronous Electric Charge Extraction.

PSRR Power Supply Rejection Ratio.

PWL Piecewise Linear.

R

R&D Research and Development.

RF Radio-Frequency.

S

S-SSHI Series Synchronized Switch Harvesting on Inductor.

SECE Synchronous Electric Charge Extraction.

SMPS Switch Mode Power Supply.

SPICE Simulation Program with Integrated Circuit Emphasis.

SSD Synchronized Switch Damping.

SSDCI Synchronized Switching and Discharging to a storage Capacitor through an Inductor.

SSHI Synchronized Switch Harvesting on Inductor.

SVC Self-V_{th} Cancellation.

U

ULP Ultra-Low Power.

W

WSN Wireless Sensor Nodes.

1

INTRODUCTION

The increasing demands for powering electronic devices, such as wearable, wireless sensor networks, biomedical implants, and so forth, have led to the current extensive exploration of power harvesting devices. The goal of electronic energy harvesting interfaces is to efficiently manage the scavenged energy to enable battery-free, low-maintenance and more eco-friendly devices, consequently allowing for more portable and lightweight electronic devices.

1.1 Motivation and Applications

Microsensor networks have an energy constraint on the sensor nodes imposed by the capacity of the nodes' battery. In order to extend the sensor lifetime, most microsensors work through a duty cycle, alternating between an active and a sleep mode, and shutdown unused components whenever possible. However, this does not remove the energy constraint by the battery.

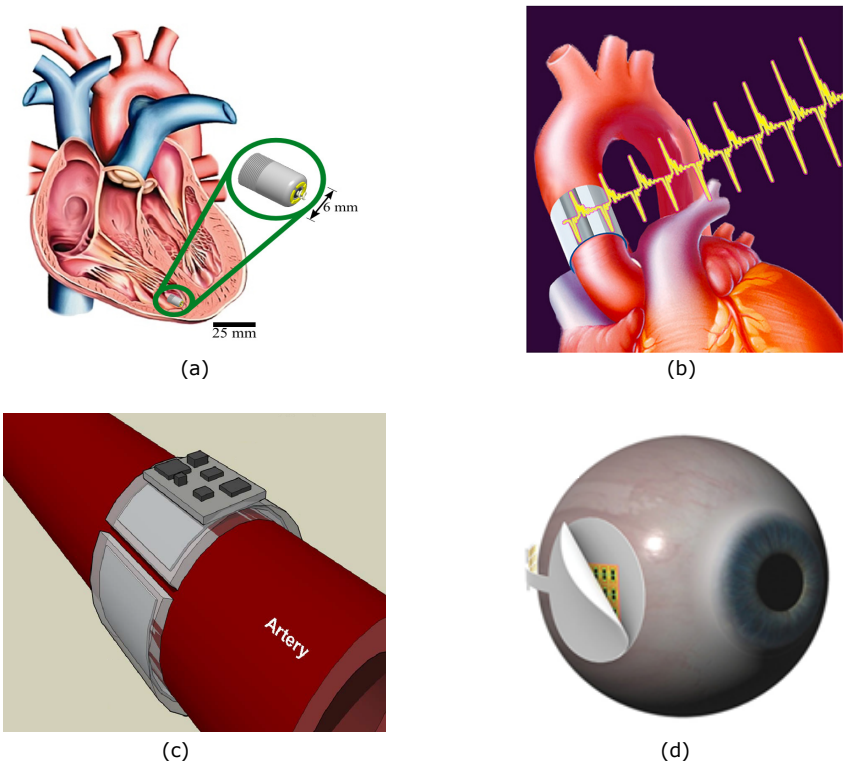
For some applications, a pure Lithium battery of $1\,cm^3$, capable of continuously supplying $1\,\mu W$ for five years, is enough (Calhoun et al., 2005). Nonetheless, nowadays batteries are a handicap for higher peak power and extended lifespan applications due to their low energy density and high costs (Bawa and Ghovanloo, 2008), raising maintenance, complexity, and recycling issues (Guyomar, 2011). In some situations, it is impractical or even impossible to change batteries. Therefore, a new approach to solve this problem involves using energy from the environment to supply devices, overcoming the previous issue, and making them self-powered and self-sufficient (Guyomar, 2011).

The recent increase of autonomous and efficient devices encouraged by industrial fields and personal applications has raised powering issues (Guyomar, 2011). There is a need for reduced power consumption, depending on the kind of use, e.g. low power sensors consumption is around $10\,\mu W$ to $100\,\mu W$.

Energy harvesting has become a significant research and development topic. This technology has a massive impact on people's life since it extends its applications in many fields, such as aeronautics, transports, civil engineering, biomedical engineer, Radio-Frequency (RF), home automation, nomad devices, and so on (Dai et al., 2015; Guyomar, 2011). Its impact on the deployment of WSN and wearable electronic devices is crucial (Dai et al., 2015), allowing the information collected from the systems to be transferred to the outside world in real-time (Bawa and Ghovanloo, 2008). Theoretically, those devices can have an infinite lifespan, being only limited by the lifetimes of their components.

Regarding the innovations above, the biomedical field benefits extensively from this technology progress through implantable sensors (Deterre et al., 2013), sending data from inside the human body (Peters et al., 2007) and allowing monitoring patient's health anywhere in real-time (Wong et al., 2016). Through these developments, patients can have a comfortable lifestyle, thanks to the freedom of movements due to wireless devices. Contrary to previous methods, which need for invasive procedures to replace batteries, these innovations reduce infection risk. Besides, they do not cause any discomfort or health risks to the patients (Peters et al., 2007). In this domain, the applications are widely explored, enabling the detection and treatment of diseases such as muscle paralysis and deafness (Cha et al., 2012). It can also be used to measure the physiological signals as heartbeat or blood flow sensing. Furthermore, it can record neuronal activity in patients with Parkinson or retinal prosthesis (Vakili and Golmakani, 2013). Figure 1 shows some of the aforementioned applications.

The implementation of these technologies has notably prompted a shift in the design approach of electronic systems, introducing new challenges for system designers. It is expected that by 2024, the global market of devices powered by ambient energy accomplish a total of 2.6 billion units (Chetto and Queudet, 2016). The European Commission presented the European Green Deal, the most ambitious package of measures aiming to become the world's first climate-neutral continent by 2050. That should enable European citizens and businesses to benefit from sustainable green transition (European Commission, 2019). A recent statistic on renewable energy sources in the European Union (EU) is given in Figure 2 (Eurostat Statistic Explained, 2020). It can be observed that the majority of countries increased the percentage of renewable sources from 2016 to 2018. For this year, 2020, most of the countries already achieve the expected goals in 2018, like Norway and Germany. Therefore, Europe is rapidly developing for a more sustainable continent.



(a) (b) (c) (d)

Figure 1: Biomedical applications requiring energy harvesting: (a) intra-cardiac implant placed in the heart cavity scavenging energy from regular blood pressure (Deterre et al., 2013); (b) a polyvinylidene fluoride harvester that extract energy from the arterial wall deformation (Yang et al., 2018); (c) implanted arterial cuff power source integrated into a self-powered blood pressure sensing system (Potkay and Brooks, 2008) and (d) flexible retinal implant device (Hwang et al., 2015).

1.2 Energy Harvesting

Energy harvesting has long been known as the process of scavenging energy available from the surrounding environment and converts it into electrical energy. Several types of sources can be used to harvest energy (Ali et al., 2014), and those are divided into two groups according to their characteristics (Dang et al., 2012). Firstly, the natural sources that are available directly from the environment, such as RF, solar power, thermal gradients, in particular geothermal heat, and mechanical vibration (Maiorca et al., 2013). Secondly, the artificial sources that are not generated by nature and result from human or system activities, such as body motion, breathing, blood pressure, and system vibration during their operational mode (Priya, 2007). A comparison of power densities from some energy harvesting mechanisms for a 10-year lifetime is given in Figure 3 (Roundy et al., 2003; Roundy et al., 2005; Cao et al., 2007). The highest power density comes from solar cells in direct sunlight - Figure 3(E). However, the best conditions for extracting solar energy are not available whenever (night) and everywhere because of climate changes. In areas with cloudy weather, Figure 3(F), where the light is not maximum, or even at

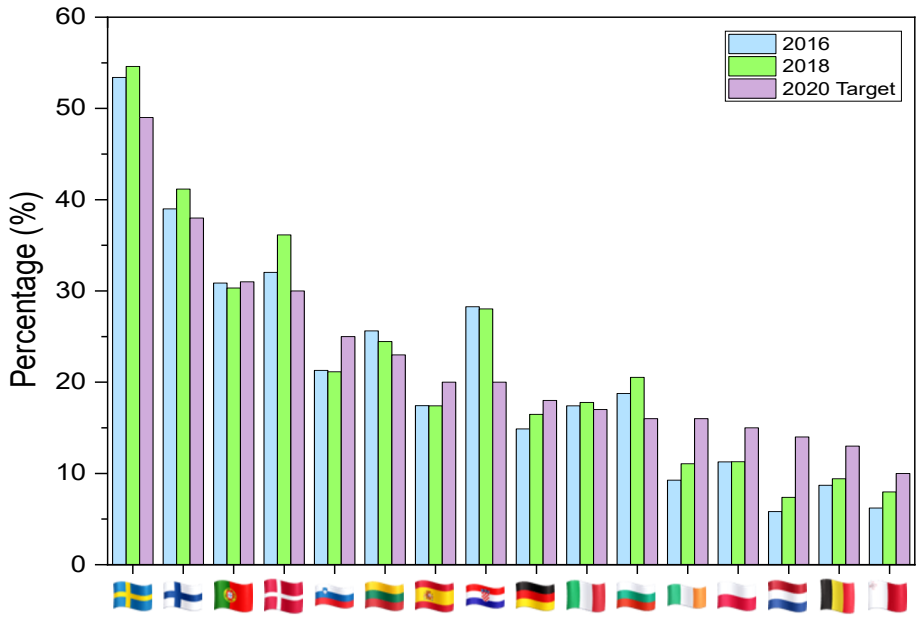


Figure 2: Overall share of energy from renewable sources in some the European Union member states (Eurostat Statistic Explained, 2020).

an indoor environment, Figure 3(G), as dim offices, the power density decreases drastically from $15000\ \mu W/cm^3$ to $6\ \mu W/cm^3$. Thermoelectric sources, Figure 3(D), scavenge power from thermal gradients with $15\ \mu W/cm^3$ at a $10\ ^\circ C$ gradient. Nonetheless, since there are sources more accessible to harvesting energy and with higher values, this method is considered inadequate.

Nevertheless, the implemented energy transducer depends on the available ambient energy to harvest. Therefore, Table 1 displays the correlation between the different ambient sources and what kind of transducer should be employed (Mateu et al., 2014).

Table 1: Transducers for different ambient energy sources.

Ambient Energy Source	**Transducer**
Light	Photovoltaic cell
Mechanical	Piezoelectric, electromagnetic, electrostatic
Thermal	Thermoelectric generator

Among the numerous sources, mechanical vibration energy is commonly explored since it is available in small-scale systems (Guyomar, 2011; Maiorca et al., 2013). Common day activities, such as walking produces energy with a power density of $850\ \mu W$, through mechanical vibrations, by applying a force of $2500\ N$ on a knee (Seunghyun, 2013). The best-known methods of transduction technologies for this source are piezoelectric,

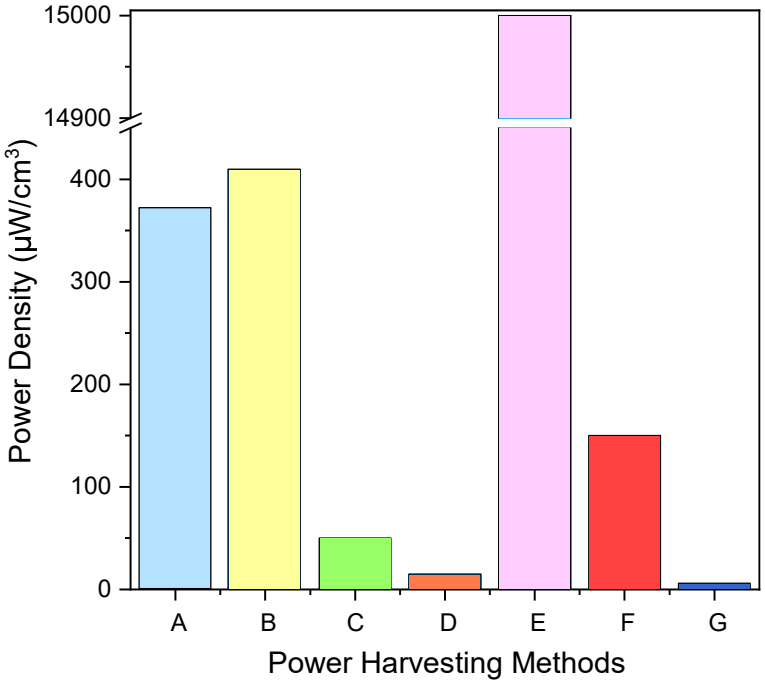


Figure 3: Comparison of energy sources with a fixed level of power generation (Roundy et al., 2003; Roundy et al., 2005; Cao et al., 2007). (A), (B) and (C) are vibration piezoelectric, electromagnetic and electrostatic, respectively; (D) is a thermoelectric source; (E), (F) and (G) are solar energy directly from sunlight on a clear weather day, on a cloudy day and indoor, correspondingly.

electromagnetic, or electrostatic (Figure 3). Those are coupled to the extraction structure to convert vibrations into electrical energy (Maiorca et al., 2013).

In Figure 3(C), with $50\,\mu W/cm^3$, is the electrostatic generation. Its operation consists of two conductors moving in relation to each other, separated by a dielectric. When the conductors move, the energy stored changes and the mechanical energy is converted into electrical energy (Roundy et al., 2003). These converters, combined with Microelectromechanical Systems (MEMS) processing technology, offer an effective method to obtain close integration with electronics and the potential to scale down to smaller sizes. These advantages are more significant for electrostatic converters than for the others. Nevertheless, the requirements of a separate voltage source to initiate the conversion process and the difficulties in their implementation constitute drawbacks for this transducer (S.P. Beepy, 2006).

The transducers represented by Figure 3(B) are ruled by the principle of electromagnetic induction defined by Faraday's law (Singh, 2011). A magnetic flux variation is created due to relative motion between a magnet and a coil, inducing an electromotive force across the coils. The corresponding energy to the motion damped is transduced into electrical energy (Kiziroglou and Yeatman, 2012). Although the energy is usually implemented for rotational movement, in energy harvesting sources, the free motion does not often come from rotational. In

literature, no inherent advantage is pointed to electromagnetic transducers over the other converters (Roundy et al., 2003).

1.3 Piezoelectric Transducer

Despite all the transducers above mentioned, this thesis project focuses on piezoelectric materials. A piezoelectric crystal suffers a charge separation due to a mechanical strain in the dielectric material, that is converted into electrical energy associated with the presence of electric charges. Thus, mechanical stress produces a voltage in the piezoelectric element (Roundy et al., 2003).

Generally, Figure 4 describes a vibration energy harvester. There is a special interest in piezoelectric elements thanks to their high energy densities and potential integration (Guyomar, 2011), exhibiting better performance than others (Maiorca et al., 2013). Even though they are more difficult to integrate into a microfabrication process than the other technologies, a recently study (Roundy et al., 2003) proves it is possible to integrate a piezoelectric transducer into a MEMS package. In this way, it becomes the premium option for the design of miniaturized and self-power devices (Guyomar, 2011). The efficiency of the conversion process from vibration into electric energy depends on the method of applying the oscillating stress onto the piezoelectric and material parameters (Priya, 2007).

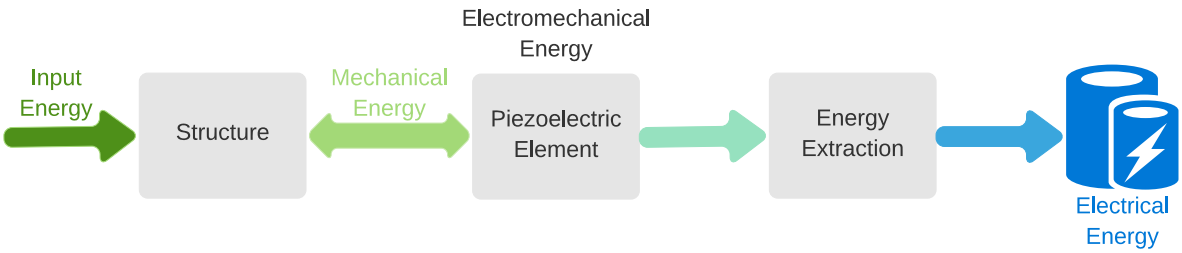


Figure 4: General schematic of a vibration piezoelectric energy harvester.

The equations (1) and (2) describe the mechanical and electrical behaviour of piezoelectric materials (Roundy et al., 2003). Assuming that δ is the mechanical strain, σ the mechanical stress, Y is the Young's modulus, also known as elastic modulus, used to describe stiffness of materials, D the electrical displacement, which is the charge density, E the electric field, ε the dielectric constant, and d the piezoelectric strain coefficient.

$$\delta = \frac{\sigma}{Y} + d \cdot E \tag{1}$$

$$D = \varepsilon \cdot E + d \cdot \sigma \tag{2}$$

An analytic model can be created associating the Euler–Bernoulli beam theory (Bauchau and Craig, 2009) and equations (1) and (2). Figure 5 shows an equivalent circuit of a basic configuration, where the output from the piezoelectric bender uses a resistive load (R_L) as termination and the piezoelectric element is modeled as an Alternating Current (AC) voltage (V_S) in series with a capacitor (C) and a resistor (R_S).

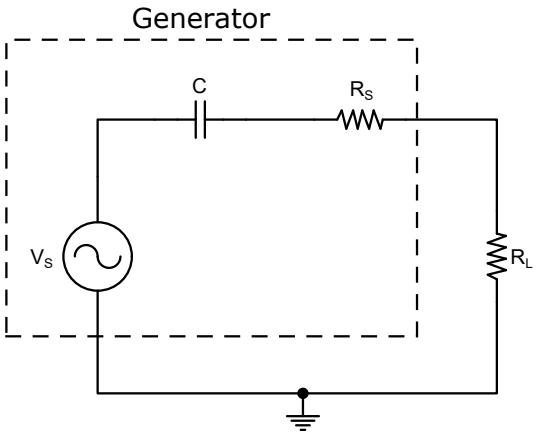


Figure 5: Equivalent circuit for a piezoelectric generator.

The energy generated by Piezoelectric Electrical Generators (PEGs) is unappropriated to directly power most of the electronic systems since it limits the power from tens of microwatts to a few milliwatts (Sodano et al., 2005). Most researchers came across this problem; thus, new methods to accumulate the generated energy are needed (Sodano et al., 2005). In order to address this issue, it is proposed the use of intrinsic mechanical nonlinearities that aims to increase the input energy in the host structure to provide more power. Beyond the type of approach, nonlinear electronic interfaces have been suggested to increase the conversion capabilities of piezo elements and extract a significant amount of energy (Guyomar, 2011).

1.4 Project Implementation

In a real-world application, the mechanical force applied to the piezoelectric crystals changes over time, resulting in changes in amplitude and frequency of the signal, and output impedance variations. A highly optimized control circuit is desirable to scavenge these power fluctuations from the different surrounding conditions.

The main problem with using these energy sources is the difference between the power generated and the power consumed. Technology developments have allowed this discrepancy to decrease, although a breakthrough is needed for an effective solution to be achieved. If the design of the piezoelectric element takes into account the typical vibration frequency of the application, the energy that is given by the transducers can be improved. Since the power output from a piezoelectric material is directly proportional to the vibrating frequency until the energy produced is optimal. This occurs when the natural frequency of the piezoelectric crystals matches the environment's vibrating frequency. Nonetheless, the development of these frequency-specific devices is costly and inconvenient, considering a new design had to be produced for each application. Thereby the power generated by the energy harvester is mostly enhanced in the power management circuit.

Another way to improve the power output is to create more efficient conversion circuits. The efficiency of these circuits is measured by a ratio between transducer energy and energy production of the final user device. Micro energy harvesters, which scavenged power is less than $0.1\ \mu W$, requires an optimized power management circuit that effectively converts and stores this power. To reach the optimal efficiency point, research must be done involving electronic circuits and methods to be employed on the desirable system.

The power management circuit of an energy harvester extracts the energy generated by the transducer element, converts it into usable electric signal for a specific application, and conveys it to the requesting devices. Thus, the AC voltage must be converted to a Direct Current (DC) voltage, typically by a rectifier for energy storage and power systems (Peters et al., 2007; Sun et al., 2016). Thence a rectifier should be capable of handling low input amplitude and high sensitivity, along with low power consumption to achieve high efficiency (Wong et al., 2016).

Several research was conducted in the past few years, revealing that the main requirements for the extraction circuits for piezoelectric energy harvesters are efficiency and autonomous operation. The circuit should operate at very low power consumption, as the transducer's energy is already extremely low. As such, the circuit efficiency is of the utmost importance.

On the final application, the harvesting circuit should operate independently from the other devices. Due to this, the energy harvester can work without the aid of external sources, ensuring the electronic device is powered as needed. It is also crucial the circuit adaptation to environmental changes, to maximize efficiency. Besides being an attempt to match the transducer's excitation frequency, the circuit should be prepared for sudden amplitude changes in the oscillation.

The main goal of this study is to design and simulate an Integrated Circuit (IC) to efficiently scavenge energy from a random low power input signal generated by a vibrating piezoelectric transducer. Furthermore, implemen-

tation of custom components taking into account the CMOS technology advantages to their maximum capability is also a requirement. The fabrication of CMOS devices can have different process sizes, in particular, for this project, it was chosen the $0.13\,\mu m$ CMOS process. This process size was chosen to shrink the design size yet remaining affordable, and keeping the leakage current low. Moreover, the reduction of parasitic capacitance and lower core voltage means the transistors can be driven by a lower voltage, which is suitable for application in diverse fields.

The harvesting architecture is based on an automatic frequency up-conversion technique (Li et al., 2014). It is designed to match the output impedance of the piezoelectric transducer dynamically by shifting the vibrational frequency of the piezoelectric element up to the resonant frequency of the harvesting interface. Thereby, an analog switch and a voltage amplifier are added to the circuit.

1.5 Thesis Organization

The present chapter introduces the concept of energy harvesting systems coming up until the concept of a piezoelectric transducer, also referring to the motivation and objectives of this dissertation. The necessary knowledge basis was acquired through a literature study in the preliminary work is presented in chapter 2, which addresses piezoelectric energy harvesters, electronic design and optimization, power management circuitry, and CMOS design/fabrication. Regarding the practical knowledge and requirements, those are supplied by the CMOS foundry partner. This chapter also explores in detail the background of the circuit of interest.

The main goal of the present study is to develop, design and simulate an IC, which includes a pre-voltage amplifier, an analog switch, and a rectifier. Those are designed according to the requested parameters by the extraction circuit with a very low power consumption. In chapter 3, an analysis of the system is done to compare topologies and to find the flaws in the circuits. It starts by modelling the system in manageable blocks and proceeding with the simulation of those blocks. The simulation results of each topology are followed by a comparison with previous works or off-the-shelf components. An iterative optimization is used to find the best topology for the use case, by maximizing the power efficiency of the circuit. Additionally, chapter 3 describes the project fabrication process.

In chapter 4 is presented the conclusion, along with some ideas that can become future target research. In addition, chapter A includes more detail regarding the CMOS fabrication, in conjunction with photos of the designs, layouts and chip. Beyond this, some of the outputs from this thesis are two articles, "**A Low-power Two-Stage**

Active Rectifier for Energy Harvesting Applications" and "**A CMOS Low-power Two-Stage Active Rectifier for Energy Harvesting Applications**", that are annexed to this document in chapter **??**.

2

STATE OF THE ART

In this chapter, for a more complete knowledge of what is done is imperative to understand the background of the critical components: switch, amplifier and rectifier. Thus, an exhaustive and detailed review is given in this chapter.

2.1 Analog Switch

Numerous harvesting interfaces have been proposed in the literature to maximize the energy extraction derived from mechanical vibrations. Switched magnetic elements, as inductors or transformers, are used in rectification stages to partially match the reactive component of the piezoelectric impedance, causing a resonance effect.

Piezoelectric rectifiers use switched magnetic components to reduce the size of inductors and transducers and efficiently extract vibrational energy. This allows scavenging energy from a wide range of frequencies caused by the use of autonomous switch techniques monitoring the surrounding conditions.

The switch-mode transformers, also known as Switch Mode Power Supply (SMPS) transformers, use a regulated power supply to step up or step down voltage or current. Besides, they are capable of providing isolation between the input and output. Their goal is to deliver a constant output voltage over varying load conditions.

According to Guyomar (2011), there are two approaches, whether the piezoelectric element is directly connected to the switched magnetic components, or just after the rectifier. The operation principles are identical: both aim to enhance the conversion by increasing the voltage and decreasing the time shift between the voltage and the velocity. A nonlinear approach reduces time shift and increase voltage.

2.1.1 Direct Energy Transfer

Standard Energy Harvesting Interface

The standard interface of an energy harvesting is depicted in Figure 6, consisting of a merely direct connection between the piezoelectric material and the storage stage through a rectifier bridge.

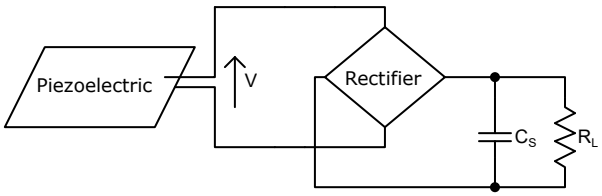


Figure 6: Circuit schematic of the standard energy harvesting interface.

The energy from the piezoelectric flows to charge the storage capacitor (C_S) anytime the absolute value of the piezo voltage (V) is higher than the rectified voltage (Lallart et al., 2011). On the contrary, when the absolute value of the piezoelectric material voltage is less than the output voltage of the rectifier, the piezoelectric element is let in open circuit, and the rectifier is blocked (Garbuio et al., 2009). Nonetheless, regarding the amount of energy that can be harvested, there is an upper limit due to the vibrational amplitude of the structure that determines the maximum piezoelectric voltage (Makihara and Asahina, 2017).

Parallel and Series Synchronized Switch Harvesting on Inductor

Series Synchronized Switch Harvesting on Inductor (S-SSHI) and Parallel Synchronized Switch Harvesting on Inductor (P-SSHI) are the first and simplest two resonant rectifiers proposed (Badel et al., 2006). The switch and the inductor, S and L, respectively, are directly connected in series, Figure 7, or in parallel, Figure 8, to the piezoelectric element. These techniques aim at artificially increasing the conversion capabilities of the piezoelectric element (Lefeuvre et al., 2006).

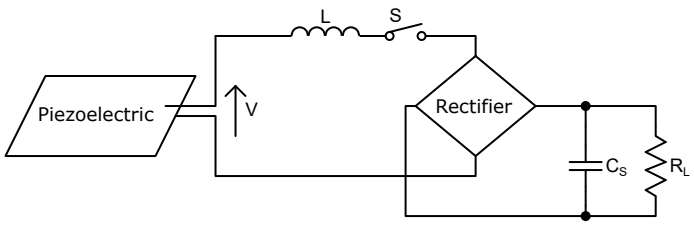


Figure 7: Circuit schematic of the S-SSHI rectifier.

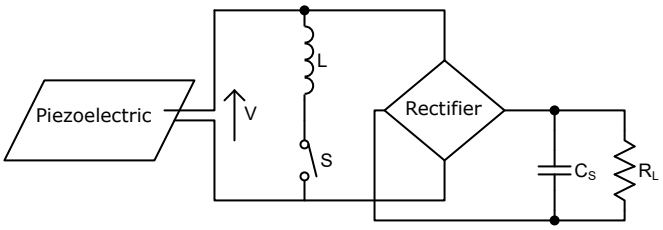


Figure 8: Circuit schematic of the P-SSHI rectifier.

In both structures, the switch S is closed when the voltage generated by the piezoelectric transducer (V) reaches an extremum. In other words, the switch closes at the maximum and minimum of the mass displacement, and is kept close until a full voltage inversion on the piezoelectric transducer is achieved. The voltage inversion occurs if the switching period (t_i) corresponds to half of the pseudo-period of the electrical resonant circuit (Equation 3) shaped by the capacitance of the piezoelectric (C_0) and the inductor (Garbuio et al., 2009).

$$t_i = \pi \cdot \sqrt{L \cdot C_0} \tag{3}$$

However, this inversion is not perfect as a result of the internal inductor losses, and it is characterized by the inversion coefficient γ defined by Lallart et al. (2011) as:

$$\gamma \approx e^{\frac{-2 \cdot \pi}{Q_i}}, \tag{4}$$

assuming that Q_i is the electrical quality factor of the circuit.

A coil has an inductance (L) when the current flows through the coil and changes at a rate (di/dt) (Singh, 2011), inducting a voltage (V_L) expressed according to Equation 5.

$$V_L = -L \cdot \frac{di}{dt} \tag{5}$$

The relationship between self-inductance and the number of turns (N) for a single coil can be given as:

$$L = N \cdot \frac{\Phi}{I}, \tag{6}$$

admitting that Φ is the magnetic flux and I the current. The coefficient of self-inductance also depends on design features, such as length, number of turns, and size. Therefore, for a coil, the magnetic flux produced in its inner core is equal to:

$$\Phi = B \cdot A, \tag{7}$$

where B is the flux density, and A is the cross-section area. The magnetic induction of a long solenoid coil with N number of turns per meter length in the inner core is given as (Singh, 2011):

$$B = \mu \cdot \frac{N \cdot I}{l}, \tag{8}$$

where μ is the permeability of the core material and l is the length of the coil, according to Faraday's Law, any change in the magnetic flux linkage produces a self-induced voltage in a single-coil as described in Equation 9 (Wadhwa, 2005).

$$V_L = N \cdot \frac{d\Phi}{dt} = \frac{\mu \cdot N^2 \cdot A}{l} \cdot \frac{di}{dt} \tag{9}$$

The operation principles of the interfaces are slightly different. In the P-SSHI, after the extraction of energy, the voltage is inverted, albeit, in S-SSHI, these two processes happen simultaneously. The Synchronized Switch Damping (SSD) is the effect of the voltage inversion, affecting the overall conversion efficiency, due to an electrical attenuation that opposes the mechanical vibration on the piezoelectric material. This is the main problem of both interfaces (Badel et al., 2006).

Synchronized Switch Harvesting on Inductor using Magnetic Rectifier

Synchronized Switch Harvesting on Inductor (SSHI) can also be achieved by replacing the switching inductor by a transformer, as exhibited in Figure 9, and it is called Synchronized Switch Harvesting on Inductor using Magnetic Rectifier (MR-SSHI).

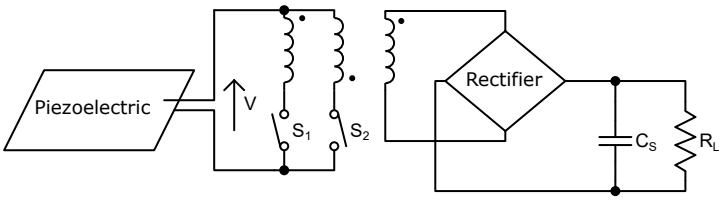


Figure 9: Circuit diagram of the MR-SSHI.

The transformer has two primary windings in series with unidirectional switches, S_1 and S_2, and one secondary winding connected to the rectifier (Garbuio et al., 2009). The two primary coils are connected with inverse polarity, to guarantee the secondary side has a proper charge flow for energy extraction. When the voltage on

the piezoelectric transducer is at its maximum, the switch S_1 conducts (Lallart et al., 2011). Oppositely, the switch S_2 leads when the transducer voltage is at its minimum. Thereby the electrical energy flowing through the transformer is converted into magnetic energy. Owing the secondary windings, this energy is converted back to electrical energy and finally stored on the storage capacitor (C_S) and the load resistor (R_L) (Lallart et al., 2011).

The set-up transformer allows an artificial change in the load seen by the piezoelectric element, since the coupling factor is chosen to be higher than 1, which increases the transducer voltage. Therefore, this technique is suitable to extract energy from reduced input power levels (Guyomar, 2011).

Hybrid Synchronized Switch Harvesting on Inductor

As the name suggests, Hybrid SSHI, is the combination of two techniques, MR-SSHI and P-SSHI, as represented in Figure 10, taking advantage of their properties. Thus, it extracts energy in both the inversion and conduction phases (Lallart et al., 2011).

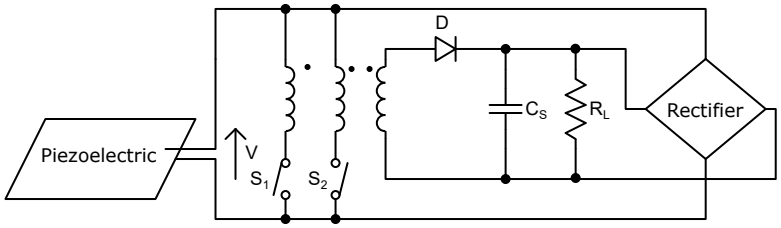


Figure 10: Schematic of the Hybrid SSHI rectifier.

The switch control works accordingly to the output voltage on the piezoelectric transducer. In such a way that, when the output voltage on the piezoelectric transducer is at its maximum, S_1 is closed. On the contrary, if the transducer voltage is at its minimum, the switch S_2 is closed. The current should flow from the piezoelectric source to the storage capacitor. For this reason, a diode (D) is implemented to ensure this flow and avoiding current backflow (Anna et al., 2018).

Both P-SSHI and MR-SSHI are operating when the maximum voltage across the piezoelectric transducer is higher than the output voltage from the rectifier; conversely, only MR-SSHI is operating. The MR-SSHI rectification technique is manly effective for high load values, howbeit the P-SSHI is mostly useful for middle values of the connected load (Garbuio et al., 2009).

Even though this technique does not improve the conversion enhancement, it endures extracting energy four times per period, as a result of working in both the inversion and conduction phases. The scavenge energy is

double in a period compared to the previous SSHI interfaces. Thereby, it widens the bandwidth of the load and still having relative independence from it.

According to Lallart et al. (2011), regarding the maximal harvested power, this technique features the same power limit as previous approaches. Nonetheless, its performance is better than both methods that integrate it separately. Moreover, the hybrid SSHI technique leads to a significant gain in terms of harvested power.

2.1.2 Load Decoupling Interfaces

Synchronized Switching and Discharging to a storage Capacitor through an Inductor

The circuit depicted in Figure 11 is the Synchronized Switching and Discharging to a storage Capacitor through an Inductor (SSDCI) interface (Guyomar, 2011).

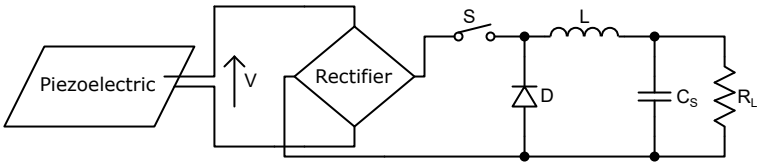


Figure 11: Circuit diagram of the SSDCI rectifier.

In this approach, the rectifier is directly connected to the piezoelectric element to prevent an electrical attenuation from the current flow. The principle of this method consists of transferring the energy available on the piezoelectric element to a storage capacitor (C_s) through an inductor (L). In this case, the switch S is closed anytime the voltage generated by the piezoelectric transducer reaches the maximum and minimum values. When the piezo-voltage equals zero, the rectifier stops the switching process. However, there is still energy in L, which is conveyed to C_s. Nevertheless, the circuits can also perform as a S-SSHI for high load values, since the piezoelectric voltage does not reach zero.

Synchronous Electric Charge Extraction

The Synchronous Electric Charge Extraction (SECE) technique is illustrated in Figure 12. Identical to the previous methods, the switch S remains open for most of the vibration period excepted if the piezoelectric voltage is at its maximum or minimum value. During the time the switch is closed, it is charging the inductor (L). Howbeit, while the switch is open, the inductor's energy accumulated is conveyed to the load stage (Tang and Yang, 2011).

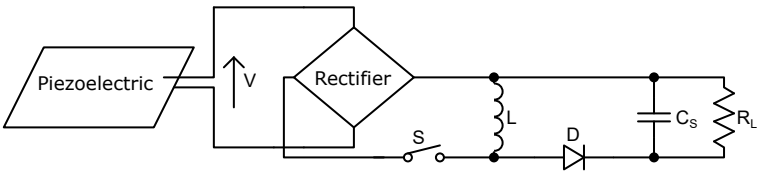


Figure 12: Schematic of the SECE and the PS-SECE recifiers.

The SECE technique is independent of changes in the load. Besides, this method is intrinsically self-adaptive to the environment, even in the case of random vibrations. The switch S prevents a direct connection between the output load and the piezoelectric device for most of the period. Thereby, the impedance seen by the piezoelectric element is almost constant (Guyomar, 2011).

The critical value given by the product of the squared coupling coefficient (k^2) by the mechanical quality factor (Q_M) works as a threshold value. Above $k^2 \cdot Q_M$, the maximum energy that can be extracted starts to decrease. Moreover, using the SECE technique, it is beyond to control the trade-off among energy extraction and the damping effect (Tang and Yang, 2011).

As reported by Lefeuvre et al. (2017), the amount of energy given by the SECE rectifier (W_{SECE}), at each closing of the switch is described in accordance to Equation 10.

$$W_{SECE} = \frac{1}{2} \cdot C_o \cdot V^2 \tag{10}$$

To improve the drawback aforementioned, Lefeuvre et al. (2017) proposed the Phase Shift Synchronous Electric Charge Extraction (PS-SECE) technique, also represented in Figure 12. The PS-SECE differs from the SECE approach in the switch control process, closing the switch triggered by the phase-shift (ϕ). Equation 11 describes the energy extracted from the piezoelectric element, $W_{PS-SECE}$, at each time the switch is closed.

$$W_{PS-SECE} = \frac{1}{2} \cdot C_o \cdot V_\phi^2 \tag{11}$$

As a result, the damping effect is controlled by varying the phase shift of the switching signal. This indicates the phaseshift can be used as a tuning parameter to control the converted power (Lefeuvre et al., 2017). Related to Equation 10, in Equation 11 the circuit losses are neglected.

Double Synchronized Switch Harvesting

The Double Synchronized Switch Harvesting (DSSH) technique is a result of combining the S-SSHI and SECE rectifiers, as depicted in Figure 13 (Lallart et al., 2008).

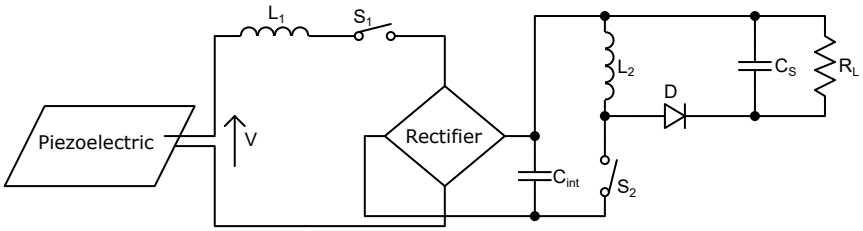


Figure 13: Circuit schematic of the DSSH, ESSH and ASSH rectifiers.

Analogous to SECE, the harvested power is almost independent of the connected load. In order to control the energy flow, two switches, S_1 and S_2, and a diode D, are implemented on the circuit. The energy available on the piezoelectric is driven to the inductor L_1 and the intermediate capacitor C_{int}, using the remaining energy for the inversion process, while S_1 is closed and S_2 opened. Then, the operating mode goes inversely, opening S_1 and closing S_2, and the energy is transferred from C_{int} to the inductor L_2. Finally, the energy is passed from the L_2 to the storage capacitor C_s and the load resistor, R_L.

Tuning the ratio between C_{int} and the piezoelectric element capacitance is an advantage of the DSSH technique over the SECE. This allows controlling the trade-off set by the amount of harvested energy and the damping effect.

Enhanced Synchronized Switch Harvesting

The DSSH can be further enhanced by the Enhanced Synchronized Switch Harvesting (ESSH) technique, which circuit schematic is represent in Figure 13. Since the circuit topology is the same, the difference between ESSH and DSSH is at the small amount of energy leaved on C_{int} by ESSH (Shen et al., 2010).

Usually, the switch S_1 is opened and is only closed for a brief time when the voltage generated by the piezoelectric element reaches its maximum or minimum, charging C_{int}. Differently, the switch S_2 is periodically closed, when the voltage drop across C_{int} exceeds a pre-set value, charging the inductor L_2. Otherwise, if the voltage drop across C_{int} is below the pre-set value, the switch S_2 opens, and the energy stored in L_2 is conveyed to the storage stage (Shen et al., 2010). Comparing to the DSSH, ESSH technique has better control of the abovementioned trade-off and lower sensitivity to a mismatch in the capacitance ratio (Anna et al., 2018).

Adaptive Synchronized Switch Harvesting

Another approach to optimize the ESSH technique is the Adaptive Synchronized Switch Harvesting (ASSH), also represented in Figure 13, that is designed for multi-mode vibrations (Shen et al., 2010). In the ASSH control technique, the switch S_1 is closed at least four times in a period, and an adjustable threshold coefficient controls it. While in ESSH, the switch S_1 closes twice in a period, every time the piezoelectric mechanical structure is at its maximum displacement. Therefore, for a single frequency excitation, the control law of ESSH is optimal (Anna et al., 2018).

Energy Injection

The energy injection technique, shown in Figure 14, is based on the SECE with an energy feedback loop from the storage stage to the piezoelectric element. The operation of this approach can be divided into three phases: harvesting, injection, and open circuit (Lallart and Guyomar, 2010).

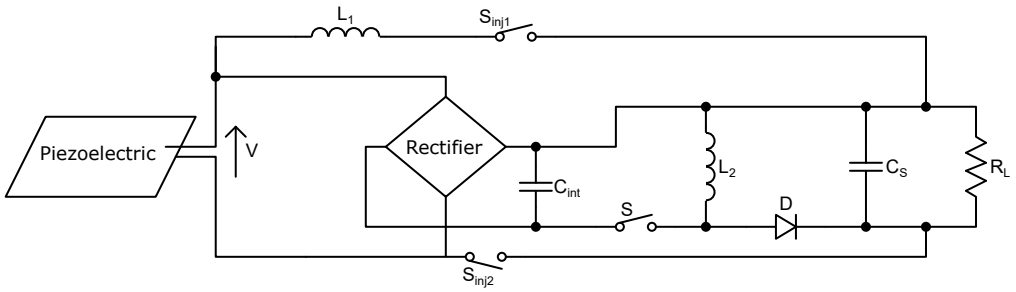


Figure 14: Circuit schematic of the energy injection technique.

Firstly, at the same time the piezo voltage modulus is at its maximum value, the switch S starts the harvesting phase, extracting energy from the piezoelectric element to the switch S and the inductor L_2. Afterwards, the two switches S_{inj1} and S_{inj2} control the energy injection process (Guyomar, 2011).

Contrary to the prior methods, this technique allows a bidirectional energy flow. Thereby, the forward energy, which goes from the piezoelectric transducer to the storage capacitor, is controlled by the switch. During this time, S_{inj1} and S_{inj2} are used to manage the reverse energy flow. This causes a power resonance phenomenon occurring at the optimal value of $k^2 \cdot Q_M$. Thanks to the bidirectional energy flow, this technique accomplishes higher outputs for different load values, leading to a more significant performance (Anna et al., 2018).

2.1.3 Switching Techniques Summary

The electronic interfaces can be divided into two classes. The first class to enhance the conversion establishes a direct connection between the piezoelectric element and the storage stage, named, Direct Energy Transfer. Due to this connection, the harvested power is strictly dependent on the connected load and, consequently, the extracted energy. In real-world applications, the load can suffer changes with time, according to the connected system state, and may not be fixed in advance. Therefore, to overcome this handicap, a second class was proposed using the same switching concept but applied differently.

The second class is the Load Decoupling Interfaces, where the inductance concept is used through an inductor as an energy storage element. This component is used to take advantage of magnetism and electricity's relationship when an electric current passes through the coil. The general operation of this category can be briefly described, starting with the piezoelectric element, through which, its energy is conveyed to the inductor. It is disconnected from the circuit, and the energy once provided to the inductor goes to the storage capacitor. As the name suggests, this interface category keeps the piezoelectric element from being straightly connected to the load stage. Hence, this leads to a process of accumulating energy independent of the connected system.

The following Table 2 organizes the literature architectures according to its class.

Table 2: State-of-the-art piezoelectric harvesting interfaces.

Direct Energy Transfer	**Load Decoupling Interfaces**
P-SSHI	SSDCI
S-SSHI	SECE
MR-SSHI	PS-SECE
Hybrid SSHI	DSSH
	ESSH
	ASSH
	Enegy Injection

For being part of the direct energy transfer category, all SSHI techniques are strongly dependent on the connected load. As an advantage, these approaches are self-powered, using off-the-shelf components and operating in a wide frequency range. In contrast, for the other techniques in the load decoupling interfaces category, implement a self-powered system is more challenging and complex due to the digital switch.

In microsystems, it is crucial to be careful about the design and implementation of the control system. Regarding the miniaturization of the device, the inductor and transformer can be seen as a limitation.

2.2 Voltage Amplifier

The piezoelectric transducers can be used on low power electronic devices to convert vibrations into electrical energy. The voltage generated by the piezoelectric element is quite small and proportional to the variation of pressure applied. Typically the amplitude is comprised in a range of a few $10\,mV$ to $10\,V$, depending on the structure construction. Additionally, it has a very high impedance.

Piezoelectric transducers generate little charge. As a result, it is not capable of providing voltage output levels that are high enough to be recognized by the rest of the circuit. Due to this problem, a voltage amplifier is required to amplify the signal to the desired level. Ideally, the amplifier features are infinite input impedance, zero output impedance, and gain independent of frequency (Gatti, 2014). Thereby, the piezo-voltage is increased and can be converted into a usable signal for the rest of the circuit.

2.2.1 Amplifier Modes

In response to mechanical stress, the piezoelectric material produces a charge compressed in the tens or hundreds of pico-coulombs per newton (pC/N). Although $1\,N$ is a relative amount of force, $100\,pC$ is a small amount of charge. Therefore, an amplifier is crucial. Typically, the high impedance of the piezoelectric sensor requires an amplifier with high input impedance, such as Junction gate Field-Effect Transistor (JFET) or CMOS input operational amplifiers. On the report of Karki (2000) two circuits are used for signal conditioning. If the amplifier is too close to the sensor, it is a voltage mode amplifier, as the one illustrated in Figure 15. Under other conditions, when the amplifier is remote to the sensor it is named a charge mode amplifier, illustrated in Figure 16. In both cases, the signal levels are set between $3\,V$ to $5\,V$.

Voltage Mode Amplifier

The output of a voltage mode amplifier depends on the amount of capacitance seen by the piezoelectric, which is associated with the interface cable. Any capacitance that is in parallel with the piezoelectric device change the relationship between the applied force and the output voltage. Thus, small changes in cable capacitance can

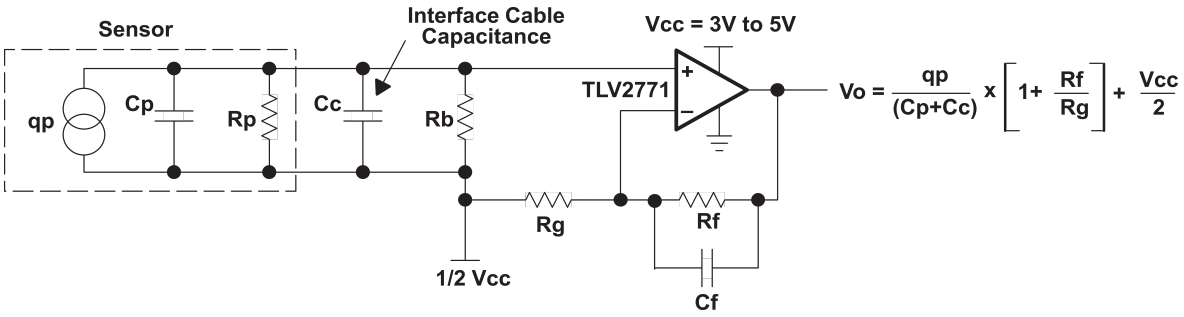


Figure 15: Circuit of a voltage mode amplifier.(Karki, 2000)

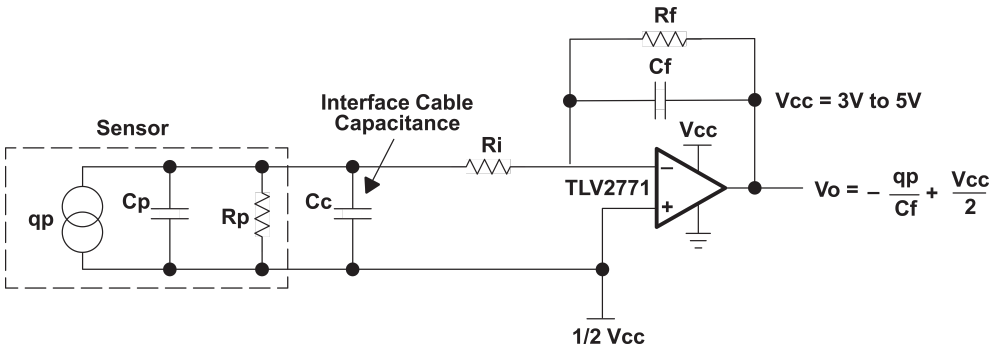


Figure 16: Circuit of a charge mode amplifier. (Karki, 2000)

have a massive impact on the system. For that reason, the voltage-mode amplifiers should be considered only when it is placed close to the sensor. The equation to measure the output voltage is depicted in Figure 15, and the maximum output gain is given by the factor $\left[1 + \frac{R_f}{R_g}\right]$. The upper ($f_H$) and lower ($f_L$) cut-off frequencies are expressed in Equations 12 and 13, respectively.

$$f_H = \frac{1}{2 \cdot \pi \cdot (R_p \parallel R_b) \cdot (C_p) \parallel C_c} \tag{12}$$

$$f_L = \frac{1}{2 \cdot \pi \cdot R_f \cdot C_f} \tag{13}$$

Assuming that R_f and C_f are the feedback resistor and capacitor, respectively, C_p and R_p are the piezoelectric capacitor and resistor, correspondingly, R_b is the bias resistor, C_c the sensor capacitance, and R_i the isolator resistor.

Charge Mode Amplifier

A charge-mode amplifier (Figure 16) transfers the charge injected into the negative input terminal of the amplifier by changing the feedback capacitor. Fundamentally, it converts the charge into voltage with high input

impedance, ensuring that the small amount of charge generated by the piezoelectric transducer does not dissipate.

The feedback resistor provides a DC bias path for the negative input and prevents the amplifier from saturating, making the circuit to behave like a high-pass filter at low frequencies. The lower cut-off frequency of the amplifier is set by the value of C_f and R_f, as described in Equation 13, and the upper cut-off frequency is expressed in Equation 14. An approximation for gain is given in Equation 15, where the smaller the capacitor, the greater the gain (Bartolome, 2010).

$$f_H = \frac{1}{2 \cdot \pi \cdot (R_i \parallel R_b) \cdot (C_p) \parallel C_c} \tag{14}$$

$$Gain = \frac{1}{C_f} \tag{15}$$

The main advantage of this kind of amplifiers is that its gain is independent of parasitic capacitance in parallel with the piezoelectric. However, according to Yaghootkar et al. (2017), these amplifiers are not suitable for the amplification of low voltage signal with a low power consumption. As a consequence of the small capacitance, the amplifier has difficulties to achieve a reasonable gain.

This method of signal conditioning can be improved by integrating Field Efect Transistor (FET) buffers into the circuit. Ideally, the buffer has high input impedance and low output impedance. The output voltage is equal to the input voltage, without any gain added, being used for Analog-to-Digital Converters (ADC), reference voltages, drive low-impedance loads, and so one (Feucht, 1990).

Convenient operation amplifiers for these tasks could be the Linear Technology LT1464/LT1465 (Lin, 1996) JFET dual input amplifier, which has $10^{12}\,\Omega$ input resistance and $1\,MHz$ gain-bandwidth product. Also, the TLV2771 (Tex, 2004) from Texas Instruments that inhere a rail-to-rail low power amplifier, also with $10^{12}\,\Omega$ differential input resistance and $5\,MHz$ unity-gain bandwidth. Those are good enough to handle the vibration ranges of piezoelectric sensors easily.

2.2.2 Piezoelectric Amplification Patents

In the USA, some approaches regarding piezoelectric sensors were patented. Firstly, an electrical circuit for the transferring and amplification of a piezoelectric transducer signal by Von (1973). This circuit employed a bipolar

piezoelectric sensor, a pre-amplifier and a differential amplifier. The bipolar sensor is connected to the two signal input terminals of an amplifier circuit. Then, the two output terminals from the pre-amplifier are connected to the input terminals of a differential amplifier, which only has one output terminal. Thus, the signals from the first amplifier are converted into an amplified single signal.

After, a piezoelectric sensor with FET amplified output was patented by Change Jr (1989). The circuit is made up of a unity gain amplifier that results in increased signal output and resolution. Moreover, negative feedback is implemented to cancel the capacitance of piezoelectric crystals, decreasing the noise level and providing voltage gain to the signal.

Lastly, a high-temperature piezoelectric vibration sensor assembly was suggested by Campbell et al. (2008), where a conditioning/processing circuit was proposed. It consists of having a charge differential amplifier combined with an integral trim adjusting capacitor and a voltage divider network to provide the ability to custom adjust input impedance, compensate the effect of parasitic capacitances and structural constraints.

2.2.3 Amplifier Topologies

According to Jung (2004), any high impedance transducers require an amplifier to convert the transfer of charge into a change of voltage. Due to the high DC output impedance of these devices, appropriate buffers are needed. The primary circuit for a charge amplifier is shown in Figure 17.

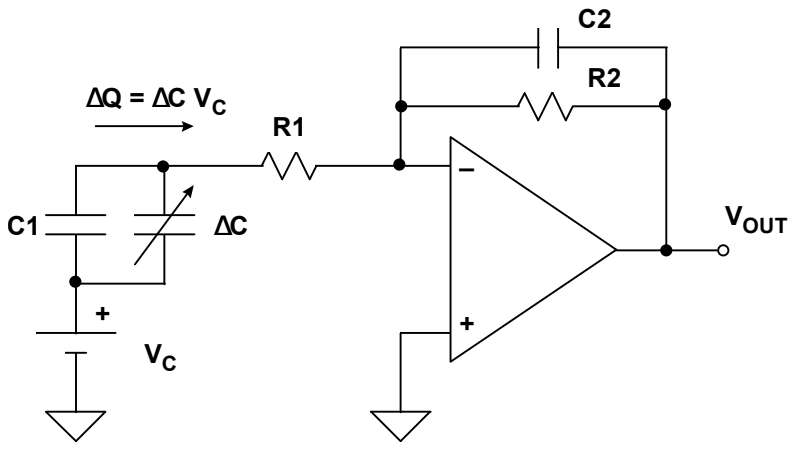


Figure 17: Schematic circuit of charge amplifier. (Jung, 2004)

For a capacitive transducer, the voltage across the capacitor (C_C) is a constant value. The change in the capacitance (ΔC) produces a charge that is transferred to the operational amplifier. Hence, the output voltage is given by Equation 16. Otherwise, if it is a charge-emitting transducer, it outputs a varying charge (ΔQ), and

the capacitance remains constant. The voltage across the transducer is constant due to a virtual ground of the operational amplifier. The charge is transferred to C2, and the output voltage is expressed by Equation 17.

$$\Delta V_{out} = \frac{-\Delta C \cdot V_C}{C2} \tag{16}$$

$$\Delta V_{out} = \frac{-\Delta Q}{C2} \tag{17}$$

A piezoelectric transducer amplifier that operates on low voltage supply, and reduced bias current is illustrated in Figure 18 (Jung, 2004). The reduction of bias current allows to lower power dissipation and to reduce leakage current. A particularity of this circuit is the AC coupling capacitor C1. Thanks to the implementation of C1, the amplifier operates over a range of $-55\,^{\circ}$C to $+125\,^{\circ}$C. In reverse, without C1, temperature range goes from $0\,^{\circ}$C to $+85\,^{\circ}$C.

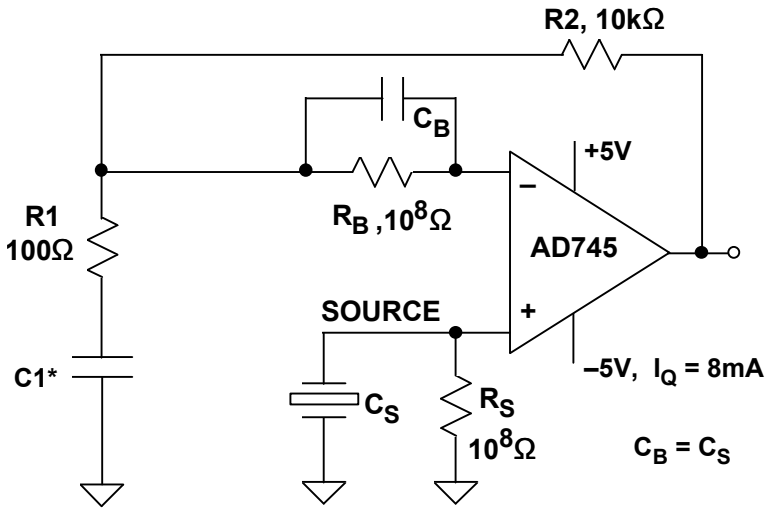


Figure 18: Schematic of a piezoelectric sensor amplifier. (Jung, 2004)

The AD746 (Ana) is a JFET amplifier suitable for high-gain pre-amplifier, that provides high gain and wide bandwidth. Moreover, it operates with extremely low levels of distortion, less than 0.0002% at $1\,kHz$ (Jung, 2004).

Li et al. (2011) implemented a circuit composed by a voltage pre-amplifier and a filtering module, to carry the signal from the piezoelectric element. A schematic of this circuit is presented in Figure 19. As a consequence of high impedance and low charge of piezoelectric, a JFET input operational amplifier, which impedance is up to $10^{12}\,\Omega$, is used to pre-amplify the piezo-voltage with a factor of 11. These amplifiers can pick up the voltage at a

mV scale. To eliminate the noise induced by the power supply, a Butterworth band-reject filter is applied (Li et al., 2011). Therefore, the piezo-voltage is amplified, and the noise filter removes noise from the signal.

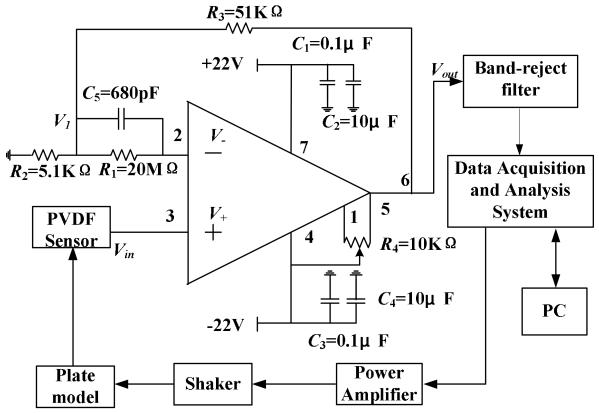


Figure 19: Circuit diagram of the vibration system. (Li et al., 2011)

To amplify a small signal using an operational amplifier, a dual power supply is needed since the output voltage cannot be larger than the voltage supply, as requested by Jeong et al. (2019). Although a voltage driver is capable of making dual-polarity from one voltage source, it dissipates power and requires additional components, increasing the system size. Instead, Jeong et al. (2019) used two piezoelectric elements as a single harvester, having two independent sources. Consequently, it can provide higher power generation than when using only one piezoelectric device.

The circuit designed by Jeong et al. (2019) is shown in Figure 20. Since the output voltage of the amplitude cannot be larger than the voltage supply, a higher voltage needs to be applied to produce an appropriate amplitude. In this case, only a positive voltage is used to supply the amplifier, which implies that the output voltage have not negative values. In order to amplify the input signal with positive and negative sides, a bipolar voltage is used to supply both power terminals of the amplifier. Two diode bridge rectifiers, D1 and D2, rectify the energy generated by the piezoelectric elements to be stored in capacitors C_{rect1} and C_{rect2}, as the shape of the signal generated by both piezoelectrics is sinusoidal. Further, the output gain can be easily adapted to the end-user requirements, by tuning the resistor R_f.

Another option to pre amplify the piezo voltage is a booster, as stated by Barcola et al. (2016) and shown in Figure 21. The booster is a nonlinear circuit composed of inductance and two switches, implemented on a SSHI interface. Its working principle consists of detecting the extremum of the output voltage from the piezoelectric element (u_p) and, consequently, close the switch. This process occurs during a brief time relative to the period ($\frac{1}{f_0}$). Thereby, the output voltage u_b is a combination of the voltage from the inductor and that from the piezo-

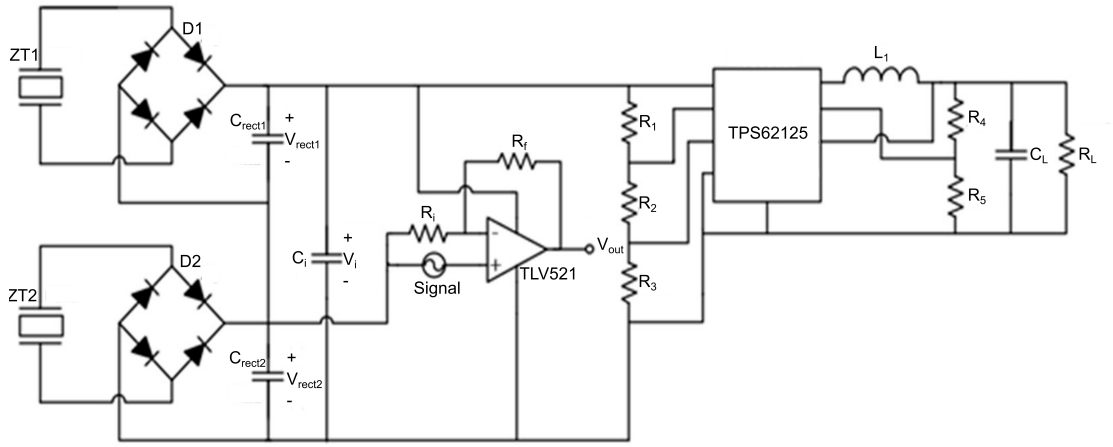


Figure 20: Circuit diagram of the operational amplifying system. (Jeong et al., 2019)

electric transducer. Nonetheless, in terms of gain, this approach needs to be improved because it is not capable of amplifying high values, thanks to the consumption of the components.

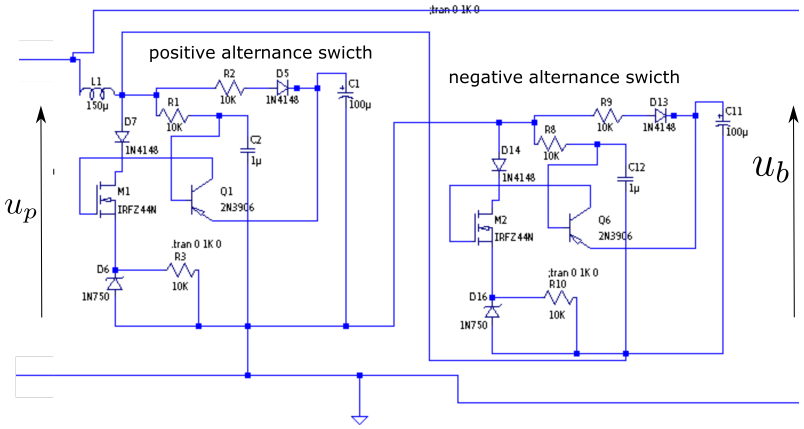


Figure 21: Schematic circuit of a booster. (Barcola et al., 2016)

2.3 Rectifier

The harvesters produce an incoming AC signal that needs to be converted into a DC signal through a rectifier (Herbawi et al., 2013). This procedure should involve a device that only allows one way of current flow. Under DC operating conditions, the storage capacitance (C_s) is given by Equation 18, where I_D is the current flowing through the forward-biased junction; τ_T is the carrier lifetime; V_T is the thermal voltage, and n is the number of free electrons in the material (Baker, 2010). Due to C_L, the ripple result from the AC-DC conversion can be reduced, smoothing the DC voltage (Peters et al., 2007). During the time the voltage from the rectifier is higher

than that of the capacitor, C_s charges up. Howbeit, when the rectifier voltage drops down, C_s provides the required current from its stored charge. Thus, C_s can supply charge anytime when it is not available from the rectifier.

$$C_s = \frac{I_D}{n \cdot V_T} \cdot \tau_T \tag{18}$$

The vibrational energy harvesting systems have a broadband operating frequency range with low output power and voltage (Yang et al., 2013). Therefore rectifiers with high Power Conversion Efficiency (PCE) are fundamental (Peters et al., 2011). In ultra low power circuits, there is a high risk of leakage current through both source-bulk and drain-bulk connections, causing some power dissipation and decreasing the efficiency. A recent trend to address this problem is the Bulk Regulation (BR) technique (Yang et al., 2013).

2.3.1 Conventional Rectifier

Half and full-wave rectifiers using diodes are known as conventional rectifiers. They are common in high voltage applications, whereas for low voltage integrated circuit functions, the PCE is significantly reduced (Li et al., 2014).

Half-Wave Rectifier

The simplest structure for a rectifier circuit is the half-wave rectifier depicted in Figure 22. This kind of circuit only allows the positive half of the AC input signal to pass through to the storage stage, eliminating the negative values, as shown in Figure 23. The output zero volts occurs when V_{in} is less than the voltage drop on the diode (V_D) and on the contrary, when V_{in} is higher than V_D, the output is the difference between them ($V_{in} - V_D$). Usually, the voltage drop is around $0.7V$.

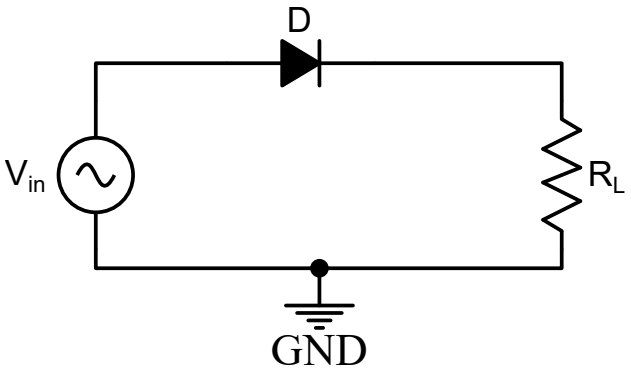


Figure 22: Schematic circuit of the half-wave rectifier.

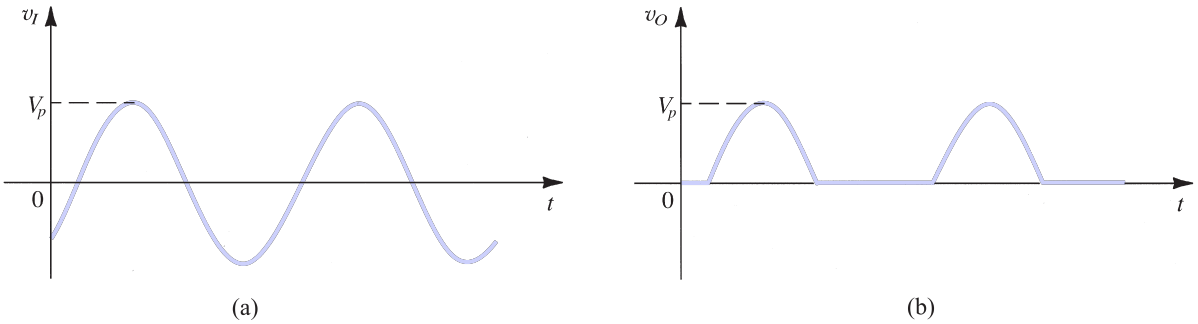


Figure 23: Half-wave rectifier: (a) input waveform and (b) output waveform rectified. (Sedra and Smith, 2014)

The rectifier operates ineffectively when the input voltage peak is approximate from the V_D value. These rectifiers have very low efficiency. However, its simplicity is an advantage over more complex schematics.

Full-wave Rectifier

When it is necessary to rectify both half-cycles of the input waveform, a full-wave rectifier configuration must be employed. A simple schematic to implement this concept is a full-wave bridge rectifier as suggested by Jain and Joshi (2018) and illustrated in Figure 24. This circuit consists of four diodes (D_1, D_2, D_3, D_4) and stands out for giving a small output ripple voltage, commonly used in high voltage applications, where the diode forward voltage drop of $0.7\ V$ to $1\ V$. For low-voltage applications, these values result in a large number of voltage losses, reducing the PCE significantly (Lam et al., 2006).

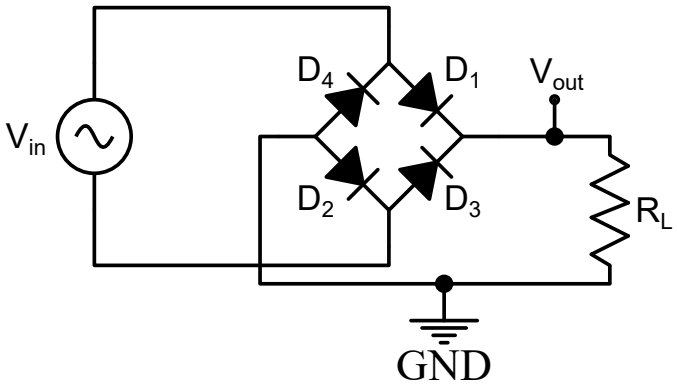


Figure 24: Schematic circuit of the full-wave rectifier.

The positive half-cycle is driven by D_1 and D_2, while the negative half-cycles flows via D_3 and D_4. The current flows up to the load, regardless of the polarity of the input. Due to this, it has twice the voltage drop than rectifier mentioned above and highly reduces the available output voltage (Figure 25). Nevertheless, this is an advantage in low voltage power supplies.

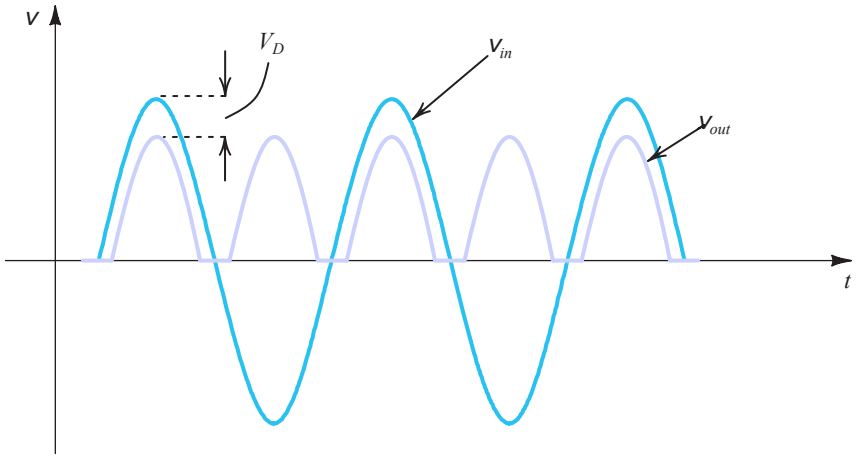


Figure 25: Input and output waveforms of a full-wave rectifier. (Sedra and Smith, 2014)

Diodes

A crucial phase when designing a convectional rectifier is to choose the diode to implement. There are some essential things to take into consideration. Firstly, the amount of current the diode can operate with is based on the maximum current that is expected to pass through the rectifier. Furthermore, afterwards, the peak inverse voltage, which should be as higher as possible to avoid reverse current across the diode.

Standard pn-junctions diodes suffer latch-up and low switching speed, both features not suitable for frequencies in MHz range (Peters et al., 2011). When the signal amplitude becomes less than the threshold voltage (V_{th}), diodes cannot play a rectifier role (Babacan, 2018).

Schottky diodes are a semiconductor that can be utilized for detecting and rectifying sinusoidal waves with a low forward voltage drop between 150 and 450 mV, suitable for the low power application (Partal and Belen, 2019). This diode is made by a metal-semiconductor junction named the Schottky barrier (Brezeanu et al., 2001) and is represented in Figure 26. Usually, the cathode is n-type silicon, while the anode is metal like platinum, chromium or tungsten. Therefore, the forward voltage depends on the choice of material used for the junction.

This diode can be employed to enhance efficiency and replace the standard diode, due to its excellent high-frequency behaviour, low forward voltage, fast switching speed and independence from the recovery time (Lam et al., 2006; Akkermans et al., 2005). One of the little limitations of the Schottky diodes is the breakdown voltage (Milanovic et al., 1996; Banu et al., 2012).

The diode needs to be modeled by the electric circuit shown in Figure 27 using Simulation Program with Integrated Circuit Emphasis (SPICE) parameters (Cadence, 2016). The model consists of a substrate resistance R_s, a junction capacitance C_j and a junction resistance Rj.

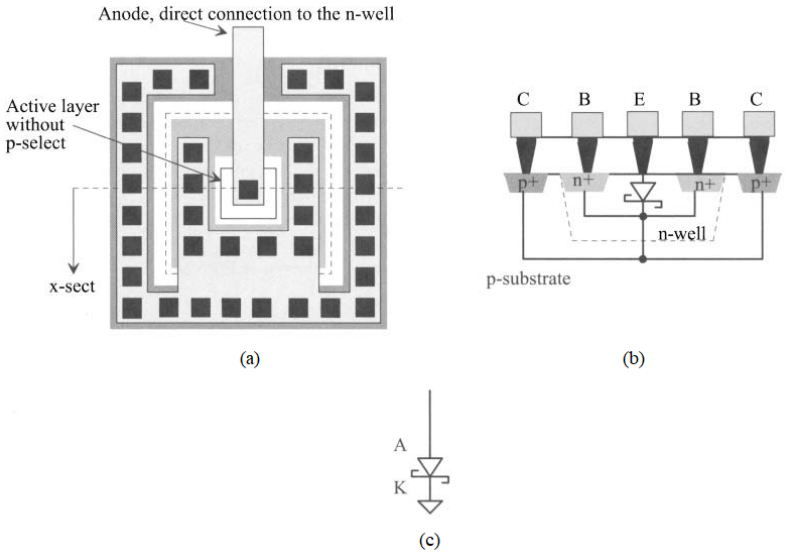


Figure 26: Schottky diode: (a) layout, (b) cross-section and (c) symbol. (Baker, 2010)

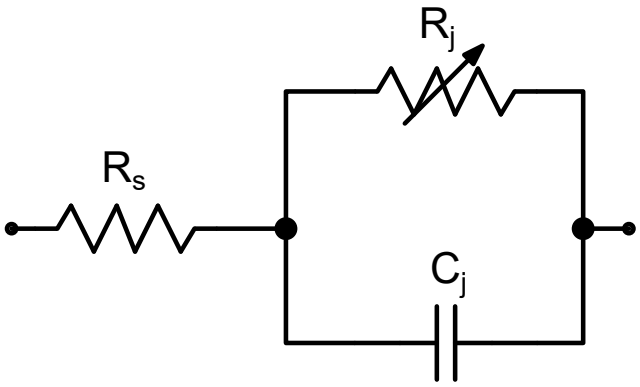


Figure 27: Schottky diode equivalent linear circuit model.

The total impedance of the linear model, Z_T, is given by Equation 19 as suggested by Kasi et al. (2012). In this equation, the values of R_j and C_j are constants, and the operation frequency, w, is the only variable parameter.

$$Z_T = R_s + \frac{R_j}{1 + j \cdot w \cdot R_j \cdot C_j} \tag{19}$$

The R_j is expressed in Equation 20, where I_b is the bias current, I_s is the saturation current, T corresponds to the temperature in kelvin and N is the ideality factor (Ali et al., 2014). At low bias levels, the voltage drop across R_s is insignificant, and the Schottky barrier dominates the diode behaviour. Contrarily, at higher bias levels, the ohmic resistance R_s dominates.

$$R_j = \frac{8.33 \cdot 10^{-5} \cdot N \cdot T}{I_b + I_s} \tag{20}$$

For energy harvesting applications, the most common is a zero bias Schottky diode model, such as HSMS-2850 in Devi et al. (2012); Kasi et al. (2012) fabricated by Agilent (2005). Albeit its advantages, the expensive production cost and high reverse leakage current are not rewarding compared to a standard CMOS process. A significant voltage drop is not tolerated for the vibrational energy harvesters. Thereby, the implementation of common and Schottky diodes should be avoided in conventional rectifiers (Raisigel et al., 2007).

For some applications, the diodes' voltage drop can be an issue. It is considering that a diode only starts to conduct when the voltage across its terminals reaches a threshold, meaning that the diode is not capable of emulating the entire positive half of the input signal. Besides, the use of diodes results in high power dissipation.

Summary

Table 3 gives an overall view of some conventional rectifiers previously mentioned.

Table 3: Comparison of the state-of-the-art of convencional rectifier topologies.

Topology	**Features**	**Comments**
Half-wave (Li et al., 2014)	Only allows an half of the AC input waveform to pass through to the storage stage.	⊙ Simple schematic; High voltage applications. ⊗ Low efficiency.
Full-wave bridge (Jain and Joshi, 2018)	It is four diode bridge configuration that full uses both half-cycles of the sinusoidal input signal.	⊙ Small output ripple voltage; High voltage applications. ⊗ Reduced PCE in low voltage applications.
Standard diodes (Peters et al., 2011)	Forward voltage $\approx 0.7\,V$	⊗ Latch-up; Slow switching; Small frequency range.
Schottky diode (Raisigel et al., 2007)	Forward voltage $\approx 150\,mV$ to $45\,mV$; Made by a metal semiconductor junction.	⊙ Wide frequency range; Low forward drop; Replace the standard diodes. ⊗ Expensive production; Reverse leakage current.

⊙ Advantage, ⊗ Disadvantage.

2.3.2 CMOS Rectifier

Rectifiers implemented on CMOS technology have been proposed to replace the conventional rectifiers above mentioned (Raop et al., 2012). In CMOS implementation circuits, Metal-Oxide-Semiconductor (MOS) transistors

in a diode configuration, meaning gate terminal connected to the drain terminal, are widely exploited (Li et al., 2014).

The transistors conduct current if the forward voltage exceeds the Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) V_{th}. The PMOS transistors' bulks must be connected to the highest potential and the NMOS to the lowest (Peters et al., 2007). These connections are helpful to avoid leakage currents and latch-up and were used in the past in many studies (Peters et al., 2011). The voltage drop over a MOS diode is related to transistor's V_{th}, which depends on the process and temperature used during fabrication (Peters et al., 2008). In Peters et al. (2007), one transistor connected as a diode in each path is replaced with a switch driven by the alternating input voltage. Due to this, every half-wave rectifier is used, and only one voltage drop occurs as a result of its conduction that takes place in pairs. However, four switches can not be applied in this way; otherwise, current backflow occurs.

A Dynamic Threshold Voltage MOSFET (DTMOS) is a technique to reduce V_{th} and power dissipation proposed by Bokor et al. (1997). It takes over from the conventional MOS diode, thanks to escaping reverse current. This technique is based on having the gate tied to the bulk terminal, as shown in Figure 28. Due to this, V_{th} becomes lower, and when implemented in a rectifier circuit provides less power consumption and, consequently, reduces power dissipation (Babacan, 2018). A PMOS can implement this connection in an n-well process or an NMOS in triple-well processes (Cardoso, 2010), although it is more expensive than a p-channel. With lower power consumption and dissipation, the prior techniques can allow the DTMOS to perform as an ideal diode for low voltage operation (Babacan, 2018).

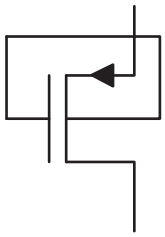


Figure 28: DTMOS configuration. (Babacan, 2018)

CMOS integrated rectifiers are roughly divided into two main groups: passive and active rectifiers. Despite advances in CMOS technologies, there is still an issue with high V_{th}. Research has been done, and many solutions intend to increase the efficiency of these circuits (Herbawi et al., 2013). A few configuration techniques can optimize the PCE and decrease the V_{th}: V_{th} cancellation techniques, since the voltage drop depends on the V_{th} (Junior et al., 2018; Lam et al., 2006; Kotani and Ito, 2009), circuits with active diode using Operational

Amplifier (op-amp) (Junior et al., 2018; Safari et al., 2018; Sun et al., 2012; Kakoty, 2011), bridgeless AC-DC converters (Junior et al., 2018) and Dickson charge pump (Wong et al., 2016).

Configuration Techniques

Rectifier topologies based on the V_{th} cancellation techniques aim to decrease the voltage drop through the rectifier to obtain more significant output voltage levels across the load (Junior et al., 2018). Application in standard CMOS processes could reduce the turn ON threshold by adding biasing circuits. This implies that the gate-to-drain voltages are fixed, and the gate drive voltages are controlled by the drain-to-source voltages that change slightly depending on the conduction. Therefore, the switches do not turn ON and OFF entirely, leading to inefficient rectification (Lam et al., 2006). Usually, the transistors are in the cut-off region, operating near the linear region. As a consequence, there is a reduction of the PCE, once the leakage current is increased (Junior et al., 2018).

The V_{th} techniques can be divided into three, as proposed by Kotani and Ito (2009): External V_{th} Cancellation (EVC), Internal V_{th} Cancellation (IVC) and Self-V_{th} Cancellation (SVC). In EVC, sown in Figure 29(a), the bias is generated with a switched capacitor circuit between the gate and the drain of the NMOS, requiring an external power supply and clock. The output voltage is given by Equation 21.

$$V_{out} = 2 \cdot \left(V_{in} - V_{th} + V_{polarization} \right) \tag{21}$$

In IVC, illustrated in Figure 29(b), the gate bias voltage came internally from the output DC voltage by a bias generation circuit (Raben et al., 2012). There is a degradation of the PCE to the passage of DC, due to power dissipation. It works in a large input power current, but not under small input power conditions.

In SVC, depicted in Figure 29(c), the gate electrodes of the NMOS and PMOS transistors are connected to the output and ground terminals, respectively. This connection boosts the gate-source voltage of the transistors as much as possible, reducing V_{th}. The V_{th} of the transistors is proportional to the output voltage, so equivalently decreases the same amount to both. SVC is the simplest technique and requires no additional power supply, resulting in a possible better PCE.

Nguyen et al. (2014) proposed enhanced IVC technique as shown in Figure 30 that consists of combine the conventional IVC and switches to improve PCE and voltage efficiency. The switching systems were implemented to create a pulse signal, that applied to the gates of M_1 and M_2 results in a better control of their operation state, reducing the reverse leakage current. These switches are carried out by PMOS and NMOS (SP1, SP2, SN1

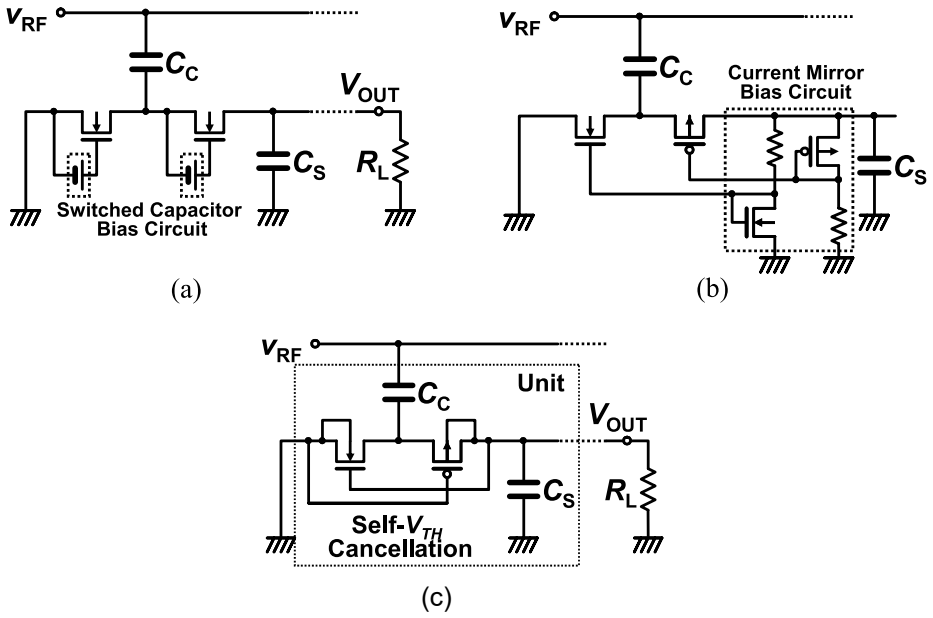


Figure 29: Circuit of the (a) EVC, (b) IVC and (c) SVC techniques. (Kotani and Ito, 2009)

and SN2), and their switch speed is not fast enough to avoid reverse current. Therefore, the body effect reduces the threshold voltage and consequently improve the switching time of SN1. Further, also the switching time of SP2 in improved by decreasing its gate voltage. As a result, no reverse current flows through M_1 and M_2 in OFF period, resulting in a raising of PCE, up to 80%.

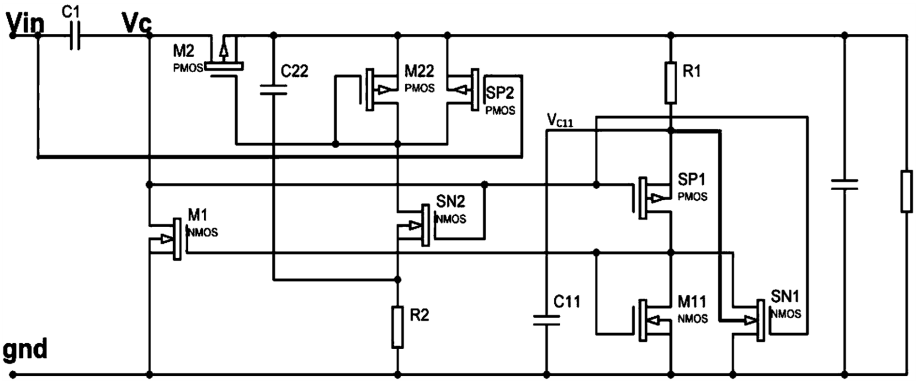


Figure 30: Schematic of the IVC technique combined with switches. (Nguyen et al., 2014)

Rectifiers with active diode based on op-amp are adopted for applications that require high accuracy in the range of V_{th}. A disadvantage of this technique is the high distortion during the zero-crossing of the input signal. This happens when diodes switch between ON and OFF states (Safari et al., 2018). Besides, the performance of the rectifier is restrained by the gain-bandwidth of the op-amp (Virattiya and Knobnob, 2011). This topology is not feasible for energy harvesting since, according to Junior et al. (2018), it increases energy consumption due to external supply voltage.

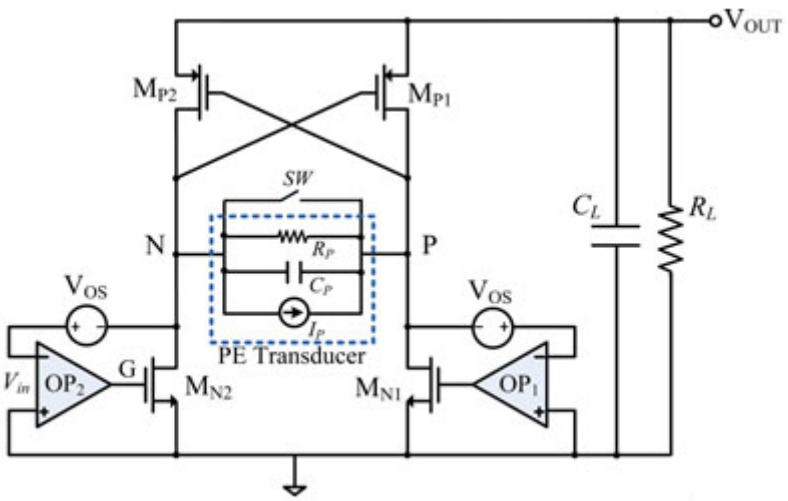


Figure 31: Schematic of a rectifier combining an active diode with an op-amp. (Sun et al., 2012)

In Sun et al. (2012), an active full-bridge rectifier is presented and exhibited in Figure 31. The dc-offset problem of the comparator based on an active diode is solved by replacing the passive diodes with an op-amp and adding a switch in parallel with the transducer. The NMOS transistor is combined with the op-amp, while the PMOS are configured in cross-coupling. Due to this, the voltage drop reduces and extracts more power from the transducer, leading to better efficiency.

The rectifier operation can be divided into three states. Firstly, no current flows through M_{P1} and M_{P2}, since I_p is charging C_p. When the voltage on the transducer is higher than the V_{th}, M_{P1} turns ON. In state 2, although M_{P1} works as a closed switch, M_{N2} remains OFF, and there is no current flowing to the output. As I_p keeps charging C_p, the voltage on the transducer is increasing and the op-amp turns ON M_{N2}. Finally, in state 3, the current flows to the output charging C_L, since both transistors M_{P1} and M_{N2} are ON.

In Kakoty (2011), a standard CMOS op-amp with three subsections stages followed by an output buffer is reported (Figure 32). It employs a Miller capacitor and is balanced with a current buffer compensation technique.

The first sub-circuit is a differential gain stage that incorporates a current mirror active load with three distinct advantages. Primary, the use of active load devices creates a significant output resistance in a relatively small amount of die area. Secondly, the current mirror topology performs the differential to the single-ended conversion of the input signal. Finally, the load also helps with the common-mode rejection ratio. The maximum and minimum output voltage of this stage is limited by keeping a PMOS in saturation and the voltage of an NMOS gate, respectively (Baker, 2010). The purpose of the second gain stage is to provide an additional gain for the output amplifier. The third stage is a bias string, which makes uses of three transistors and a current source.

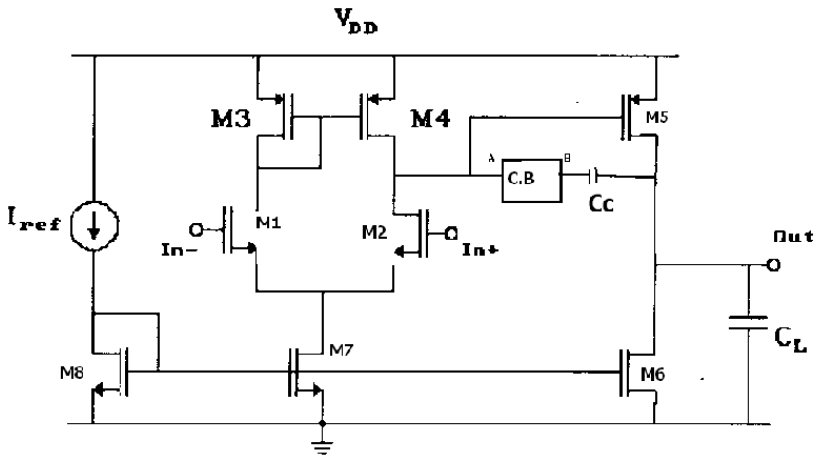


Figure 32: Circuit of an op-amp with a compensation block. (Kakoty, 2011)

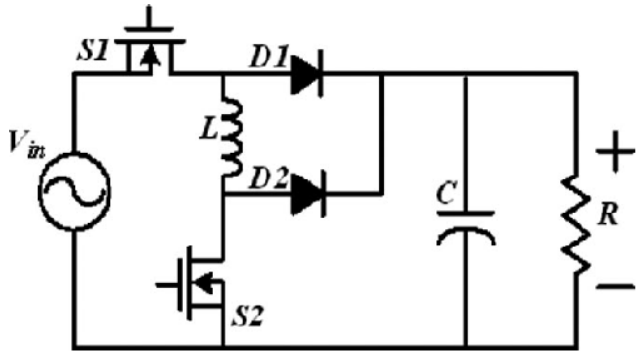


Figure 33: Circuit of a bridgeless rectifier. (Wang et al., 2013)

Bridgeless AC-DC converters use inductors to increasing the PCE specially for low-voltage applications (Junior et al., 2018). A bridgeless rectifier was suggested by Wang et al. (2013), as represented in Figure 33, integrating a boost and a buck-boost converters. The circuit operates in the boost mode when the input voltage, V_{in}, is positive, turning On the transistor S_1 and the diode D_1 is reverse biased. When the input waveform becomes negative, the switch S_2 turns ON and D_2 is reverse biased. Thus the circuit operated under the buck-boost mode.

Dickson charge pump is known as a switched capacitor with a voltage gain higher than one, also commonly called voltage multiplier. It is responsible for amplifying the signal without distortion of the input waveform. This technique is a DC to DC converter and is not a rectifier since it is not capable of separate the input signal between positive and negative cycles. However, with some modification, it could be transformed into a rectifier. The aim is to optimize features as leakage current, output voltage and rise time to improve the PCE (Ballo et al., 2019).

In Dickson (1980), a solution was patented, reported in Figure 34. The Dickson charge pump is made up of NMOS transistors, with the bulk connected to the ground, and the gate coupled to a forward node, avoiding

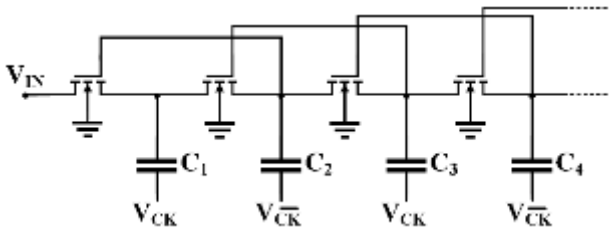


Figure 34: Dickson charge pump with NMOS transistors. (Ballo et al., 2019)

voltage losses due to the transistor threshold voltage. Its main handicap is the reverse current that follows anytime the charge transfer switch is turned off, resulting in a reduction of PCE.

The topology presented in Figure 35 is a general block scheme proposed by Wong et al. (2016), where the Dickson charge pump is connected in parallel with the voltage doubler. Focusing on the first stage, during the negative half-cycle, the first diode is activated and charges the first capacitor while the other diode is in the cut-off. Otherwise, the second diode is activated, charging the second capacitor, while the first diode is cut-off. To enhance the performance, instead of using a diode-connected MOSFET, a Ultra-Low Power (ULP) diode was implemented, since those have lower leakage current and higher output voltage. Consequently, the efficiency achieved increased from approximately 8% using MOSFETs to around 17%.

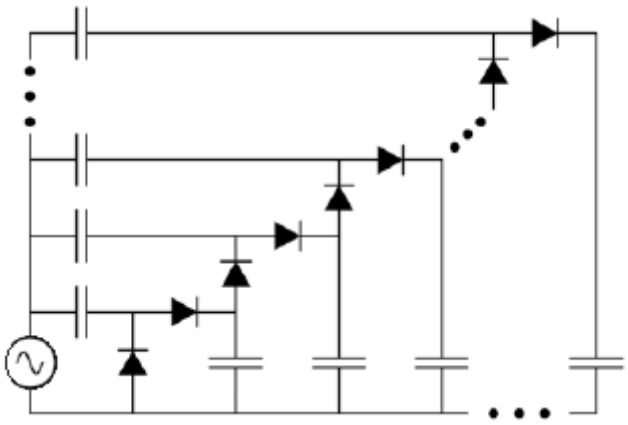


Figure 35: Dickson charge pump rectifier. (Wong et al., 2016)

Passive Rectifiers

Passive rectifiers implemented in a conventional IC process using diodes are discussed previously. As a result of the power losses, the forward voltage drop and the leakage current within full-wave rectifiers using diodes, MOSFETs replace them in a diode tied configuration. The efficiency of the circuit strongly depends on the transistor's threshold voltage, especially if the MOSFET is not completely turned ON or OFF.

In order to improve the power and voltage conversion efficiency, the forward voltage drop should reduce. It can be reduced in designs where the input directly drives the devices. A full-wave rectifier with parallel transistors was proposed by Le et al. (2006), as represented in Figure 36. Since in a conventional full-wave rectifier the voltages loss is equivalent to two diodes voltage drop, the circuit inside the dotted box is used to overcome this obstacle. The operation principle is similar to the conventional rectifier. The positive half-cycle of the input waveform flows through D1, when the input voltage, at least one diode voltage drop higher than the output voltage, charges the holding capacitor. The capacitor is also charged towards by the diode D2. By this reason, the voltage held on the capacitor is given by Equation 22. Alternatively, the bottom portion of the circuits conducts for the negative half-cycle, coupling the input voltage to the ground. Moreover, the voltage loses thanks to the diodes voltage drop, causes an increase in power dissipation. Furthermore, even with all the capacitors off-chip due to their large sizes, the die of this circuit still occupies a large area attributable to the diodes.

$$V_{out} = V_{in} - 2 \cdot V_{th} \tag{22}$$

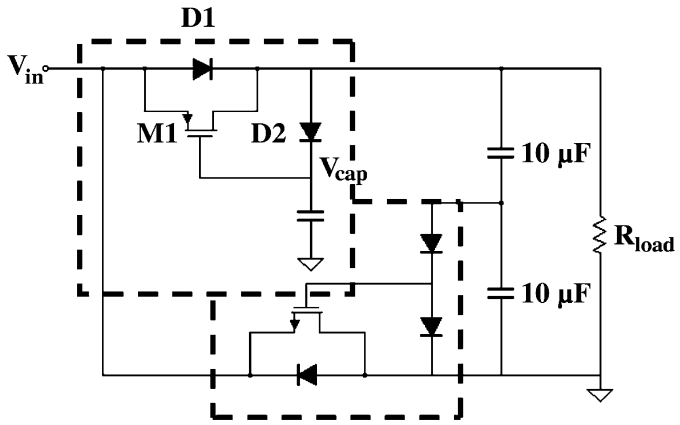


Figure 36: Circuit design of a full-wave passive rectifier. (Le et al., 2006)

To enhance the previous circuit, a full-wave rectifier with gate cross-coupled was designed by Cha et al. (2012), and is illustrated in Figure 37. In this way, the transistors' gates are cross-connected, meaning that the transistor conducts the current polarization opposite to the one that activates it. The maximum output voltage of this rectifier is achieved by Equation 23. This configuration reduces the reverse current compared to the previous full-wave rectifiers. Nonetheless, when the transistors are turned OFF, some reverse current keeps flowing through them, dissipating energy and, consequently, decreasing the efficiency.

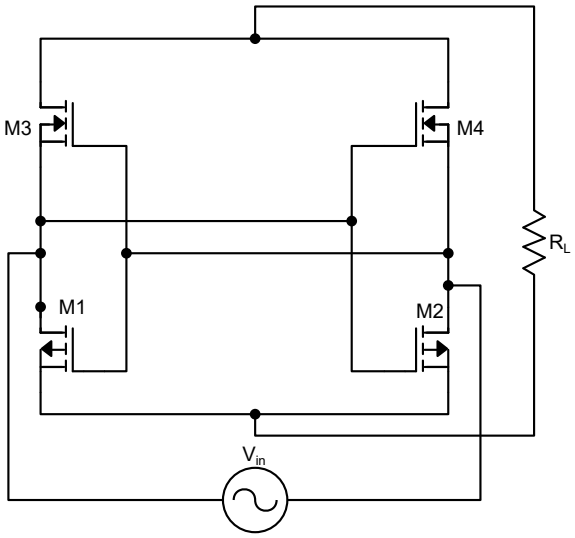


Figure 37: Schematic of a full-wave cross-couple rectifier.

$$V_{out} = 2 \cdot V_{in} - 2 \cdot V_{th} \tag{23}$$

Regarding to the voltage and PCE, even though passive rectifiers have simple structures, with MOSFETs tied as diodes, and can incorporate techniques to reduce the V_{th}, they still have lower performance than active rectifiers. Although they handle high input frequency applications, for low input voltage amplitudes, the remaining voltage drop reduces the performance. Thus, passive rectifiers have lower performance than active rectifiers (Peters et al., 2011).

Active Rectifiers

Active rectifiers increase efficiency throughout active signal control mechanisms that interfere with the rectification process. Those use controlled switches and high-gain comparators, providing reduced forward voltage compared to other mechanisms described above. Nevertheless, they control circuits constitute an additional power consumption for the system and, in some situations, can require limited supply. Low power consumption and capacity to handle low input amplitude signals are basic needs (Sun et al., 2016). Active rectifiers aim to behave as an ideal diode, which implies no voltage drop in forwarding direction and no reverse current. Usually, these rectifiers are supplied from the C_L, and high-efficiency is achieved through a low power control sub-circuit Peters et al. (2011).

Alternatively to a full-wave passive rectifier, a cross-coupled schematic was suggested by Hashemi et al. (2009), to enhance the efficiency and output voltage. Figure 38 represents the implemented circuit where $M1$ and $M4$

replace two diodes in a conventional full-wave rectifier. During positive cycles, $M1$ conducts neglecting the resistive drops. When the input signal is higher than the output signal the current flows trough $M8$, a low voltage is applied to the gate of $M6$, which puts $M6$ conducting and consequently, also $M4$. The performance of the circuit is influenced by the switching time and conditions. This structure increases the efficiency by 10% compared to a gate cross-coupling passive rectifier.

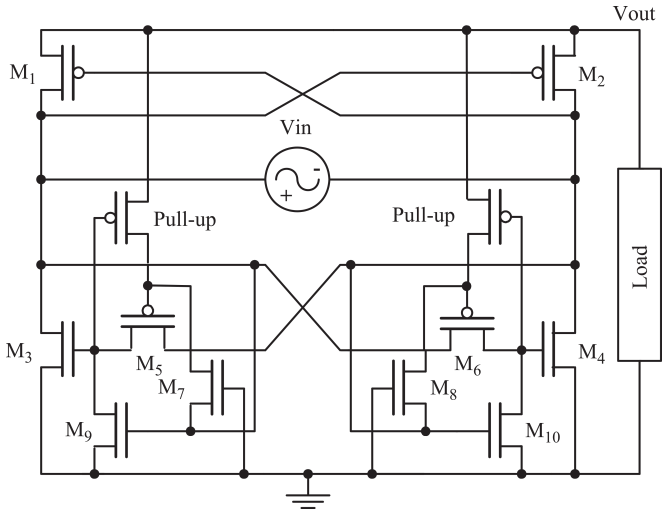


Figure 38: Schematic of the full-wave cross-couple rectifier. (Hashemi et al., 2009)

A full-wave active rectifier is reported in Lam et al. (2006) with two dynamically biased and symmetrically matched active diodes, D1 and D2 (Figure 39(a)). Each active diode is performed by an NMOS switch driven by a comparator, exhibited in Figure 39(b), that incorporates a reverse-current control and a 4-input with common gate input stages.

The active diode D2 is turned ON when $V_{C1} > V_{C2}$ and M_{P4} is activated. To achieve this conditions, V_{ac} is higher than V_{dc} and V_{C2} drops below V_{GND}. Thereby, V_{dc} is charged by D2 and M_{P4}. After V_{ac} reaches a peak it starts to decrease, V_{C2} rises, turning of the active diode. On the contrary, when $V_{C1} < V_{C2}$ and M_{P3} is turned ON, D1 is activated. The transistor M_{N1} should be activated when the condition described in Equation 24 is respected. In order to accomplish that action a comparator is implemented.

$$V_{C2} - V_{dc} > V_{C1} - V_{GND} \tag{24}$$

The transistors $M1$ to $M8$ from Figure 39(b) work as a two-stage comparator with common-gate input stages. $M1$, $M2$ and $M7$ are employed to monitor the voltage across M_{N1}, while $M3$, $M4$ and $M8$ monitor the voltage drop of M_{P3}. Moreover, $M9$ is implemented to control the reverse current.

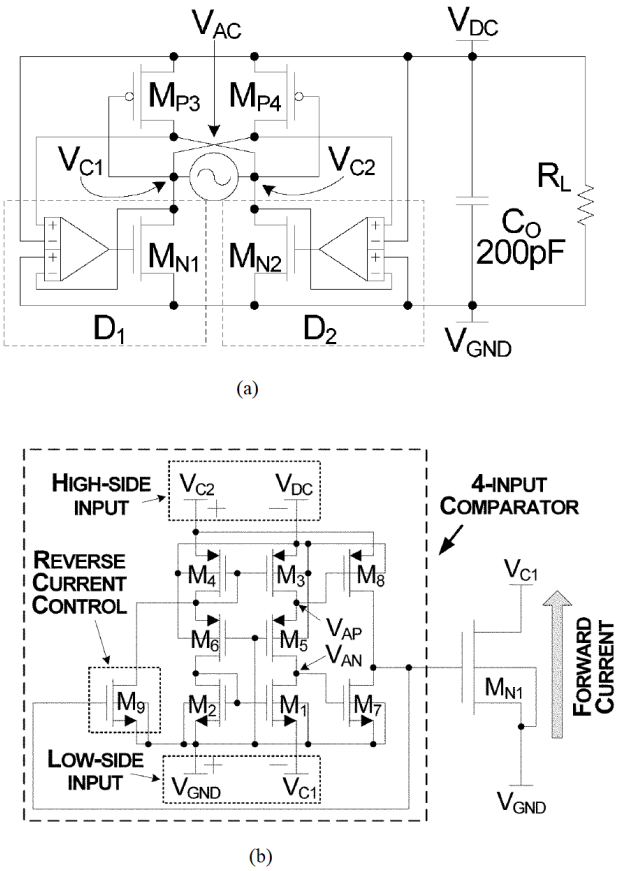


Figure 39: Full-wave active rectifier: (a) schematic diagram and (b) implemented active diode. (Lam et al., 2006)

This circuit enables to drive an NMOS power switch effectively, due to the low forward voltage of the active diodes, with a performance that matches a zero-threshold diode. However, the comparator has a current offset, inserting a delay on the system.

In contrast, a circuit using only one active diode is presented in Peters et al. (2010). The authors introduce an entirely new concept of a two-stage structure with a Negative Voltage Converter (NVC) combined with an active diode was used. It can be seen in Figure 40 that the active diode is controlled by a three-stage comparator: bias circuit, bulk-input stage, and output stage.

The first stage is a NVC used to convert the negative half-wave into a positive one. This stage is not sufficient to charge up a storage capacitor since the current direction is not controlled. As a consequence, a second stage is needed, the active diode, which consists of a PMOS switch driven by a comparator. Beyond this, a BR circuit is implemented to avoid leakage current. Furthermore, a PMOS diode is implemented in parallel to the active diode to ensure a safe start-up under all the possible conditions.

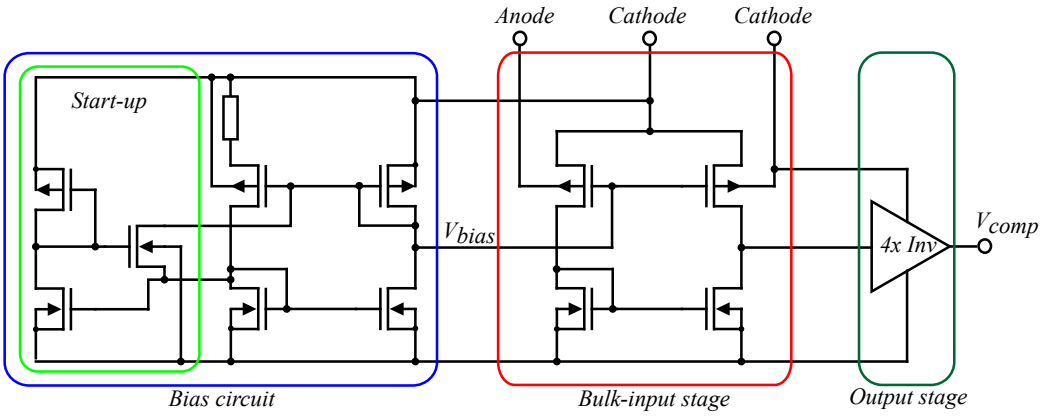


Figure 40: Design of the comparator and respective sub-circuits. (Peters et al., 2010)

The dependence of the drain current from the bulk voltage is an undesired effect. Therefore, in this comparator, the bulk works as an input terminal while at the gate, the bias is provided. This biasing voltage is created using a conventional beta-multiplier bias circuit with start-up, making it almost independent from the voltage supply. The bulk-input stage compares the anode and cathode potential through the bulk inputs of two PMOS transistors. The output stage is a cascade of four inverter stages, used to generate and generates a digital signal.

This circuit has some inconveniences, particularly a low input working voltages, and high complexity, as the use of four inverters in the last stage. Moreover, incorporate a resistor in the comparator design increases power consumption and chip area.

The same architecture is used in Li et al. (2014), with a three-stage comparator to control the active diode, namely: bias stage, source input stage, and output stage. In this case, the schematic was simplified since the last stage only uses two inverters. However, it was added a resistor in the bias stage, increasing the power consumption of the comparator and occupies a large chip area.

The rectifier in Cha et al. (2012) implemented a four-input cross-coupled latched comparator and a speed-up technique. This circuit was made particularly for biomedical applications, with a specific input frequency in the order of MHz. The MOSFETs operate as a switch driven by self-dynamically powered comparators without a constant voltage supply. Nonetheless, both resistors and capacitors increase power consumption and chip area. Besides this, the rectifier is symmetric, making use of two active diodes.

A fully CMOS rectifier composed of a three-stage comparator is reported in Peters et al. (2008). The circuit includes a self-biasing, a common-source output amplifier, based on an unsymmetrical two-stage amplifier, and an inverter, to ensure a digital output. Nevertheless, it has a high minimum input voltage. The bias current is dependent on the supply voltage, due to the self-biased.

Summary

Table 4 summarizes some of the aforementioned state-of-the-art structures of a rectifier given in this section with their advantages and disadvantages.

Table 4: Comparison of the state-of-the-art of CMOS rectifier topologies.

Topology	Features	Comments
DTMOS (Bokor et al., 1997; Cardoso, 2010; Babacan, 2018)	The MOSFETs has the gate tied to the bulk terminal.	⊙ Reduce V_{th}; Low power dissipation and consumption; Wide voltage operation; No reverse current; Replace the conventional MOS diodes. ⊗ Expensive if it uses NMOS.
Passive rectifier (Peters et al., 2011; Junior et al., 2018; Kotani and Ito, 2009)	Composed by conventional rectifiers and configurations with MOSFETs connected as a diode.	⊙ Simple structures; Configuration techniques to reduce V_{th} and increase PCE; High input frequency applications. ⊗ Weak performance; Large chip area.
Active rectifier (Lam et al., 2006)	Full CMOS active rectifier employing a four input comparator with common gate input stages.	⊙ Performance matches a zero-threshold diode. ⊗ Offset current; High schematic complexity.
Two-stage active rectifier (Peters et al., 2010)	System composed by a NVC and an active diode controlled by a three stage comparator.	⊙ Low input voltage applications. ⊗ Limited voltage range; High schematic complexity.
Two-stage active rectifier (Li et al., 2014)	Two-stage structure that includes a three-stage comparator with a resistor.	⊙ Simple schematic. ⊗ High power consumption; Large chip area.
Active rectifier (Cha et al., 2012)	Active NMOS and PMOS diodes composed by a four-input common-gate-type cross-coupled comparator.	⊙ Speed-up technique. ⊗ High power consumption; Large chip area.
Two-stage active rectifier (Peters et al., 2008)	Fully CMOS two stage active rectifier controlled by a three stage comparator.	⊙ Fully CMOS architecture. ⊗ High minimum input voltage.

⊙ Advantage, ⊗ Disadvantage.

3

DEVELOPMENT AND RESULTS

Electronic devices consume energy in order to generate the desired output and in unwanted behavior such as waste heat. When energy is harvested from small environment sources, the energy consumption must be kept to a minimum, to maximize the device efficiency.

Using CMOS technology, custom transistors are used for constructing an IC. This fabrication processes are able to form symmetric p- and n-type transistor pairs. The possibility of this symmetry is beneficial to design accurately mixed-signal systems. Another essential feature is the CMOS low static power consumption compared to other IC technologies. Additionally, CMOS technology can reduce the energy consumption to an absolute minimum during the OFF state of the system. For these reasons and the ability to integrate complex systems on the same chip, CMOS was chosen as the main technology used for the development of the proposed system.

Although CMOS devices fabrication is cumbersome and expensive, the use of Electronic Design Automation (EDA) tools is needed. Thereby, the design can be tested through simulation, allowing an increased reliability and a faster prototyping on new iterations.

3.1 Analog Switch

Per the research described in section 2.1, an original design is developed. Several improvements are made to increase the switching speed and efficiency, keeping a wide frequency range.

3.1.1 Up-conversion Technique

The main limitation in standard energy transfer approaches is the high inductance value needed to properly match the impedance of the piezoelectric element, due to the low operating frequency of conventional piezoelectric transducers. An automatic frequency up-conversion technique based in Li et al. (2014), as represent in Figure 41, overcomes this drawback, shifting the working operational frequency to higher values. This harvesting architecture is designed to match the output impedance of the piezoelectric transducer dynamically, by shifting the vibrational frequency of the piezoelectric element up to the resonant frequency of the harvesting interface.

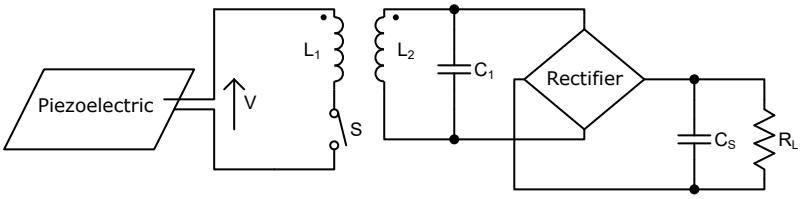


Figure 41: Schematic of the frequency up-conversion rectifier.

The circuit illustrated in Figure 41 is composed of a transformer, a bilateral switch S, and a tuning capacitor C_1. L_1 and L_2 are the inductances of the primary and secondary coils in the transformer, respectively. Therefore, the switched transformer is employed as an active component to implement the up-conversion technique.

The current in the first loop can be expressed by Equation 25, where I_{1m} is the maximum current and ω_0 is the angular frequency of the piezoelectric.

$$i_1(t) = I_{1m} \cdot sin(\omega_0 \cdot t) \tag{25}$$

Equation 26 describes the equivalent input resistance of the frequency modulation circuit. On the assumption that T and D_1 are the period and duty cycle of the switch, respectively.

$$R_1 = \frac{2 \cdot L_1}{D_1^2 \cdot T} \tag{26}$$

The secondary resonance circuit also creates a resistance in the transformer (R_2). To simplify the analyzis, the rectifier is considered as a diode bridge. When the voltage across the inductor L_2 reaches the threshold voltage of the diode, energy can be transferred for the storage capacitor (C_s;.otherwise, the capacitor C_1 is charged. Thus, assuming that $i_2(t)$ as the current in the secondary resonant circuit, the voltage across the secondary circuit can be expressed bu Equation 27.

$$V_{L2}(t) + V_{C1}(t) + V_{R2}(t) + V_D = 0, \tag{27}$$

where V_{L2}, V_{C1}, V_{R2} and V_D are the voltage across the inductor L_2, the capacitor C_1, the resistance R_2, and the threshold voltage of the diode bridge rectifier, respectively.

Moreover, for the resonant matching circuit, the efficiency is proportional to the quality value. Hence, equations 28 and 29 express the quality factor of the primary and secondary transformer loops, correspondingly.

$$Q_1 = \frac{1}{R_1} \cdot \sqrt{\frac{L_1}{C_p}} \tag{28}$$

$$Q_2 = \frac{1}{R_2} \cdot \sqrt{\frac{L_2}{C_1}} \tag{29}$$

3.1.2 Management System

The switching circuit for vibrational energy harvesting applications implemented in this work is exhibited in Figure 42. The management system is composed of a piezoelectric transducer, a switching circuit, a transformer, a rectifier, and lastly a storage stage.

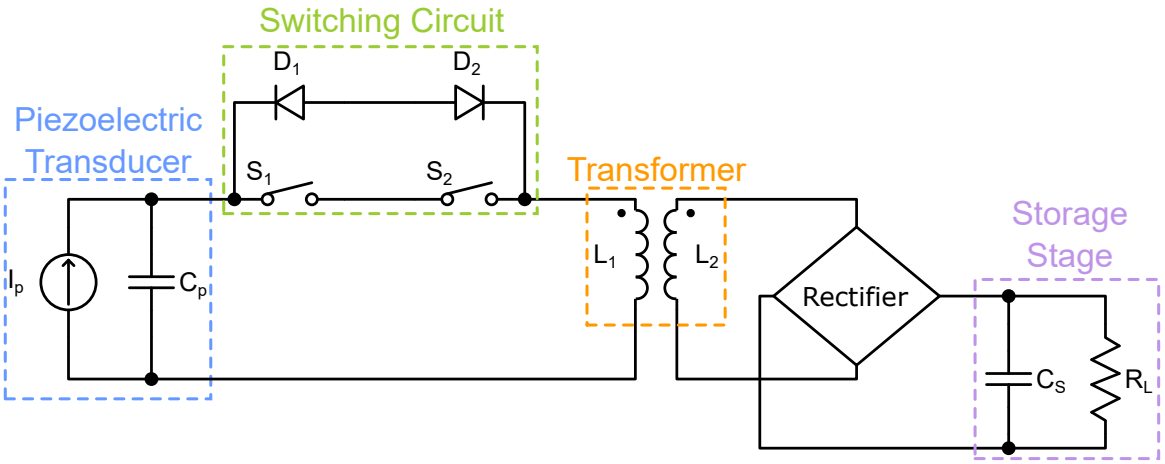


Figure 42: Circuit diagram of the switching approach for vibrational energy harvesting.

The resistance of the piezoelectric can be ignored in the analysis since its value is approximately $10^7\ \Omega$, and the equivalent capacitor (C_p) is relatively small. The equivalent model of a capacitor is implemented by an AC

current source in parallel with the equivalent capacitor. The equivalent capacitor can be formulated according to Equation 30.

$$C_p = \varepsilon_0 \cdot \varepsilon_r \cdot \frac{S}{d}, \tag{30}$$

Where ε_0 is the vacuum dielectric constant, ε_r is the relative permittivity, and the term $\frac{S}{d}$ is the ratio between the area (S) and the thickness (d) of the piezoelectric.

Transformer

Two coil winding, L_1 and L_2, around a solid core, create the transformer, which the working principle relies on the Faraday's law of induction based on the change of magnetic field. Both coils are connecting two electrical circuits through electromagnetic induction. By mutual induction, one coil magnetically induces a voltage into another coil, located at the proximity. In this way, there is no direct electrical connection between the coils.

Thanks to the transformer it is possible to either increase or decrease, or even produce the same voltage applied to the primary winding, without changing its frequency, or the amount of electrical power being transferred from one to another winding. This is accomplished by changing the number of turns in the primary coil (N_1) compared to the number of turns in the secondary coil (N_2). The ratio of transformation (n) dictates the operation of the transformer and the corresponding voltage available on the secondary winding (V_2), and is given by Equation 31.

$$n = \frac{N_1}{N_2} = \frac{V_1}{V_2} \tag{31}$$

Switching circuit

Analog switches are a common building block in analog signal processing, that when turned ON are capable of conducting both analog and digital signals from the input to the output, regardless of the signal travelling direction. The structure of a conventional analog switch connects an NMOS in parallel with a PMOS. MOSFETs make almost excellent switching devices and are often used in power applications. Those are faster, smaller, easy-to-use, and consume less power than other electrically controlled switches. While turned ON, it allows the signal to pass in either direction, during the time is turned OFF isolates the piezoelectric transducer. Nevertheless, there are some obstacles on analog switches. These circuits have a frequency response limitation due to channel capacitance,

that can be caused, for example, by parasitic capacitance at high frequencies. The ideal switch should transmit a signal without changing the original, creating a short-circuit at OFF state and an open-circuit at ON state. However, there are some losses associated with the resistance of the conducting channel when the MOSFET is turning ON. Moreover, the analog switch generates ground bounce noise and demonstrates a propagation delay.

The switching circuit works as a frequency converter or frequency changer, which converts an AC signal of a specific frequency to an AC signal with another frequency. This is achieved, as depicted in Figure 42, by two switches, S_1 and S_2, and two diodes, D_1 and D_2, connected in parallel to the switches. Both switches operate at a switching frequency, referring to the rate at which the switch connect and disconnect the conducting path from the piezoelectric transducer. Besides, since the switch as no preferred direction for current flow, the diodes work as a barrier to avoid the reverse current. As a result, the switching circuit turns ON and OFF at the desired frequency, the signal is modeled into that frequency.

The switching frequency is a circuit parameter to take into consideration since it affects nearly every performance characteristic of the system. A high switching frequency reduces the size of associated components, such as the inductors, transformers, and capacitors, decreasing space requirements on a board or chip. However, converters operating at higher frequencies have reduced efficiency due to the increased power losses. Thus, it is necessary to equilibrate these factors.

Figure 43 illustrates the CMOS analog switch implemented in this work. The transistors M1 and M2 constitute the conventional switch, an NMOS connected in parallel with a PMOS, correspondingly. The switch mechanism is controlled by an inverter or NOT gate, constituted by both p-channel and n-channel MOSFETs, M3 and M4 respectively. The working principle is simple: at the time the voltage that enables the transistors (V_{EN}) is high, the gate of M1 is activated, and the current can flow through it. The signal is inverted by the NOT gate, activating the gate of M2. Thereby, the analog switch is turned ON, or the circuit is closed. Otherwise, when V_{EN} is a low voltage, the gate of M1 is not activated and the transistor works as an open circuit. In this case, the signal is inverted by M3 and M4 and is not able to activate the transistor M2. Since both the switch transistors M1 and M2 are in open circuit, the current is not flowing to the output, and the system is isolating the input signal. Thence, if both transistors, M1 and M2, are turned OFF, the switch is opened.

To enhance the performance of the switching circuit on Figure 44(a), a current starved technique is added, as shown in Figure 44(b), to reduce the current and power consumption. The transistors M3 and M4 constitute the standard CMOS inverter. M5 and M9 limit the current available to the inverter. The drain currents of M6 and M8 are the same and are fixed by M7.

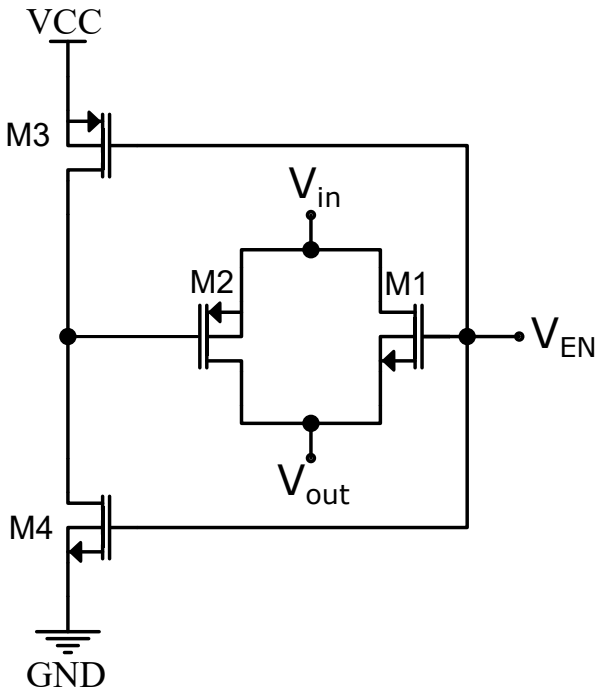


Figure 43: Analog switch schematic for the switching circuit.

The switch is closed when V_{EN} is a high value. In this way, the n-channel MOSFET M1 is activated. Subsequently, V_{EN} is inverted by the upturned into V_{nEN}, which is capable of turning ON the p-channel MOSFET M2. Afterwards, the analog switch is closed and the input signal is flowing to the output. On the contrary, if V_{EN} is a low signal, M1 is turned OFF along with M2 and the analog switch is open.

3.1.3 Features

During the designing process is crucial to define the circuit´ specifications. There are many performance criteria to consider, due to a large number of analog switches in the market. A structure of a conventional analog switch is an NMOS connected in parallel with a PMOS. Therefore, some important parameters are described as following:

- Absolute maximum supply voltage: this is the maximum voltage that may be applied to power the analog switch.
- Absolute maximum input voltage: the maximum and minimum input voltage that may be applied at either the source or drain terminal and pass through the analog switch.

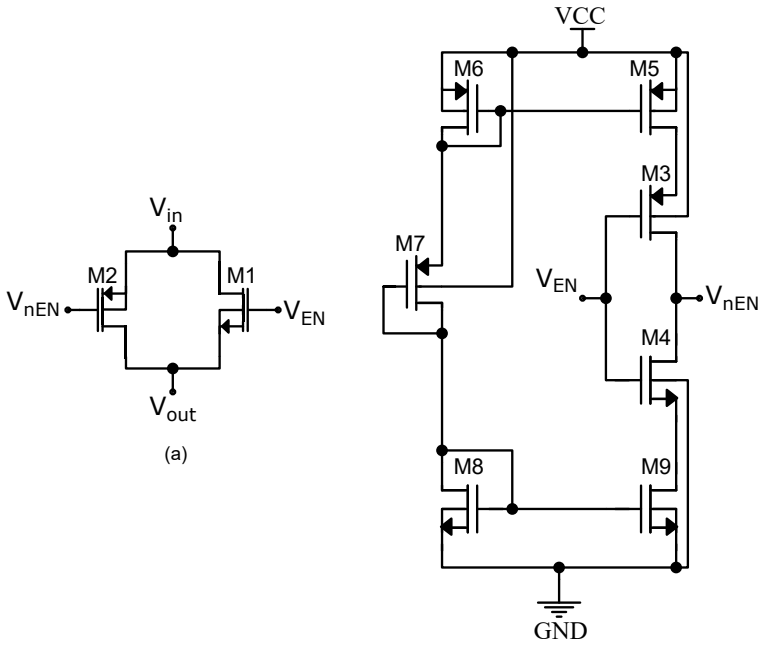


Figure 44: Enchanced analog switch coupling the (a) conventional switch with a (b) current starved technique.

- OFF isolation: the amount of coupling from input to output of a disabled channel. A measurement of OFF state switch impedance.
- ON loss or insertion loss: represents the attenuation of the output signal from the respective input signal and strongly depends on the load stage.
- Control system: the voltage levels of the switch need to be compatible with the switch control.
- Charge injection: changing the state on the control pin causes a charge to be coupled to the channel of the transistor, introducing signal noise.
- Switching speed: specifies how long it takes for the switch to actuate. This is the delay from when the logic state of the switch control change, and subsequently enables its output in response to the given input. Turn ON time (t_{ON}) is the maximum amount of time needed to be in the ON or in conducting state after its digital input turns it on. Nevertheless, turn OFF time (t_{OFF}) is the maximum amount of time needed to be in the OFF or the non-conducting state after its digital input turns it off.
  - Break-Before-Make (BBM): If $t_{ON} > t_{OFF}$, the first set of contacts break (open) before engaging (close) the new contacts. This process is called BBM and prevents a momentary electrically connection between the old and new signal pads when the select input changes.

  - Make-Before-Break (MBB): If $t_{ON} < t_{OFF}$, the signal paths are not open when the select input changes state. In other words, MBB describes a configuration to avoid opening both switches at the same time. In this way, the new connection path is settled before the previous contacts are opened.

- ON resistance (R_{ON}): the resistance value between the drain and source of a MOSFET during operation. Ideally, this parameter should be as low as possible to keep the signal losses and propagation delays small. However, the trade-off on reducing R_{ON} is that it involves increasing the width (W) and length (L) ratio, resulting in higher parasitic capacitance and a larger silicon area. Apart from W and L, R_{ON} is a function of electron and hole mobility (μ_n and μ_p, respectively), oxide capacitance (C_{OX}), V_{th}, and signal voltage (V_{GS}) of the n- and p-channel MOSFETs as formulated in equation 32.

$$R_{ON} = \frac{L}{\mu \cdot C_{OX} \cdot W \cdot (V_{GS} - V_{th})} \tag{32}$$

- OFF resistance (R_{OFF}): this describes the resistance of the switch in OFF state or open circuit. In this case, the higher the R_{OFF}, the smaller the energy losses during switch OFF state. Nonetheless, a high R_{OFF} is also very important for a good OFF-isolation (OFF state impedance).

- Feedthrough: this characteristic is related to the ability of the switch to block signals in OFF state. Parasitic capacitance allows high frequencies to mix through the switch, making it appear to be ON or closed circuit. This parameter is directly connected with OFF isolation and OFF resistance.

An important characteristic is the transistor dimensions. For low voltage design, a large width is needed to keep the voltage drop over the device low. The transistors size is chosen to keep R_{ON} low. The selected transistors size for the designed circuit in Figure 44 is pointed in Table 5.

Table 5: Dimensions of the switching circuit transistors.

Transistor	**Width (μm)**	**Length (μm)**
M1, M2	12	5
M3, M4, M5, M6, M8, M9	0.28	0.13
M7	0.15	0.13

For the proposed applications, some specifications are established to enhance the performance of the circuit. The supply system should have a voltage of $3.3\ V$ and a current higher than $0.05\ \mu A$. The OFF resistance should

be as high as possible and the ON resistance approximately $50\,\Omega$. Additionally, the leakage current should be null, although, in a real-world application, those conditions are not possible to achieve. Thus, a leakage current with a maximum of $1\,nA$, and a switching speed of $100\,ns$ are desired.

3.1.4 Results

In order to test the proposed circuit, SPICE simulations tools were used in Cadence software with the appropriate $0.13\,\mu m$ CMOS technology.

The results of the analog switch operation are presented in Figure 45, show how the analog switch operates. A sinusoidal input voltage (V_{in}) with $1\,V$ and an offset voltage of $1\,V$ at $10\,kHz$ was adopted. The offset voltage is applied to guarantee that the input voltage has not negative values. Due to this, the input voltage goes from $0\,V$ to $2\,V$. Besides, a supply voltage (V_{supp}) was set at $3.3\,V$, and a resistor load (R_L) was added at the end of the circuit to simulate an unstable state. Furthermore, the enable signal (V_{EN}) was simulated as a Piecewise Linear (PWL) voltage source, which within $0\,s$ until $200\,\mu s$ is zero, then from $200.1\,\mu s$ until $600\,\mu s$ is $3\,V$. Finally, up to $600.1\,\mu s$, V_{EN} is grounded again.

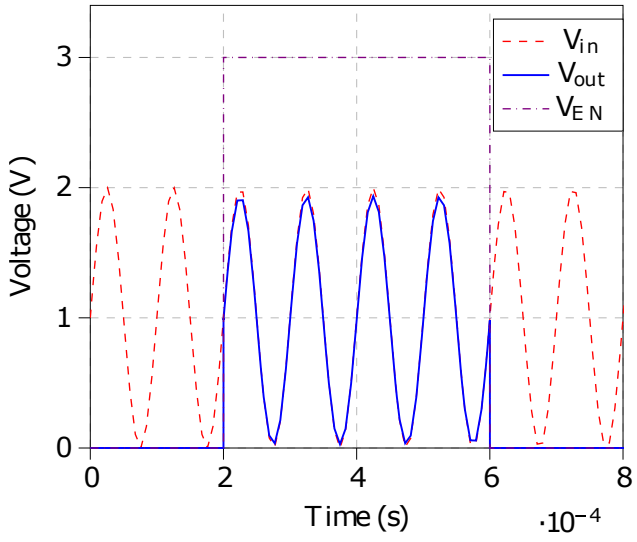


Figure 45: Operation principle representation of the designed analog switch, including the input signal (V_{in}), enable signal (V_{EN}) and the output waveform (V_{out}).

As observed in Figure 45, the operation of the switching circuit is fulfilled. When V_{EN} reaches high values, the analog switch is closed, allowing current to flow and outputs a signal similar to V_{in}. Moreover, the switch is open, isolating the input from the output when V_{EN} is low and the switch output is zero.

In addition to the first simulation, more specific testing was conducted. In order to measure the switching speed, the following input parameters were chosen: a DC source of $1\,V$ as the input voltage and V_{EN} is a PWL, which within $0\,s$ to $10\,\mu s$ is $0\,V$, then from $10.1\,\mu s$ to $12\,\mu s$ is $3\,V$. Finally, up to $12.1\,\mu s$ is grounded again. Figure 46 illustrates the results and allows to calculate the turn ON and OFF times.

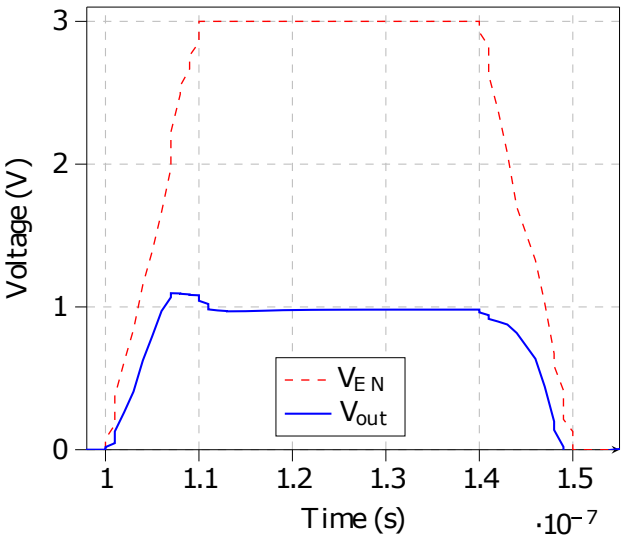


Figure 46: Switching speed estimation of the analog switch, with representation of the signal to enable (V_{EN}) and the output signal (V_{out}).

Once V_{EN} achieve high amplitudes at $110.0\,ns$, and V_{out} equals the input waveform when $t = 111.884ns$, the switch takes $1.88\,ns$ to conduct after the enable signal turned it ON. Contrarily, when V_{EN} is null at $150.0\,ns$, V_{out} reaches $0\,V$ at $161.266\,ns$. The time needed for the switch to stop conducting after the enable signal turns it OFF is $11.266\,ns$. Therefore, the turn ON and OFF times are $1.88\,ns$ and $11.27\,ns$, respectively.

The study on how the output voltage is affected by the input signal and the voltage supply, simultaneously, was made through parametric analysis. Thereby, V_{in} is a DC source with variable amplitude and different voltages supply to the circuit. The results of this experimentation are exhibited in Figure 47.

In the ON state, Figure 47(a), the switch losses are increasing during the time $V_{out,OFF}$ is rising. The circuit output signal is increasing until $V_{in} = V_{supp}$, then $V_{out,ON}$ is the same, independently from the input. Figure 47(b) shows that the output voltage during the time the switch is not conducting for different V_{supp}. The circuit outputs almost null as far as $V_{in} = V_{supp}$, at the time the switch is not capable of isolating the system and current starts to flow to the output. Thus, the analog switch works efficiently unless $V_{in} > V_{supp}$. Furthermore, the current supply is monitored for $V_{supp} = 3.3\,V$, and its value is maintained stable, approximately for $43\,\mu A$.

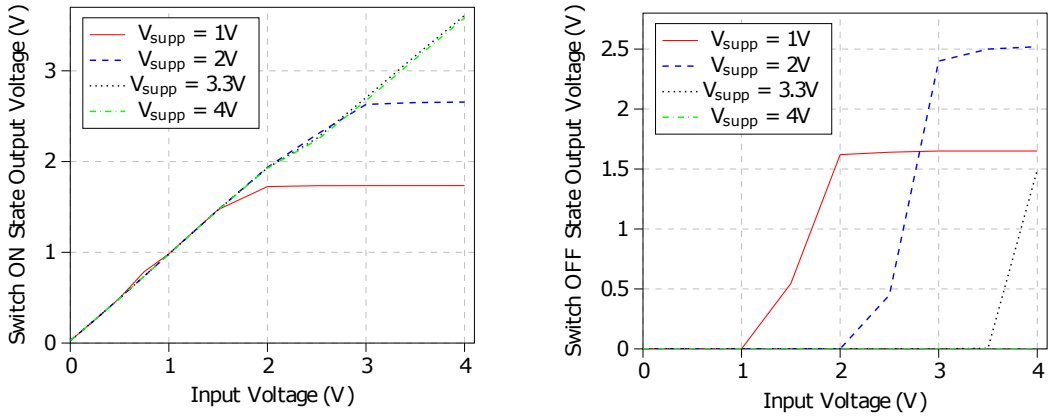


Figure 47: Output signal of the analog switch in (a) ON ($V_{out,ON}$) and (b) OFF ($V_{out,OFF}$) states, according to the input (V_{in}) and supply (V_{supp}) voltages.

The voltage gain is the quotient between V_{out} and V_{in}, as expressed in Equation 33. For low input values, the gain of the switch is higher, around 30, than for high input values. Particularly, in the case, $V_{supp} = 3.3\,V$ and V_{in} is up to $1\,V$, the gain is 0.98.

$$A_v = \frac{V_{out}}{V_{in}} \tag{33}$$

The $V_{out,ON}$ versus frequency is plotted in Figure 48, demonstrating a properly performance of the switch from $1\,Hz$ to $1\,MHz$. For this simulation, an AC input source is used with an amplitude of $0\,V$ to $3\,V$. At a certain point, the sinusoidal wave achieved a frequency not tolerated by the circuit, due to its switching speed and the information is lost. For this reason, achieving an efficient system it is important to keep the frequency within this wide range.

The $V_{out,ON}$ is also simulated according to the current supply (I_{supp}) for different V_{supp}, and the results are depicted in Figure 49. Due to the results of the previous simulation, the input is a signal with amplitudes between $0\,V$ and $2\,V$ at $10\,kHz$. Since for $V_{in} > V_{supp}$ the circuit allows a reasonable amount of voltage to flow on the OFF state, the simulations starts with $V_{supp} = 1\,V$.

The current supply is in the nano range for values under $1.25\,V$ of V_{supp}. Then, with an increase of V_{supp}, the I_{supp} is higher, reaching $176\,\mu A$. Due to this, the circuit under un-conducting operation lets the current to flow in the range of $10^{-3}\,A$. Moreover, the $V_{out,ON}$ slightly decreases with an increase of V_{supp}.

According to the last performed studies, the voltage supply was fixed at $1.5\,V$ with the same input parameters as before. The simulated output voltage when the circuit is opened and closed, $V_{out,ON}$ and $V_{out,OFF}$ respectively, versus load resistor (R_L) values, is exhibited in Figure 50.

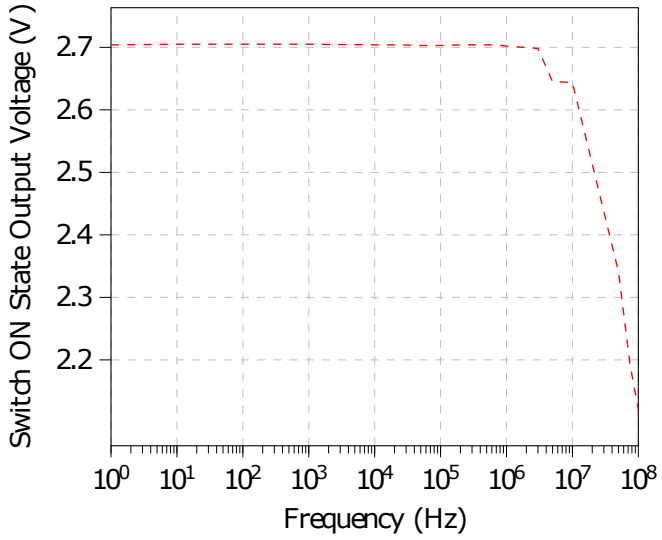


Figure 48: Operational frequency range of the analog switch, representing the output voltage during the switch conducting state ($V_{out,ON}$).

For high values of R_L, both $V_{out,ON}$ and $V_{out,OFF}$ increase and similarly, when R_L is low, both output voltages decrease. It is crucial to accomplish an equilibrium between the three parameters. The resistor must be between $10k\,\Omega$ and $50k\,\Omega$, avoiding unwanted current flow during the OFF state, and still achieving high values of $V_{out,ON}$.

ON and OFF resistances were calculated based on Ohm's law represented in Equation 34, where R, V and I are resistance, voltage and current, respectively. For this simulation, a sinusoidal input signal from $0\,V$ to $2\,V$ at $10\,kHz$ was used. The voltage supply was set at $3\,V$, to ensure $V_{in} < V_{supp}$. The resistance was calculated between the drain and the source terminals of M1 and M2.

$$V = I \cdot R \Leftrightarrow R = \frac{V}{I} \tag{34}$$

To measure R_{ON} and R_{OFF} it is necessary to calculate the voltage between the drain and the source terminals. These terminals are connected to V_{in} and V_{out}, respectively, for both transistors M1 and M2. Thus, regardless the operational state, V_{DS} is given by Equation 35.

$$V_{DS} = V_D - V_S \equiv V_{in} - V_{out} \tag{35}$$

Applying the simulations results on the previous equation, V_{DS} is $70\,mV$ during the conducting state and approximately $2\,V$ under non-conduction conditions.

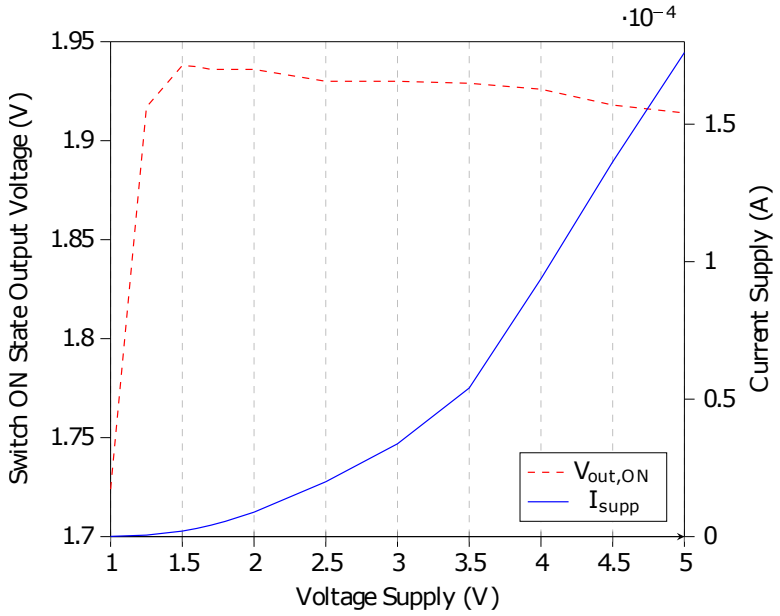


Figure 49: Output voltage when the switch is closed ($V_{out,ON}$) and supply current (I_{supp}) under different voltages supply.

Furthermore, I_{DS} is measured for M1 and M2 during the switch operation in the ON state. Equation 36 calculates the current on transistor M1 and Equation 37 on transistor M2.

$$I_{DS,1} = I_{D,1} - I_{S,1} \tag{36}$$

$$I_{DS,2} = I_{D,2} - I_{S,2} \tag{37}$$

For the transistor M1, $I_{D,1} = 21.179 \cdot 10^{-6}\,A$ and $I_{S,1} = -570.8 \cdot 10^{-9}\,A$. Thus, implementing these values in Equation 36, the $I_{DS,1}$ is $21.75\,\mu A$. Similarly, for the transistor M2, $I_{D,2} = 11.172 \cdot 10^{-6}\,A$ and $I_{S,2} = -36.44 \cdot 10^{-9}\,A$, leading to $I_{DS,2} = 11.21\,\mu A$. After employing these values to Equation 34, the resistance of M1 and M2 is obtained, $322\,\Omega$ and $625\,\Omega$, correspondingly. Finally, since M1 and M2 are in parallel the equivalent resistance is calculated based on Equation 38, which result in a R_{ON} of $212.5\,\Omega$.

$$R_{eq} = \frac{R_1 \cdot R_2}{R_1 + R_2} \tag{38}$$

Analogous, the same process was followed to calculate R_{OFF}. In a OFF state, $I_{DS,1} = 739.6\,pA$, $I_{DS,2} = 3.01\,nA$, and the resistance of M1 and M2 are $2.7G\,\Omega$ and $645M\,\Omega$, respectively. Then, applying Equation 38, R_{OFF} is $520.6\,M\Omega$.

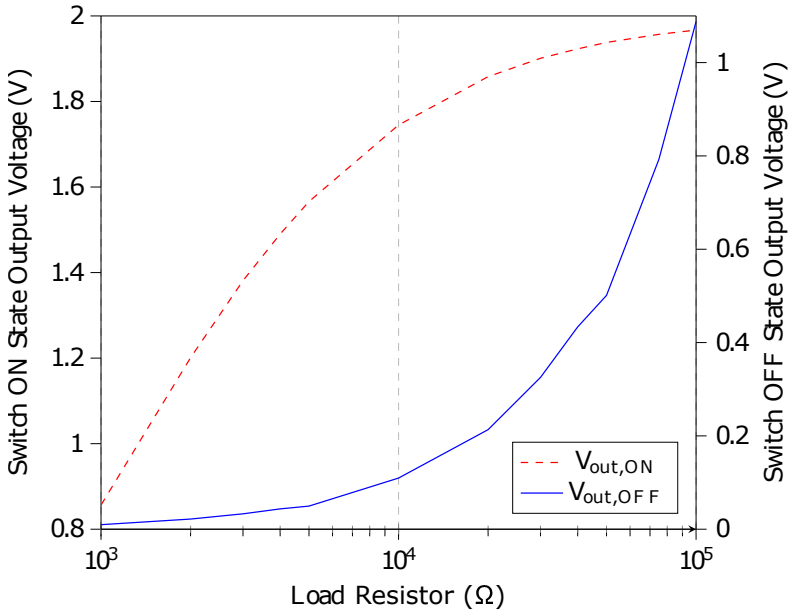


Figure 50: Output voltage when the switch is in conducting ($V_{out,ON}$) and in non-conducting ($V_{out,OFF}$) states, through different ohmic load values.

These values were calculated according to the imput parameters estimated in the previous simulation. Herefore, if those are changed, R_{ON} and R_{OFF} also change. Both values vary according to the input and supply signals.

Furthermore, the ON loss and OFF isolation are calculated. For this measurements a supply voltage of $2\,V$ and a continuous input voltage of $1\,V$ were chosen. The calculated V_{out} is $0.98\,V$ with the switch closed, and it is $2.74\,\mu V$ in open-circuit. The insertion loss is expressed in Equation 39, and OFF isolation in Equation 40, which are $-0.16\,dB$ and $-111.2\,dB$, respectively. Both are negative since V_{out} is lower than V_{in}, and a unitary gain is not achieved.

$$ONLoss = 20 \cdot log\left(\frac{V_{out}}{V_{in}}\right) \tag{39}$$

$$OFFIsolation = 20 \cdot log\left(\frac{V_{out}}{V_{in}}\right) \tag{40}$$

The temperature stability was also analyzed, and the circuit behaves similarly from $-40\,°C$ to $150\,°C$, with small attentions. Using an input of $2\,V$, at $-40\,°C$, the maximum $V_{out,ON}$ is $1.945\,V$ and the maximum $V_{out,OFF}$ is $25.58\,\mu V$. Howbeit, at $150\,°C$, $V_{out,ON}$ and $V_{out,OFF}$ are $1.9\,V$ and $651.56\,\mu V$, respectively. The difference in the outputs is reduced and irrelevant when compared to a temperature of $190\,°C$, where the results diverge.

The turn-off time also suffers modifications according to the surrounding temperature. In a hooter environment (150 °C) the analog switch needs $27.05\,ns$ to completely open the circuit. On the other hand, under negative temperatures, t_{OFF} is faster. In this case, at $-40\,^{\circ}C$, the switch only needs $12.82\,ns$. Analysing both the times, the difference is minimal and insignificant for the system.

3.1.5 Discussion

According to the main goal, the design of an analog switch fast and efficient, and capable of achieving a high OFF resistance and low ON resistance, was achieved. As shown in the results section, the circuit is fast and has appropriate behaviour under conducting and non conducting conditions. Special attention needs to be taken into account in order to guarantee that the input signal never increase above the voltage supply. If this happens, the switch can not efficiently isolate the circuit under non-conducting conditions. One essential objective for the design is the temperature independence of the circuit, which was also achieved.

The market offers a variety of analog switches, and each semiconductor manufacturing company also supplies the costumers with selection guides and data sheets that can help narrow down to the best off-the-shelf option. Some possible and adequate options are TS12A4514 from Texas Instruments (Tex, 2009) or ADG841 from Analog Devices (Ana, 2005).

An overview comparison with standard switches commercially available is represented in in Table 6. The data were acquired by the review of datasheets provided by the companies. The features of TS12A4514 and ADG841 are with a voltage supply of $3.3\,V$ and $2.7\,V$ to $3.6\,V$, respectively.

The proposed circuit shows an overall performance better than the commercial components. Althought the supply voltage is not as small as required for the others, it has a broader range. Moreover, the operating temperature range is more extensive than the others and presents a faster switching speed. Despite the turn-off time of ADG841 is lower, the turn-on time of the proposed work is lower than its.

Ideally, the analog switch has no resistance in the ON state and infinite off impedance. However, real CMOS analog switches meet none of those criteria. The R_{ON} of this work is higher than previous works, but small enough for the propose of the system. Likewise, the OFF isolation is directly connected with the resistance of the switch and to its ability to block the signals in the OFF state. Acceptable OFF isolation means an absolute value as high as possible. Therefore, since the OFF isolation of this work is above the featured by other components, it implies its R_{OFF} is also higher.

Table 6: Comparison of proposed analog switch with off-the-shelf components.

References	TS12A4514 (Tex, 2009)	ADG841 (Ana, 2005)	Proposed Work
Voltage Supply (V)	-0.3 - 13	-0.3 - 4.6	-0.25 - 19
Input Voltage (V)	$V_{supp} \pm 0.3$	$V_{supp} \pm 0.3$	$\leq V_{supp}$
Temperature (°C)	-40 - 85	-40 - 125	-40 - 150
Turn ON time (s)	100n	14n	1.88n
Turn OFF time (s)	50n	7.8n	11.2n
ON resistance (Ω)	50	0.28	212.5
OFF resistance (Ω)	-	-	520.6M
ON loss (dB)	-	-0.02	-0.16
OFF isolation (dB)	-94	-54	-111.24

3.1.6 Summary

A fast and efficient analog switch, with an inverter, making use of a starved current technique, was designed. The circuit is supplied by a wide voltage range. Compared to previous research, this circuit performs in the normal range, for its purpose, especially with the chosen technology.

During simulations, a sensitivity analysis was performed. The proposed design is suitable for matching the high impedance of the piezoelectric element, shifting the vibrational frequency of the piezoelectric up to the resonant frequency of the harvesting interface. Besides, the circuit is capable of supporting high frequencies up to MHz. This is also suitable for low voltage operation. Additionally, the integration of the switch cell to CMOS circuit designs should be straightforward, even with already existing designs.

The circuit used CMOS technology, taking into advantage the sub-threshold region of CMOS transistors. The final layout design and fabrication steps are presented in section 3.4. The design has in mind energy harvesting interfaces and wireless sensor networks, although it has, likewise, applications for modems, audio, communication systems, and so forth.

3.2 Voltage Amplifier

The energy generated by PEGs has limited power from tens of microwatts to a few milliwatts, being unsuitable to directly powering most electronic systems. In order to overcome this issue, a voltage amplifier was implemented to pre-amplify the signal is needed. Therefore, the application of MOSFETs with low power consumption is essential.

3.2.1 Design and Modeling

Amplifiers must be designed according to specific design and application objectives. According to the consideration described in section 2.2, an original design is developed. For this project, the voltage amplifier is exhibited in Figure 51, and consists of a non-inverting two-stage amplifier.

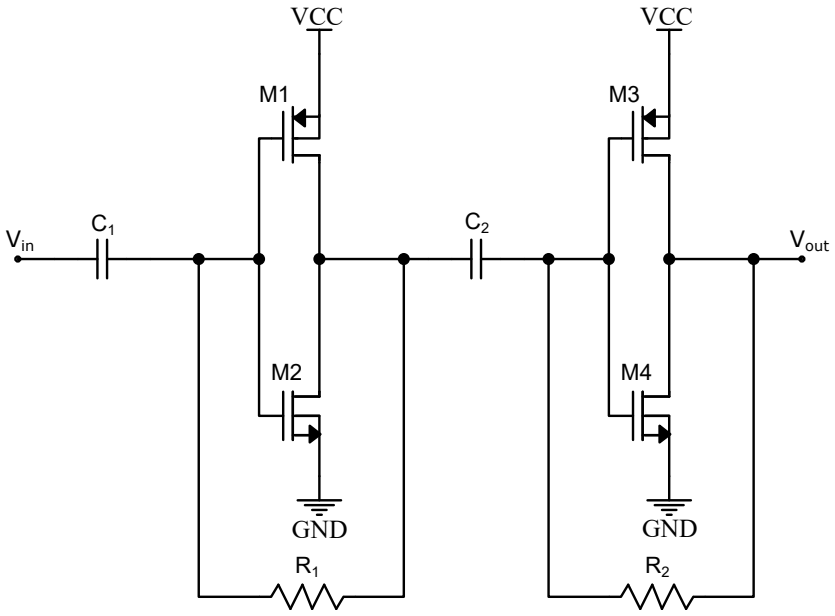


Figure 51: Circuit schematic of the designed voltage amplifier.

The resistors, R_1 and R_2 provide DC feedback, and ensure the stability of the circuit. The capacitance C_2 is responsible for attenuating the offset voltage. To amplify the signal, the input has to be coupled via a capacitor, C_1, and the transistor M1 should present a high width. The specifications of the components are depicted in Table 7.

The voltage amplifier is implemented by two inverters or NOT gates in cascade. The first stage is constituted by C_1, R_1, M1 and M2, while C_2, R_2, M3 and M4 make up the second stage. Thus, the input signal is twice inverted, and the circuit output is a non-inverted signal.

Table 7: Specifications of the voltage amplifier circuit components.

Component	Specifications
R_1, R_2	$1\,M\Omega$
C_1, C_2	$1\,nF$
M1	10/0.35 (μm)
M2, M3, M4	0.15/0.13 (μm)

3.2.2 Features

Ideally, an amplifier would have infinite voltage gain, input resistance (R_{in}), Gain Bandwidth (GBW) range and slew rate. In opposition, it should have a null output resistance (R_{out}), offset current and offset voltage. However, every single amplifier is different, distinguished by their configuration, operation principle and output. Therefore, some critical parameters to classify the amplifiers are described as following:

- Offset voltage: a small offset caused by the inherent properties of the amplifier resulted from the mismatches in the input bias arrangement. This implies that even if the input signal is ground, there is a small voltage at the output. In order to solve this issue, an offset nulling method is commonly used. This consists of providing a reduced offset voltage in the input, making the output to have a zero voltage.
- Unit gain frequency: corresponds to the frequency for which the gain is $0\,dB$.
- Open loop gain: the gain obtained when no overall feedback is used in the circuit and it is calculated by the ratio between the output voltage and the input signal.
- Slew rate: in an ideal diode, regardless of the input signal frequency, no information is lost. In real-world, if the frequency of the input waveform is too high, the output can not handle, and the output signal is distorted.
- Power Supply Rejection Ratio (PSRR): this is defined as the gain from the input to the output divided by the gain from the supply to the output of the amplifier, in the presence of supply noise. This parameter indicates the ability of the circuit to suppress any variation of the power supply to its output signal.
- Quiescent current: is defined as the amount of current used when the circuit is operating at a null state, meaning it produces an output of zero.

- Supply voltage: the range of voltage supply for which all the presented characteristics are maintained.
- Temperature behaviour: the range of temperature for which all the presented features are maintained.
- Stability

Specifications were settled to accomplish an efficient voltage amplifier with excellent performance. To match the piezoelectric element is essential to accomplish a simple circuit of one stage, with low power consumption, less than $10\,mW$. A high gain of 1000 or more than $60\,dB$ to convert small amplitudes into usable signals is also required. Furthermore, a quiescent current of $1.6\,\mu A$, a minimum supply voltage of at least $1.6\,V$, and PSRR from $0\,Hz$ to $100\,kHz$ of $130\,dB$ to $25\,dB$, are requested.

3.2.3 Results

Circuit simulations can be used to have a more practical understanding of an amplifier behaviour. Electronic simulations development has improved, taking into account not only ideal mathematical models, but also external factors, such as temperature, noise, or even process variations resulted from the fabrication.

The amplifier basic operation is shown in Figure 52, extracted from Cadence software, using the $0.13\,\mu m$ CMOS technology. A sinusoidal input waveform (V_{in}) with $5\,mV$ of amplitude at a frequency of $10\,kHz$ and voltage supply (V_{supp}) of $1.6\,V$ is used. The maximum and minimum output voltage are $1.463\,V$ and $67.77\,mV$, respectively, which implies that the peak-to-peak voltage is $1.40\,V$. Thereby, the gain is 140 or $42.9\,dB$, as expressed in equations 41 and 42. Due to the offset voltage, the output voltage is higher than $0\,V$.

$$A_v = \frac{V_{out,pp}}{V_{in,pp}} \tag{41}$$

$$A_v(dB) = 20 \cdot log(A_v) \tag{42}$$

In Figure 53 is exhibited the output voltage variation according to the input and supply voltages. Since the circuit has an offset voltage, the output values correspond to ($V_{out,max}$ - $V_{out,min}$). The purpose of this circuit is to amplify the piezoelectric signal. Herefore, the input voltage is a sinusoidal signal with an amplitude from $0\,V$ to $1\,V$ at $10\,kHz$.

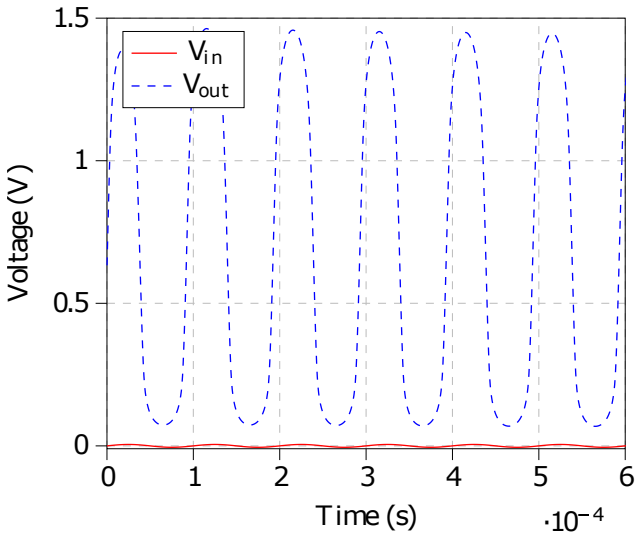


Figure 52: Input signal (V_{in}) and amplified output signal (V_{out}) of the projected amplifier.

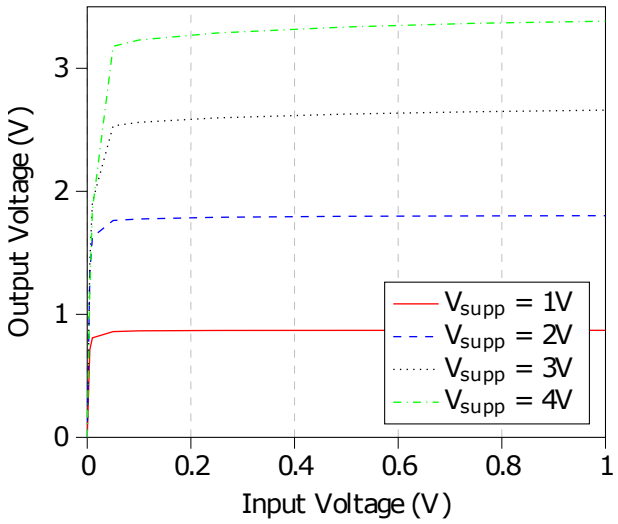


Figure 53: Output signal (V_{out}) of the voltage amplifier through different input (V_{in}) and supply (V_{supp}) voltages.

When V_{supp} increase also V_{out} is higher. Further, the gain is higher for low V_{in}, as exhibited in Figure 54, than for high input voltages. The resistance load is big enough to not affect the output - $R_L = 100\,k\Omega$.

The offset voltage (V_{offset}) is simulated by tying the input of the amplifier to the ground and measuring the output voltage. Once V_{offset} depends on the supply voltage, the lowest value measured for V_{offset} was $8.86\,\mu V$, with a V_{supp} of $2\,V$.

The quiescent current (I_Q) is measured with $O\,V$ in the input and $V_{supp} = 2\,V$ and $I_Q = 49.5\,\mu A$

The supply current (I_{supp}) is the sum of the current on both stages. An input voltage of $5\,mV$ at $10\,kHz$ and V_{supp} of $2\,V$ is applied. The current in the first and second stage are $124.5\,\mu A$ and $57.13\,\mu A$, respectively. Thus, I_{supp} is $181.63\,\mu A$.

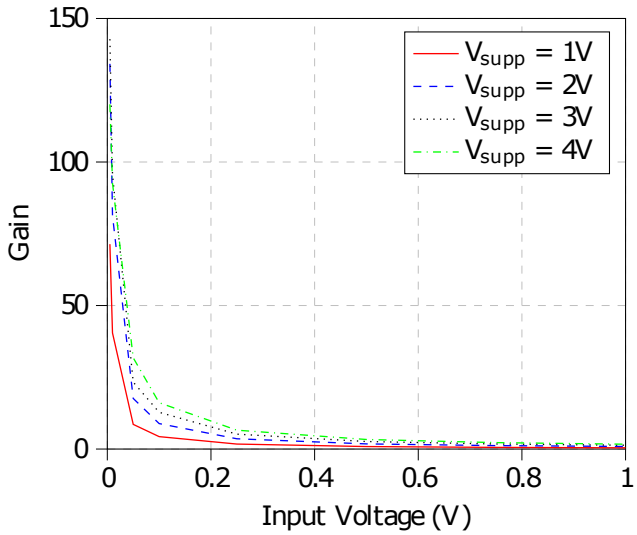


Figure 54: Gain versus input voltages, according to the variation of supply voltages of the designed voltage amplifier.

Through I_{supp} and V_{supp}, it is possible to calculate the power consumption of the amplifier as formulated in Equation 43.

$$P = I_{supp} \cdot V_{supp} \tag{43}$$

Hence, the power consumption of the circuit is $363.23\,\mu W$.

To measure PSRR of the circuit, the schematic plotted in Figure 55 was used. An AC voltage of $10\,\mu V$ at $10\,kHz$ (V_{dis}) was added to the supply terminal. The noise created by the power supply that is rejected by the amplifier is measured. Plus, a filtering capacitor (C_f) of $5\,pF$ is added.

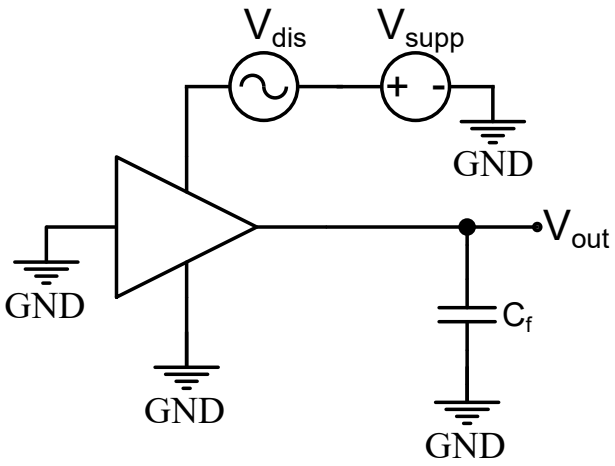


Figure 55: Circuit used for PSRR simulation of the amplifier.

The power supply gain (A_{ps}) is the ratio between the output voltage peak-to-peak and the supply voltage, as expressed in Equation 44. Since the amplitude of the output voltage is $6.505\,mV$ and the supply voltage is $2\,V$, A_{ps} of $3.25 \cdot 10^{-3}$ was obtained.

$$A_{ps} = \frac{V_{out,pp}}{V_{supp}} \tag{44}$$

The nominal gain after a $5\,mV$ at $10\,kHz$ input waveform, with $V_{supp} = 2\,V$ was 134.2 (Equation 45). By applying the both gains in Equation 46, a PSRR of $41\,292$ was calculated, or $46.16\,dB$ (Equation 47).

$$A_v = \frac{V_{out,pp}}{V_{in,pp}} \tag{45}$$

$$PSRR = \frac{A_v}{A_{ps}} \tag{46}$$

$$PSRR(dB) = 10 \cdot log(PSRR) \tag{47}$$

The temperature stability was also analyzed and the circuit behaviour changes with temperature. Figure 56 shows how the output signal changes with a temperature range from $-40\,°C$ to $150\,°C$. The output voltage peak to peak is higher for low temperatures and decreases with the increase of temperature. Using an input of $5\,mV$ at $10\,kHz$ and $V_{supp} = 2\,V$, with $-40\,°C$, the $V_{out,pp}$ is $1.48\,V$. At $150\,°C$, $V_{out,pp}$ is $1.13\,V$. The difference in the outputs is reduced compared to the difference between the temperatures. Nonetheless, the circuit should work near from the environment temperature, $25\,°C$.

3.2.4 Discussion

A circuit capable of amplifying the piezoelectric signal to be further processed, with a high gain and low power consumption, was achieved in these simulations.

The market offers a variety of amplifiers, more related to differential and operational amplifiers, but with the right features, those can be used for this application. Within the options are NCV952 from ON Semiconductor (ON , 2015), TLV314 from Texas Instruments (Tex, 2016), and LMV321L from STMicroelectronics (STM, 2014).

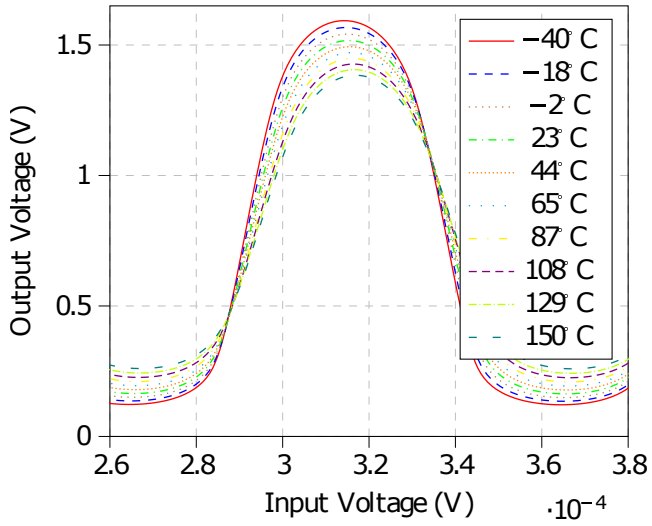


Figure 56: Output signal of the amplifier according to the variation of the temperature.

A comparison between the proposed voltage amplifier and off-the-shelf components is presented in Table 8. The features of the commercial components were taken from the datasheets. These features were represented for a voltage supply of $3\,V$, $2.7\,V$ and $1.8\,V$ for NVC95, LMV321L and TLV314, respectively.

According to the specifications and goals of the systems, the proposed circuit shows an overall performance better than the commercially available components. Although the supply and input voltage range of this work are smaller than the others, for the final application only matters the reduced voltage supply and smaller input voltages. Therefore, those ranges are enough. Besides, the implemented circuit has the smallest offset voltage.

Despite the gain of the proposed work being reduced, it is enough for input voltages in the range of $10^{-3}\,V$. This was the primary purpose of the voltage amplifier, to increase the input signal into a range detectable for the other circuits. Moreover, the capacity for rejection the power supply noise in this work is average compared to the others. NVC95 has the best PSRR, but a very high power consumption. Regarding the power consumption, TLV314 has the lowest value. However, its PSRR and offset voltage are worse than the proposed amplifier. Therefore, the performance of this work is generally better than the others.

3.2.5 Summary

A high gain and low power voltage amplifier, with two-stage, was designed. In comparison to commercial components, this circuit performs better for the purpose. The specifications which were not accomplished, in the worst case are reasonably good for energy harvesting applications.

Table 8: Comparison of the proposed voltage amplifier with commercial components.

References	NCV95 (ON , 2015)	LMV321L (STM, 2014)	TLV314 (Tex, 2016)	Proposed Amplifier
Voltage Supply (V)	2.7 - 16	2.7 - 5.5	1.8 - 5.5	1 - 4
Input Voltage (V)	$V_{ss} - 0.3$ - $V_{DD} + 0.3$	$V_{ss} - 0.3$ - $V_{DD} + 0.2$	$V_{ss} - 0.5$ - $V_{DD} + 0.5$	-1 - 1
Offset Voltage (V)	0.6m	1m	0.75m	8μ
Gain (dB)	88	39	85	42.56
Power Supply Rejection Ratio (dB)	60	-	35	46.16
Quiescent Current (A)	$0.7\,m$	$120\,\mu$	$122\,\mu$	$49.5\,\mu$
Power consumption (W)	$2.1\,m$	$324\,\mu$	$219.6\,\mu$	$363.23\,\mu$
Temperature (°C)	-40 - 125	-40 - 125	-40 - 125	-40 - 150

Further improvements can be made to replace the capacitors and resistors by MOSFETs, to reduce the occupied area and proceed to the fabrication of an IC, using the $0.13\,\mu m$ CMOS technology.

3.3 Rectifier

The power management circuit of an energy harvester extracts the energy generated by the transducer element, converts it into usable electric energy for a specific application and conveyes it to the requesting devices. The piezoelectric harvesters produce an AC signal that needs to be converted into a DC signal, through a rectifier, and storage to power up electronic systems (Sun et al., 2016; Herbawi et al., 2013). The vibrational energy harvesting systems have a broadband operating frequency range with low output power and voltage (Yang et al., 2013). Therefore rectifiers should be capable of handling a wide voltage operating range with low power consumption to achieve high PCE (Peters et al., 2011; Wong et al., 2016).

CMOS technology is predominant in industries due to its low-cost and high-performance solution, as the major technology for fabricating IC and chips (Baker, 2010). Although conventional rectifiers have simple topologies, they are not suitable for low power applications, due to its high power dissipation and leakage current, which

results in low efficiency. Rectifiers implemented in CMOS processes have been proposed as a better option for applications that require low power consumption, reduced power dissipation and present no reverse current, to achieve a high PCE. Therefore, the developed rectifier explores this technology, producing a circuit tailored to the desired requirements.

This work aims to develop a CMOS rectifier with low power and high efficiency for energy harvesting applications. The specifications for this circuit are a low forward voltage, lower than $0.4\,V$, low power consumption, and a minimum reverse voltage or, in other words, a breakdown voltage, of around $30\,V$. Since the power consumption is limited by the leakage current in the subthreshold region, the circuit needs a low leakage current, from fA to pA range. Moreover, the rectifier needs to have a voltage and power efficiencies as high as possible.

3.3.1 Design and Modeling

Recent literature was reviewed and described in section 2.3, making this work up to date on the newest techniques and selecting features to optimize the system. The choice was made from conventional, passive and active rectifiers, through iterative circuit implementation and consequent simulations.

Diodes are basic components of passive rectifiers, thereby different Schottky diode models were simulated varying their SPICE parameters to understand which one has the best behaviour. An overview of the models is exhibited in Table 9, where I_S is the saturation current, N the emission coefficient, R_S the ohmic resistance, TT the transit time, C_{JO} the zero-bias junction capacitance, V_J the junction potencial, M the grading coefficient, EG the activation energy, BV the breakdown voltage and I_{BV} the current at the breakdown voltage.

The simulations were carried out by a sinusoidal input signal of $1.5\,V$ at $50\,Hz$ to a diode in series with a resistance of $1\,k\Omega$. For each diode, its I-V characteristic curve and output signal are analysed.

The Da1N4004 presented the worst performance, with a forward voltage (V_f) of $0.3\,V$ and with the output equals to the signal applied in the input terminal. The Dmurs360t3 has the best performance, thanks to its capability of partially nulling the negative half-cycles of the input signal and $V_f = 0.25\,V$. Both models, 1N5711 and HSMS2850, are capable of nulling the negative values of the input signal. However, HSMS2850 has higher gain and lower V_f than the 1N5711 model. The V_f is $0.2\,V$ using the HSMS2850 diode and $0.1\,V$ with the 1N5711. Therefore, the HSMS2850 Schottky diode model has the best behaviour.

A full-wave rectifier was designed with four Schottky diodes, whose layout is illustrated in Figure 57. For low-voltage IC applications, the V_f is responsible to reduce the PCE. Due to this, Schottky diodes with a low forward

Table 9: Diodes model and respective SPICE parameters.

Diode Model	SPICE Parameters
Da1N4004	$I_S = 18.8\,nA$, $R_S = 0\,\Omega$, BV $= 400\,V$, $I_{BV} = 5\mu\,A$, $C_{JO} = 30\,F$, M $= 0.333$, N $= 2$
Dmurs360t3	$I_S = 0.3\mu\,A$, $R_S = 0.049\,\Omega$, BV $= 600\,V$, $I_{BV} = 10\mu\,A$, $C_{JO} = 0.137\mu\,F$, M $= 0.744$, N $= 2.2$
1N5711	$I_S = 315\,nA$, $R_S = 2.8\,\Omega$, BV $= 70\,A$, $I_{BV} = 10\mu\,V$, $C_{JO} = 2\,pF$, M $= 0.333$, N $= 2.03$
HSMS2850	$I_S = 3\mu\,A$, $R_S = 25\,\Omega$, BV $= 3.8\,V$, $I_{BV} = 0.3\,mA$, $C_{JO} = 0.18\,pF$, M $= 0.5$, N $= 1.6$
Default	$I_S = 10^{-14}\,A$, $N = 1$, $R_S = 0\,\Omega$, $TT = 0\,s$, $C_{JO} = 0\,F$, $V_J = 1\,V$, $M = 0.5$, $EG = 1.11\,eV$, $BV = \infty\,V$, $I_{BV} = 10^{-3}\,A$

drop can be used to enhance efficiency. Nevertheless, its production cost is high compared to a standard CMOS process.

A cross-coupled PMOS rectifier, with two p-channel MOSFETs connected with two diodes, is shown in Figure 58. An issue of this circuit is its poor efficiency. To overcome this drawback, it is necessary to replace the diodes by active circuits that can switch between operation modes fast and efficiently, avoiding reverse current. Therefore, a comparator based on Lam et al. (2006) is simulated and connected to the PMOS. However, the output signal was very attenuated due to the high power dissipation.

A comparator based on Louzada (2017) is designed and shown in Figure 59. The transistors M1, M2, M3 and M4 constitute a common gate comparator. M1 and M2 work as an inverter that provides either non or DC signal at the output, while M3 and M4 are a voltage divider. The capacitor C_1 and the voltage divider are responsible for decreasing the comparator delays. Besides, both M3 and M4 are in charge of switching the inverter composed by M5 and M6. As long as it is still not fully charged, C_1 allows the AC signal input controls the rise of the signal responsible for the inverter.

The comparator is tested using an input sinusoidal signal of $1.3\,V$ at $10\,kHz$ and a voltage supply of $1.2\,V$. The dimensions of the transistors are exhibited in Table 10.

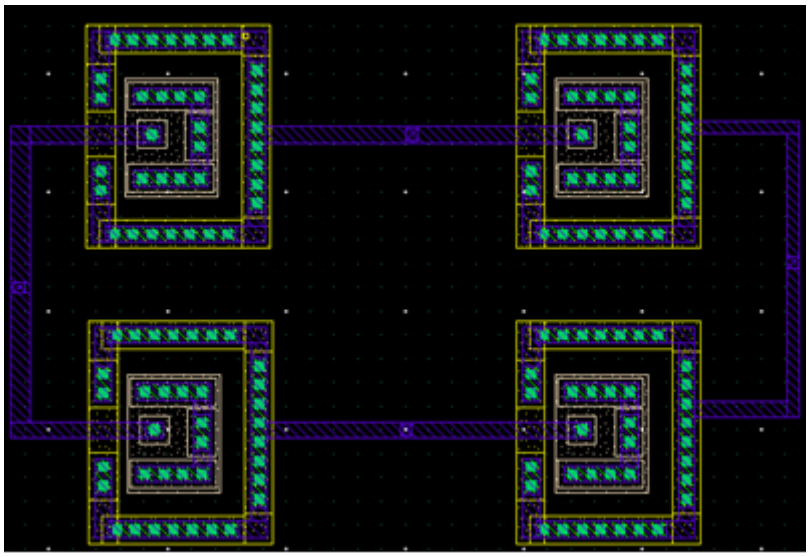


Figure 57: Layout of a full-wave rectifier using Schottky diodes.

Table 10: Dimensions of the transistors from the comparator circuit.

Transistor	**Width (μm)**	**Length (μm)**
M1	47.6	0.13
M2	11	0.13
M3, M6	0.16	0.13
M4	0.7	0.13
M5	5	0.13

The comparator behaves as expected when the voltage on the gates of the inverter is higher than half of the DC voltage supply. In this case, the output signal is null. Otherwise, the output voltage is equal to the supply voltage. However, the size of the capacitor C_1 influences the operation of the circuit. Through a parametric analysis is possible to observe that when C_1 decreases, the performance of the comparator is worst. To compensate this handicap, it is necessary to increase the frequency of the input signal. Consequently, it is crucial to scale the capacitor.

There are two important variables concerning the capacitor scaling: the operating frequency of the circuit, which reveals how long the capacitor should be charged, and the electrical resistance of the circuit from the capacitor position, which is around $413.9\,\Omega$. The relationship between the resistance and capacitance is given by capacitor charge time (τ) as represented in Equation 48.

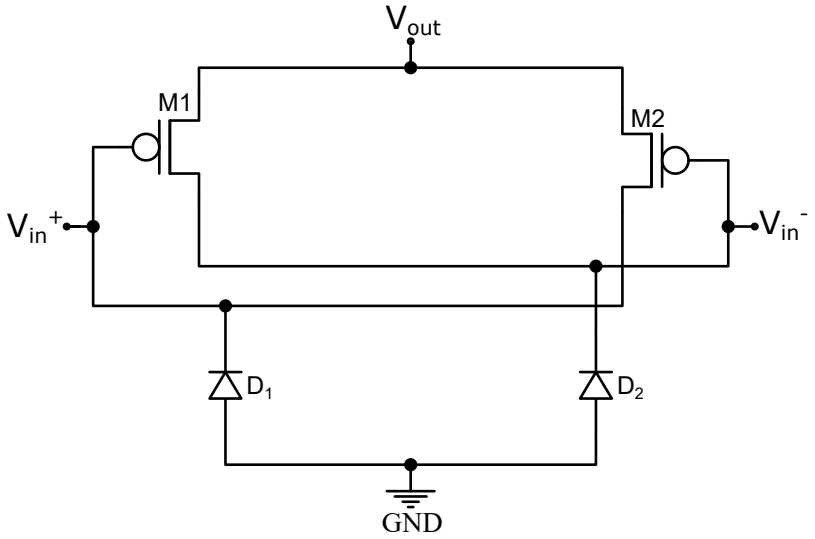


Figure 58: Schematic design of a full-wave rectifier with cross-couple PMOS.

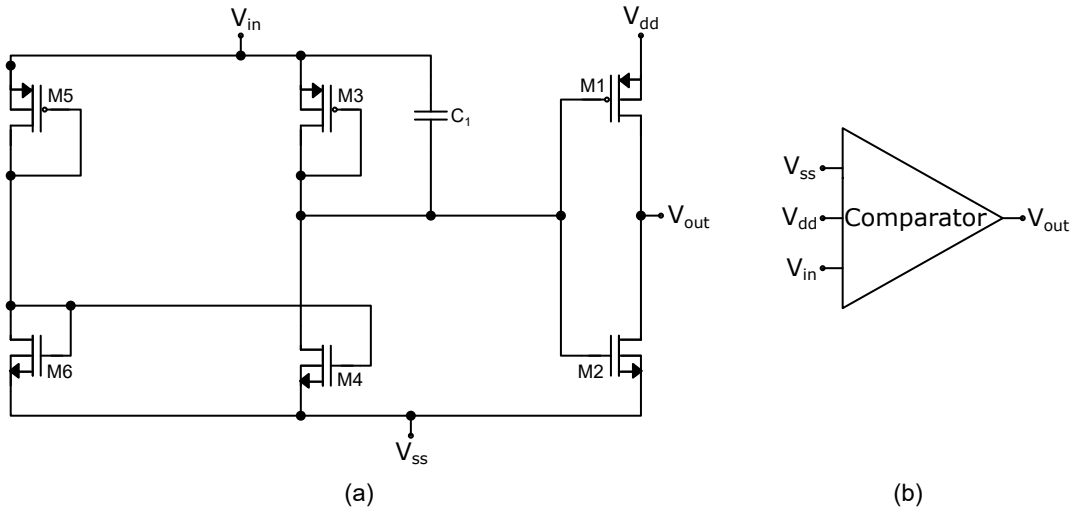


Figure 59: Design of a comparator: (a) schematic and respective (b) symbol.

$$\tau = R \cdot C \tag{48}$$

The capacitor charge time for the circuit must be less than the time for the AC signal goes from zero to the peak voltage. Hence τ should be one-quarter of the input signal. Thereby, for an input frequency of $10\,kHz$, $\tau = 25\,\mu s$. In other words, in $25\,\mu s$ C_1 is charged or discharged at 63% of its total charge. When pass $5 \cdot \tau$ it is considered a charge of 99.3%.

The optimal capacitance calculated for $25\,\mu s$ is $12.08\,nF$. When the size of the capacitor is equal or bigger than the optimal value, the capacitor is fully charged only at the peak voltage of the input signal. The input directly influences the inverter, controlling it more than the necessary time. This causes a delay in the comparator and amplifies the reverse current. Therefore, the chosen value for C_1 was $10\,nF$.

This comparator is implemented on a active rectifier, as depicted in Figure 60. Two comparators are supplied by the output voltage of the rectifier.

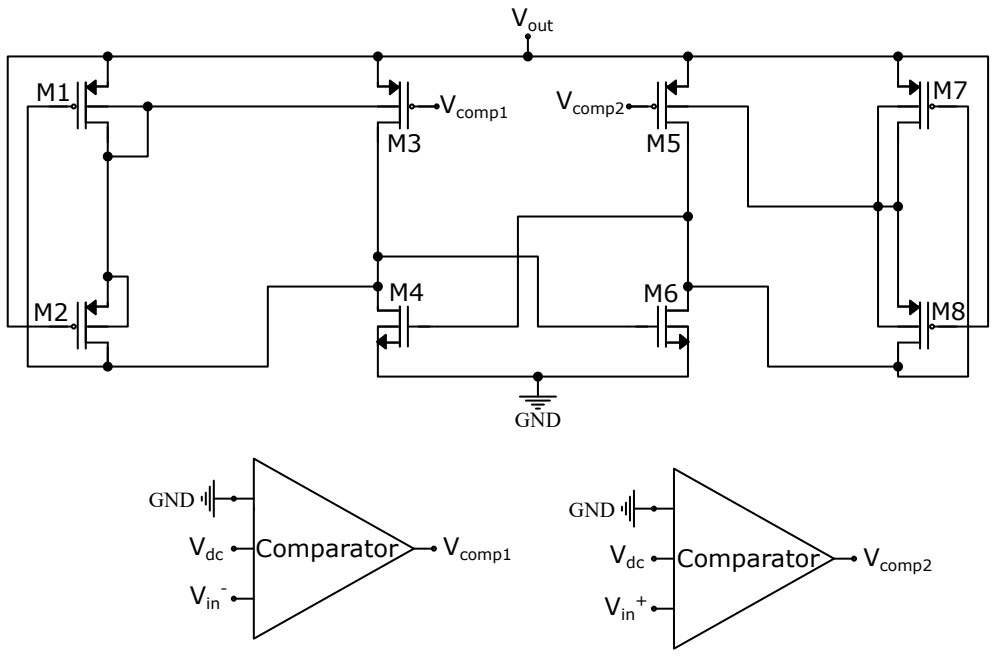


Figure 60: Structure of a full-wave active rectifier.

The rectifier was simulated with $V_{in} = 1.3\,V$ at $10\,kHz$, $R_L = 1\,k\Omega$ and $C_L = 10\,\mu F$. The transistor dimensions used in the active rectifier are specified in Table 11. The output voltage is $1.07\,V$, but due to the high power consumption, approximately $1.16\,mW$, the PCE is 34.8%. Besides, the power consumption of the comparator is $690\,\mu W$.

Table 11: Dimensions of the transistors from the active rectifier.

Transistor	Width (μm)	Length (μm)
M1, M3, M7, M8	10	0.13
M3, M4, M5, M6	100	0.13

In the attempt to improve the performance of the rectifier, a comparator based on Kakoty (2011) was designed. The comparator is comprised of four subsections: a differential gain stage, a second gain stage, a current source and an inverter, as shown in Figure 61. Additionally, the ratio between width and length of the transistors are displayed in Table 12.

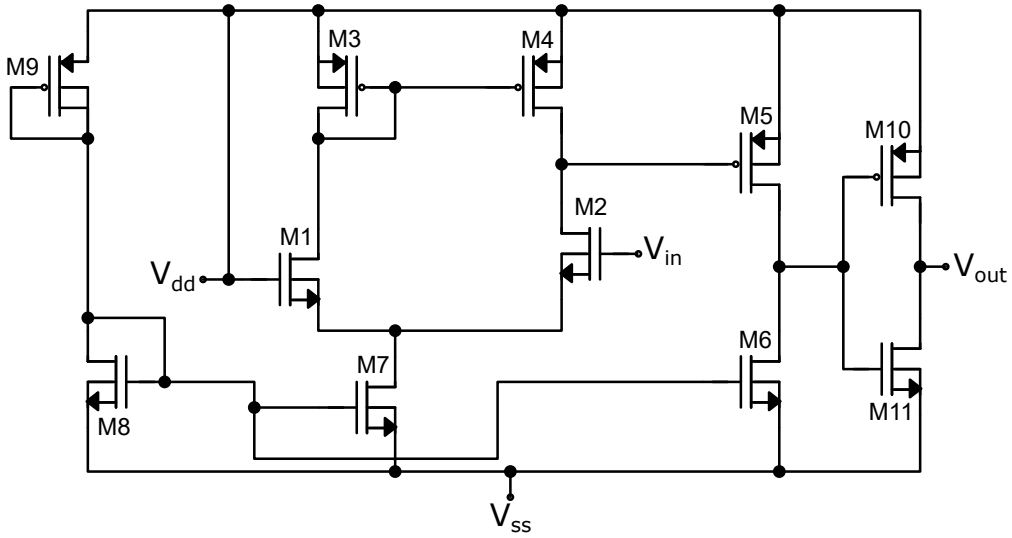


Figure 61: Circuit design of a four-stage comparator.

The transistors M1, M2, M3 and M4 constitute the first stage, where M1 and M2 form the primary input stage of the amplifier. The current mirror between M3 and M4 is advantageous since it creates a significant output resistance a reduced die area and performs the differential to the single-ended conversion of the input signal. The maximum output voltage is limited by keeping M4 in saturation, as presented in Equation 49.

$$V_{out,max} = V_{dd} - V_{SD,sat} \tag{49}$$

The minimum output voltage is determined by the voltage on the gate of M2 (Equation 50):

$$V_{out,min} = V_{G2} - V_{th} \tag{50}$$

Table 12: Dimensions of the transistors of the four-stage comparator.

Transistor	Width (μm)	Length (μm)
M1, M2	0.28	0.13
M3, M4	0.39	0.13
M5. M10, M11	0.26	0.13
M6	1	0.13
M7	10	0.13
M8	10	0.13
M9	0.15	0.13

M5 and M6 accomplish the second gain stage. The purpose of this stage is to provide an additional gain in the amplifier. The voltage on the drain terminal of M2 is amplified by M5, along with M6.

In the current source subsection, M8 and M9 supply a voltage between the gate and source of M7 and M6. The current on M6 and M7 is controlled by the bias string, based on their gate to source voltage. Proper biasing for the others transistors in the circuit is controlled by the node voltages present in the circuit itself.

Finally, M10 and M11 constitute the inverter, providing either ground signal or DC signal at the output. When V_{G10} and V_{G10} are higher than half of V_{dd}, $V_{out} = 0\,V$; otherwise, $V_{out} = V_{dd}$.

Analogous to the previous case, the comparator was tested, integrating a two-stage active rectifier, with a NVC and a BR technique. This concept of a two-stage active rectifier is further developed in section 3.3.2. The same input conditions of previous simulations, are applied in these simulation. Regarding power consumption, it suffers an improvement. The rectifier consumes $9.86\,\mu W$ and the comparator $20.88\,\mu W$. Nonetheless, its PCE is reduced, 17.8%.

To overcome these limitations, simpler comparators based on logic gates are designed. A NAND (Figure 62(a)), a NOR (Figure 62(b)) and a NOT (Figure 62(c)) gate are simulated using both structures, a full-wave active rectifier and a two-stage active rectifier. The overall performance is summarized in Table 13. For all the performed simulations, the input voltage and frequency were settled at $1.5\,V$ and $10\,kHz$, respectively. According to Table 13, it is concluded that a two-stage active rectifier structure has a higher PCE and lower power consumption than a full-wave active rectifier. Mostly due to the use of only one comparator in the first case. Between the three logic gates, the NOT stands out. Beyond having a higher PCE, it also has lower power consumption. Thus, a NOT gate is chosen to play the role of a comparator. Next section explains the final proposed rectifier.

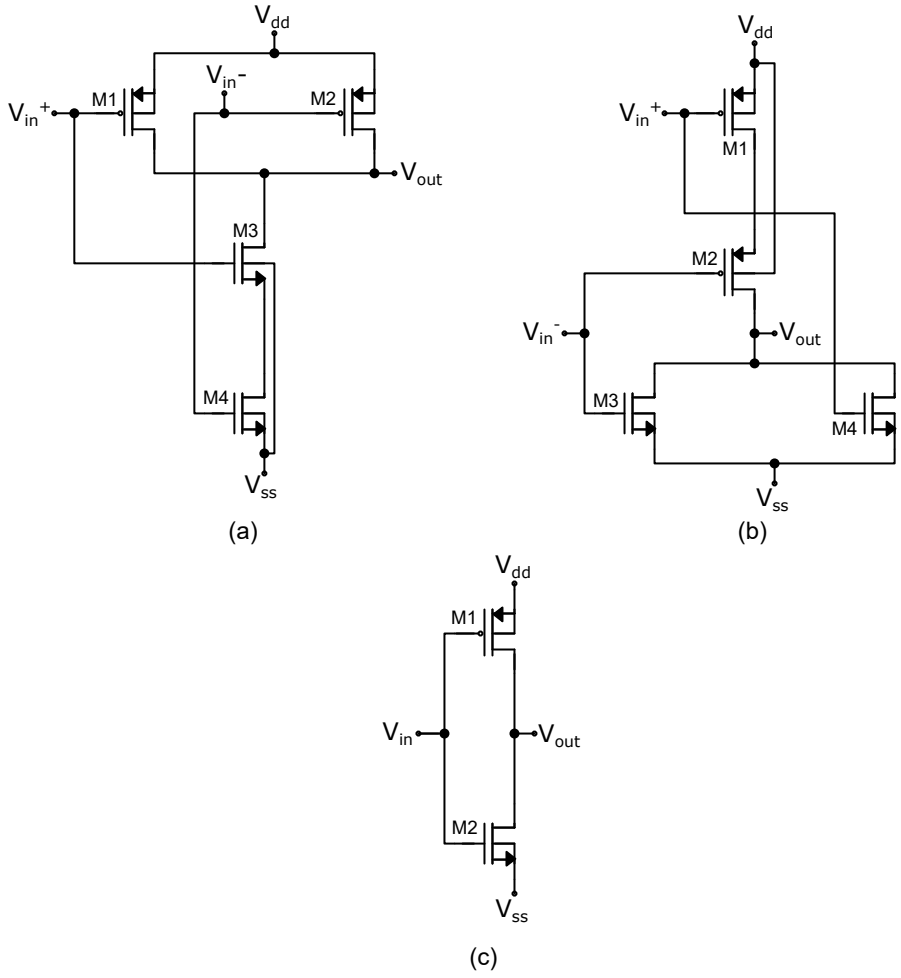


Figure 62: Schematic of the logic gate: (a) NAND, (b) NOR, and (c) NOT.

Table 13: Performance summary of different logic gates in a full-wave and two stage active rectifiers topologies.

Features	NAND$^{\odot}$	NOR$^{\odot}$	NOT$^{\odot}$	NAND$^{\otimes}$	NOR$^{\otimes}$	NOT$^{\otimes}$
Output Voltage (V)	997.3m	983.5m	875.6m	784.3m	780.4m	779.4m
Power Conversion Efficiency (%)	6.91	31.71	31.97	25.4	38.08	40
Comparator Power Consumption (W)	193.3μ	909n	230.1n	10.51μ	1.11μ	247.4n
Power Consumption (W)	994.6μ	1.26m	1.256m	12.3μ	16.80μ	17.71μ
Load Resistor (Ω)	1k	1k	1k	50k	50k	50k

$^{\odot}$ Full-wave active rectifier topology, $^{\otimes}$ Two-stage active rectifier topology.

3.3.2 Proposed Rectifier

This section presents the study and the design of a rectifier. A two-stage structure has been taking into consideration, along with a dynamic body bias circuit, as demonstrated in (Cha et al., 2012). The comparator implemented in this study is based on overcoming previous drawbacks and adapted to the required conditions. The impact of employing an MOSFET Bypass PMOS Diode (MBPD), as in (Peters et al., 2010; Li et al., 2014), is tested to enhance the system performance under undesirable work conditions.

A simple circuit of a two-stage active rectifier, depicted in Figure 63, was designed, dismissing any resistor or capacitor. It consists of a passive stage implemented by a NVC and an active stage accomplished through an active diode, controlled by a comparator with BR, additionally in parallel a bypass PMOS diode MBPD.

Under DC operating conditions, C_L is given by Equation 51, where I_D is the current flowing through the forward-biased junction; τ_T is the carrier lifetime; V_T is the thermal voltage, and n is the number of free electrons in the material (Baker, 2010). Due to C_L, the ripple resulted from the AC-DC conversion can be reduced, smoothing the DC voltage (Peters et al., 2007). When the voltage from the rectifier is higher than that of the capacitor, C_L

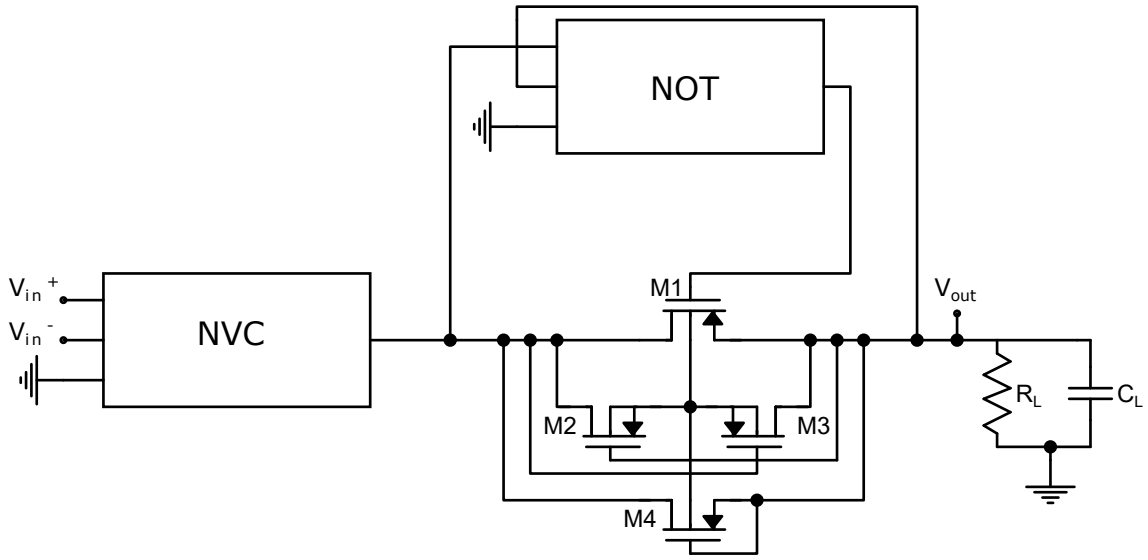


Figure 63: Projected two-stage active rectifier circuit.

charges up. When the rectifier voltage drops down, C_L provides the required current from its stored charge, supplying the rectifier anytime it is not available.

$$C_L = \frac{I_D}{n \cdot V_T} \cdot \tau_T \tag{51}$$

Negative Voltage Converter

The NVC in Figure 64 is the first passive stage of the two-stage concept applied to the rectifier, responsible for converting the negative half-waves of the sinusoidal input into positive ones.

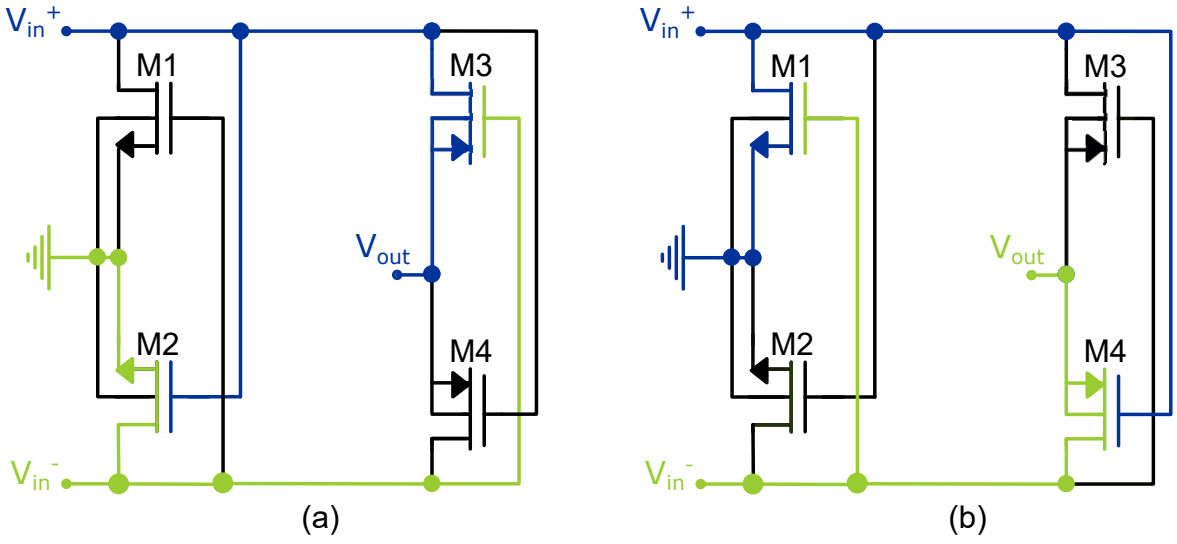


Figure 64: Negative voltage converter circuit conducting for (a) positive and (b) negative half-cycles.

This conversion is simply accomplished by four standard MOSFETs: two NMOS and two PMOS. This stage is entirely passive. The transistors are driven by the alternating input voltage and work in an extensive frequency range, up to MHz. It eliminates the V_{th} loss between the input and the output compared to a diode-connected MOS transistor.

The working principle of NVC is illustrated in Figure 64. When $|V_{in}^{+}| > |V_{in}^{-}|$ the transistors M2 and M3 conduct, as depicted in Figure 64(a). Thereby, V_{in}^{+} activates M2, allowing V_{in}^{-} to pass by and connecting to the ground, cancelling the negative half-cycle. Since M3 is turned ON by negative amplitudes on its gate, the current passes through it and $V_{out} = V_{in}^{+}$. On the contrary, when $|V_{in}^{+}| < |V_{in}^{-}|$, the circuits behaves as Figure 64(b). In this case, M1 and M4 are turned ON by V_{in}^{-} and V_{in}^{+}, respectively. M1 connects the positive half-cycles to ground, while M4 enables the current to connect to the output; therefore, $V_{out} = |V_{in}^{-}|$.

For low voltage design, a large width is needed to keep the voltage drop over the device low. The transistor size is chosen to keep its on-resistance (R_{ON}) low. Hence NVC reaches high efficiencies, even at low input voltages without overlooking the parasitic capacitances of large transistors. The trade-off on reducing R_{ON} is that it involves increasing the width (W) and length (L) ratio, resulting in higher parasitic capacitance and a larger silicon area. Apart from W and L, R_{ON} is a function of electron and hole mobility (μ_n and μ_p, respectively), oxide capacitance (C_{OX}), V_{th}, and signal voltage (V_{GS}) of the n- and p-channel MOSFETs as formulated in Equation 52. The selected transistor size for this design is 10/0.13 (W/L) in μm. Increase the transistor width further would result in a decrease in the voltage drop, but also a large area. No supplementary dynamic BR system is necessary on this stage, due to the bulk connections to the higher and lower voltage nodes.

$$R_{ON} = \frac{L}{\mu \cdot C_{OX} \cdot W \cdot (V_{GS} - V_{th})} \tag{52}$$

The main advantage of this configuration is the ability to convert the input voltage up to MHz into a positive signal on the output. Otherwise, it can not charge the C_L and is not capable of controlling the current direction. Therefore a second stage is implemented to block the reverse current.

Active Diode

A second stage is added to the system since if the input voltage exceeds the V_{th}, current backflow occurs and C_L, directly connected, would discharge. The active diode, implemented by a PMOS switch controlled by a comparator, is represented by M1 in Figure 63. The current flows only in the output direction, preventing reverse current, which involves almost no voltage drop, working similar to an ideal diode. An active diode has a permanent

current consumption caused by the control circuit. The conduction voltage drop of the active diode is smaller than the forward-biased voltage of a standard diode. M1 drain and source terminals are equivalent to the anode and cathode of a diode, respectively, and the comparator detects the voltage between them.

Furthermore, a BR circuit is established by M2 and M3 from Figure 63. Both transistors are connected to M1's bulk to restrain latch-up. Due to this, a low-impedance path is generated between the power supply and the ground during the start-up process. As a result, M1's bulk is switching between the higher and lower potential terminal, avoiding leakage current. M2 and M3 can have a reduced width considering only a slight current flows during the start-up phase.

Comparator

Active rectifiers that use comparators, the transistors have their gate voltage controlled, minimizing the reverse current that appears during operation mode changes. The purpose of this is to speed up the transistor switching process and eliminate this current. The comparator characteristics such as delay, power consumption, and output drive capability have a significant effect on the maximum achievable efficiency.

A suitable comparator design with low power consumption and fast response is imperative to the rectifier. If the comparator is slow, only a portion of the available energy can be transferred to the capacitor, causing a high risk of current backflow. A high-speed comparator with high power consumption is also not desirable because the overall efficiency sharply decreases.

The comparator architecture is obtained by a NOT gate, which is simple, quick and low power, as shown in Figure 65. The supply voltage (V_{supply}) is sourced from C_L. When the output voltage (V_{out}) is higher than the NVC output voltage ($V_{out,NVC}$), the comparator output voltage ($V_{out,comp}$) is high, turning OFF the switch and, consequently, preventing reverse current to occurs. Reversely, in the opposite condition, $V_{out,comp}$ is a low signal to turn ON the switch.

A current starved technique is added to reduce the current and diminish power consumption. The transistors M5 and M6 constitute the traditional NOT gate, working as an inverter, while M7 and M4 limit the current available to the inverter. The current is equal in each branch due to the current mirrors M1 and M4, and M3 and M7, hence $I_{D2} = I_{D4}$. In order to reinforce the current, M1 and M3 create p and n-type mirrors, respectively. The Equation 53 expresses the current in M2 (I_{D2}), while operating in the subthreshold region, which means that the condition $V_{GD} > |V_{th}|$ is verified. Besides, since M2 has the gate tied to the drain $V_D = V_G$, and consequently $V_{DS} = V_{GS}$.

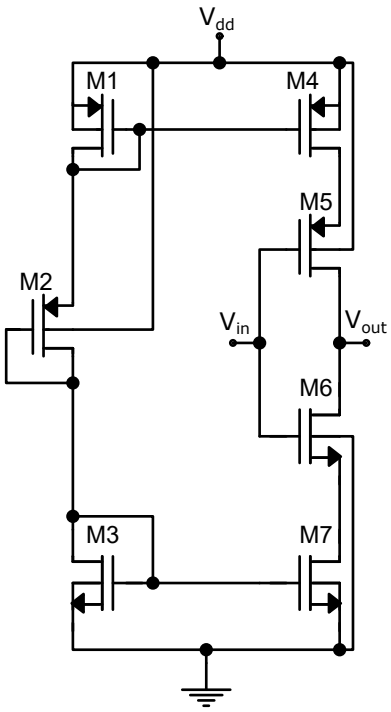


Figure 65: Comparator circuit implemented by a NOT gate with starving current technique.

$$I_{D2} = \mu_p \cdot C_{ox} \cdot \frac{W_2}{L2} \left[(V_{GS} - |Vth|) \cdot V_{GS} - \frac{V_{GS}^2}{2} \right] \cdot (1 + \lambda \cdot V_{GS}) \tag{53}$$

The current in M2 only depends on its dimensions ratio, since the drain currents of M1 and M3 are the same and fixed by M2. Therefore M2 is smaller than the other to limit the current. Thus, the transistors' dimensions are the same, except for M2, as shown in Table 14.

Table 14: Dimensions of the transistors from the proposed comparator circuit.

Transistor	**Width (μm)**	**Length (μm)**
M1, M3, M4, M5, M6, M7	0.18	0.13
M2	0.15	0.13

Mosfet bypass PMOS diode

The transistor M4 in Figure 63 is positioned in parallel with the switch, M1, ensuring a safe start-up of the active diode. It enhances the trustworthiness of the active diode under worst-case conditions, including process variation with high V_{th} and extreme temperatures. Its only drawback is the increasing area, yet irrelevant when compared to the advantages. M4 stops operating and keeps a high ohmic state after the active diode starts working.

The need for a bypass depends on the process and operating conditions, thus to understand its requirement, an evaluation is presented by simulation in section 3.3.3. A width of $0.18\,\mu m$ in combination with a length of $0.13\,\mu m$ was used.

3.3.3 Results

The proposed circuit is simulated using the Cadence environment and SPICE simulations tools, with the appropriate $0.13\,\mu m$ CMOS technology parameters.

The most favorable dimension for M1, M2 and M3 from Figure 63 is 0.18/0.13 (W/L) μm. The signals in Figure 66 show the behaviour of different sub-circuits. A sinusoidal input voltage (V_{in}) with $1.5\,V$ at $10\,kHz$ is selected to perform the simulations. As expected, the $V_{out,NVC}$ signal only has positive values from converting the negative half-waves into positives ones.

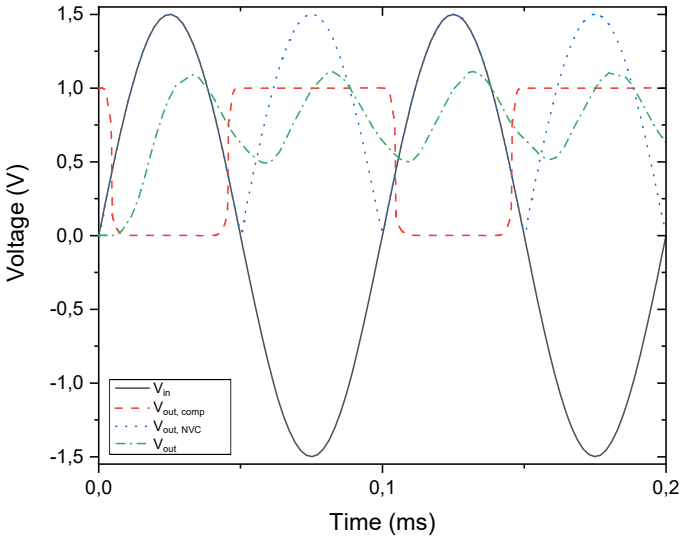


Figure 66: Operational principle of the NVC ($V_{out,NVC}$), the comparator ($V_{out,comp}$), and the rectifier (V_{out}), with V_{in} as the input signal for each simulation.

The simulated results reveal the NOT gate works properly and effectively as a comparator. When V_{in} is higher than half of V_{supply}, $V_{out,comp}$ is equal to the ground. In reverse, when V_{in} is lower than half of V_{supply}, $V_{out,comp}$ is equal to V_{supply}, which is a DC source of $1\,V$. An essential characteristic of the comparator is the power consumption, which the lower it is, the better. The power consumption of this comparator is $114\,nW$.

The output signal from the active rectifier, V_{out}, is exhibited in Figure 66. Every half-wave is applied to load up C_L. The input parameters for this simulation are $680\,pF$ and $50\,k\Omega$, correlative to C_L and R_L, respectively.

As explained in the previous section, it is necessary to simulate the active rectifier with and without the MBPD. Figure 67 depicts how the maximum output voltage of the active rectifier ($V_{out,max}$) differs through the temperature variation from $-20\,^{\circ}C$ to $80\,^{\circ}C$, including or not the MBPD transistor. The input parameters are the same as in the previous simulation. In the absence of the MBPD, V_{out} varies on an extension of $40\,mV$. However, in the presence of it, V_{out} suffers a variation in a spectrum of $26\,mV$. Beyond this, $V_{out,max}$ is significantly higher with the MBPD. Moreover, the rectified signal amplitude slightly decreases with the increasing of the temperature.

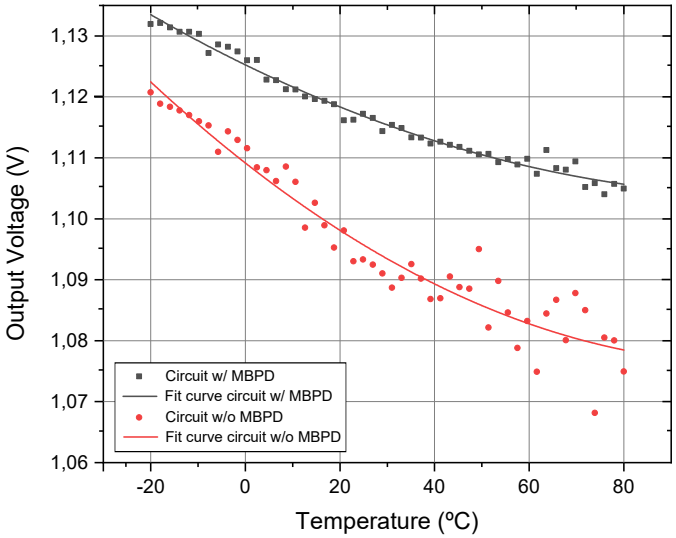


Figure 67: Output voltage according to the temperature variation, with and without the MBPD, and 2nd order polynomial fitting.

The main aspects of rectifiers are the $V_{out,max}$ and its efficiency depending on the input frequency and V_{in}. The higher the efficiency, the less power is wasted. To measure the PCE is crucial to follow a few steps. Firstly, it is necessary to determine the input power (P_{in}), as expressed in Equation 54.

$$P_{in,rms} = rms\left(I_{in} \cdot V_{in}\right) \tag{54}$$

Then the power consumption of the comparator (P_{comp}), was calculated according to Equation 55 and the output power (P_{out}) is expressed in Equation 56.

$$P_{comp,rms} = rms\left(I_{dd} \cdot V_{dd}\right) \tag{55}$$

$$P_{out,rms} = rms\left(\frac{V_{out}^2}{R_L}\right) - P_{comp,rms} \tag{56}$$

Finally, it is possible to determine the PCE, dividing P_{out} by P_{in} as formulated in Equation 57 (Technologies, 2017). A particularity is the use of root mean square (rms) to obtain more reliable results instead of extrapolating. For an arbitrary periodic sinusoidal waveform, f(t), of period T, the value of rms is described in Equation 58 (Beranek and Mellow, 2012).

$$PCE = \frac{P_{out,rms}}{P_{in,rms}} \cdot 100 \tag{57}$$

$$rms(f(t)) = \sqrt{\frac{1}{T} \cdot \int_0^T [f(t)]^2 \cdot dt} \tag{58}$$

The PCE and the V_{out} versus frequency is illustrated in Figure 68, demonstrating that it works properly from $10\,Hz$ to $3\,kHz$. At a certain point, the maximum effective frequency is achieved by the comparator, and sudden V_{out} drops down, known as breakdown point. After this frequency, the active diode works unstable and must avoid operating under these conditions. At $1\,kHz$, the rectifier has the best performance with 40.4% of efficiency, while P_{comp} is $113.9\,nW$, and P_{out} is $17.7\,\mu W$. This simulation uses a parametric analysis and V_{in} is $1.5\,V$. Without the BR and MBPD techniques the PCE of the respective rectifier was 3.46%.

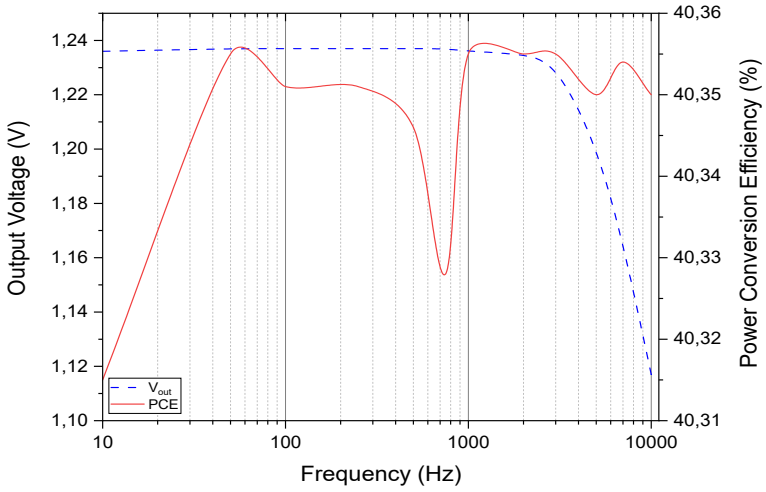


Figure 68: Output voltage and power conversion efficiency through different frequencies.

The $V_{out,max}$ and PCE through different V_{in} are exposed in Figure 69. The simulation is performed at $1\,kHz$ with a V_{in} spectrum from $100\,mV$ to $5\,V$. Thus the working V_{in} range is measured and varies from $0.6\,V$ to $4.5\,V$. The voltage efficiency (η_v) is defined in Equation 59. The maximum voltage efficiency is 82%.

$$\eta_v = \frac{V_{out}}{V_{in}} \cdot 100 \tag{59}$$

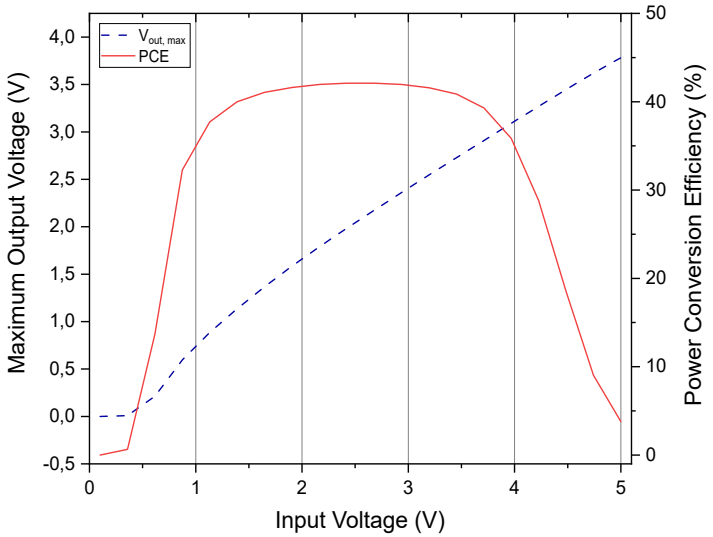


Figure 69: Output voltage and power conversion efficiency values, according to input voltage variations.

The simulated V_{out} and PCE versus R_L is plotted in Figure 70. The simulation is performed at $10\,kHz$ with a R_L spectrum from $1\,k\Omega$ to $1\,M\Omega$. The input parameters are the same as previously with an additional V_{supply} of $1\,V$. At $300\,k\Omega$, the PCE reaches a maximum value of 47% with a V_{out} of $1.45\,V$, corresponding to a voltage efficiency of 96.7%. Thus, the circuit generates high amplitudes for large values of the ohmic load. Bellow $30\,k\Omega$ V_{out} strongly decreases, and at $9\,k\Omega$, it reaches output values lower than the operational voltage.

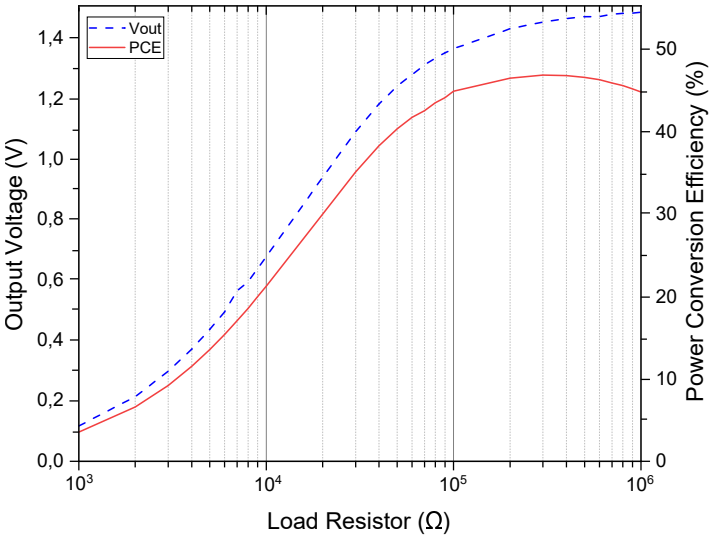


Figure 70: Simulated output voltage and power conversion efficiency through different ohmic load values.

Table 15: Comparison of the proposed rectifier with other previously reported.

References	Peters et al. (2010)	Peters et al. (2008)	Cha et al. (2012)	Li et al. (2014)	Proposed Rectifier
Technology (μm)	0.35	0.35	0.18	0.18	0.13
Input Frequency (Hz)	100 - 5k	1 - 100k	13.56M	10 - 1k	10 - 3k
Input Voltage (V)	0.5	1.25 to 3.75	1.5	0.45 - 1.8	0.6 - 4.5
Output Voltage (V)	0.45	2.15 $@V_{in} = 2\,V$	1.33	0.43 - 1.79	0.1 - 2.45
Load Resistance (kΩ)	50	50	1	50	50
Load Capacitor (F)	10μ	3.3μ	-	10μ	680p
Power Consumption (W)	19μ	110μ	1.76μ	197n	17.76μ
Power Conversion Efficiency (%)	70	95	81.9	84	40.4
Area (μm^2)	330 × 190	240 × 100	9000	-	17.6 × 16.2

3.3.4 Discussion

The final design encompasses the leading benefits from each specific research in the section 2.3. A direct comparison between the presented final circuit and previous works is presented.

The performance summary for the proposed rectifier circuit and previous studies are shown in Table 15, for comparison. The data are taken from a combination of published works.

The highest operation voltage found on previous rectifiers is achieved by Peters et al. (2008) and the lowest by Li et al. (2014) and Peters et al. (2010). The rectifier exposed in this work overcomes both of these features, operating at a wider input voltage. Furthermore, it has a larger frequency range than Cha et al. (2012) and Li et al. (2014), and still supporting lower frequencies. Beyond this, the higher frequency measured in this work

is below $20\,MHz$ Peters et al. (2007), making it suitable for biomedical applications since it avoids unwanted tissue heating.

In all the preceding works, the equation to measure the PCE neglects the power consumption of the active components, reaching inaccurate values. In this work, P_{comp} is a variable with high impact in Equation 56, since the higher the P_{comp}, the lower the PCE. The P_{comp} of the circuit described in this work is $113.9\,nW$, considerably less than the P_{comp} reported by Peters et al. (2010), which was $200\,nW$. Overall, the power consumption value of the suggested rectifier is low and trustworthy. Li et al. (2014) reported a $197\,nW$ power consumption rectifier at $450\,mV$ and $1\,kHz$ input signal. Under the same initial conditions as Li et al. (2014), the power consumption of the proposed rectifier is $19.27\,nW$. This means a reduction of 90.22% of the rectifier in this work compared to Li et al. (2014).

Regarding the ohmic load, an advantage of this rectifier is its capacity to maintain a high PCE and voltage efficiency within an extensive range of R_L. The highest value of PCE and voltage efficiency are 47% and 96.7%, respectively. The performance of Cha et al. (2012) sharply decreases for R_L values above $2\,k\Omega$ and with $10\,k\Omega$ is less them 9%. Comparing Cha et al. (2012) with the presented work, the PCE keeps consistent values, with small variation, while R_L increases, and at $10\,k\Omega$ the PCE is 21.3%. This means a PCE boost of 42.3% from the circuit in this work compared to Cha et al. (2012).

An important parameter for this design is the temperature independence of the circuit. Thus, a PMOS connected to the switch of the comparator was added to the proposal.The temperature stability is achieved by using a MBPD.

The two-stage active rectifier constitutes a crucial part of an IC for energy harvesting systems. The active area of the complete active rectifier circuit is around $(17.6 \times 16.2)\,\mu m^2$. The chip area is notable for the reduced dimensions and the miniaturization of the active rectifier was achieved using a $0.13\,\mu m/$ 8-Metal/ 2-Poly CMOS technology. Both, layout and chip fabrication is presented in section 3.4.

The choice of only one active diode is an advantage, decreasing power consumption. Moreover, the new active diode has a wideband of input voltage and frequency, and is implemented by a simple, efficient and low power comparator. Even further, the developed method to calculate the PCE is enhanced to have the most realistic and pragmatic values.

3.3.5 Summary

A efficient, reliable, low power and functional rectifier, accomplishing the requirements of low power and real-world applications, was designed.

The highlight of this system is low power consumption around $17.7\,\mu W$, under conditions of $1.5\,V$ as input voltage and a frequency range from $50\,Hz$ to $3\,kHz$. A novel architecture for the active diode consists of a NOT gate inspired topology performing a comparator role. The comparator power consumption is $113.9\,nW$, which is an advantage of this circuit compared to simulations in referenced literature.

The system overcomes previous drawbacks from published literature since the design was realized successfully without any capacitors and resistors, reducing the occupied area and having low power consumption. The fact that is resistor-less is an advantage, since in CMOS technology the resistors are responsible for significant anomalies. In combination with decreased transistors dimensions, the space occupied for the rectifier is notably smaller, comparatively to the literature.

The techniques used in this structure should establish a reasonably stable device. The rectifier system is straightforward, its power consumption is reduced and it operates in a wide voltage and frequency range in CMOS $0.13\,\mu m$ technology. The design of the rectifier has focused on low power energy harvesting applications for biomedical, industrial, and commercial fields.

3.4 Layout Design and Fabrication

Application-Specific Integrated Circuit (ASIC) Research and Development (R&D) can be costly to undertake because of high fabrication cost. As a result, it is necessary to ensure that the design process is well controlled. Each stage of the ASIC design and research process should be carefully monitored, and precautions are taken into account to ensure that the final design meets the requirements and operates properly in real-world applications. Errors occurring later in the process become progressively more costly to correct. In order to reduce future errors, it is crucial to investigate modelling, simulation and verification of the system working conditions prior to fabrication. This procedure can facilitate both more efficient and cost-effective research and fabrication, while generating new knowledge on novel low power and high-efficiency electronic components.

This project process can be compiled into a diagram flow, as illustrated in Figure 71, describing the decisions and several steps that need to be taken into consideration to achieve the expected outcomes.

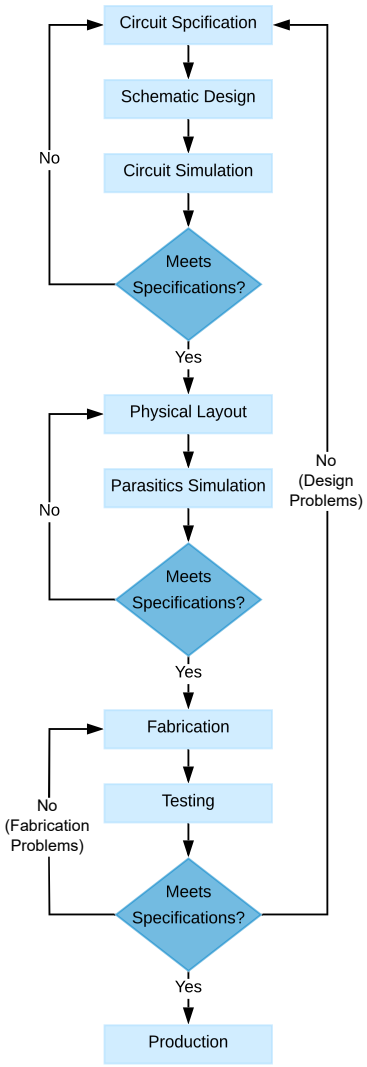


Figure 71: Diagram flow of the CMOS process fabrication.

Firstly, it is imperative to identify the circuit specifications to start with the schematic design and then, the circuit simulations. After obtaining the results from simulations in Cadence EDA, those are analyzed to check if correspond to the specifications. On the contrary case, it is necessary to start again the simulation; otherwise, if the results meets the specifications, the process moves forward to the physical layout.

After the layout design, some simulations considering parasitic analysis are performed to see if they match the specifications. Once again, if they do not meet the specification, then the layout needs to be improved. Instead, the process moves to the next step, the fabrication and testing of the IC. At this point, three conditions are possible to occur. If the testing results are not in accordance to the specification due to the fabrication problem, it is imperative to revise the fabrication parameters. Alternatively, if it is due to issues in the design, the project

needs to move back to the circuit specifications. In the case the measurements results match the specifications, the project can finally advance to the production.

The main project harvesting circuit was split into different sub-circuits, including an operational amplifier, an oscillator, a rectifier, an analog switch and a voltage and current references. In Figure 72 is a representation of those sub-circuits and their interaction on the IC divided into modules. Table 16 complements this figure with a description of the terminals. Nevertheless, in this project, we focus on the design of a low power rectifier, a voltage controllable analog switch and a voltage amplifier, which were completed with success.

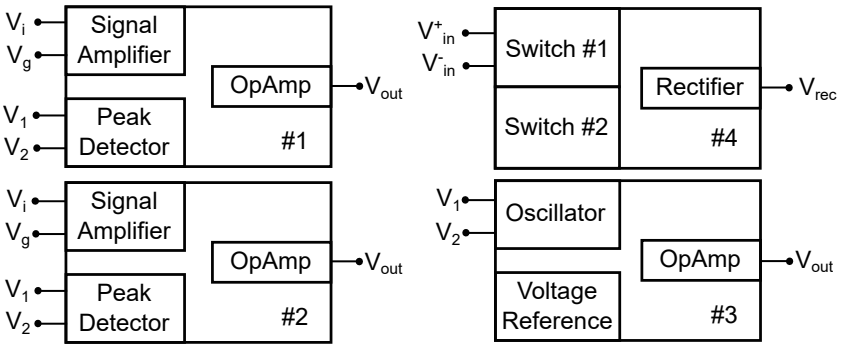


Figure 72: IC block representation.

Table 16: Pins description of the energy harvesting IC system.

Module	Pin Name	Description
#1, #2, #3	V_i	DC signal controlling the duty cycle
	V_g	Amplifier gain control
	V_1	Non-inverting oscillator frequency control
	V_2	Inverting oscillator frequency control
	V_{out}	Output signal
#4	V_{in}^{+}	Non-inverting piezoelectric signal input
	V_{in}^{-}	Inverting piezoelectric signal input
	v_{REC}	Rectified output signal

By splitting the system into submodules, it is easier to determine which issues are not addressed correctly in the analytical and simulation analysis and focus on them individually. The submodules can be tested by simulation and discrete components experiments, helping to reduce any issues found on the system itself. A step by step analysis can be done, pinpointing any point of failures that might exist. If all design work as expected, the circuit can be considered for implementation.

All the circuits accomplished its role and respected its specifications. Since the design is completed, the next step to move forward is the layout. The layout design of the circuit components was realized and the verification tests were performed, namely the Design Rule Check (DRC) and Layout Versus Schematic (LVS). Once no error was found, the implementation continued to the Input and Outputs (IOs) pads placement of final circuit and Electrostatic Discharge (ESD) protection in IOs pads. After the final verification and cross-checking, where no error or any high-risk situation of failure was found, the circuit was prepared for fabrication submission. The fabrication was submitted in SMIC Foundry, which is a major foundry in China. The CMOS fabrication parameters can be consulted in section **??**.

3.4.1 Layout Design

The layout is the final step done before sending the IC to fabrication. A representation of the transistors and other components composing the system are drawn layer by layer in software. Physical verification is done to prove the correct behaviour of the layout. In this stage, check for the manufacturing rules, parasitic extraction, layout versus schematic comparisons and electrical rules need to be considered.

This application requires high efficiency, and consequently, low power. In order to minimize power consumption, techniques can be used during the layout sketch. Passive components, as resistors, have to be carefully designed to reduce heat generation and, where available, replaced by other components.

This section defines the different sub-circuits layouts, mainly the analog switch, the voltage amplifier and the rectifier. Using the rules imposed by the CMOS technology process guidelines provided by the foundry, the layout of all the integrated parts is exhibited in Figure 73. These rules are intrinsic to the device transistors, based on optimal transistor matching and intelligent layout design. More details regarding the physical layout can be seen in section **??**.

Although the chosen technology is very small, over time, CMOS processes tend to be replaced by better processes, which offer smaller dimensions, lower power consumption and, consequently, more efficient performance. Due to this, the design used cannot guarantee full compatibility with the most recent processes. Nevertheless, with small modifications in the original layout, it is easily integrated into diverse systems.

Figure 74 shows the physical layout of the analog switch implemented in section 3.1, with the p and n channels connected in parallel, creating a basic bilateral CMOS switch. Additionally, with an inverter employed by a NOT logic gate and a starved current technique.

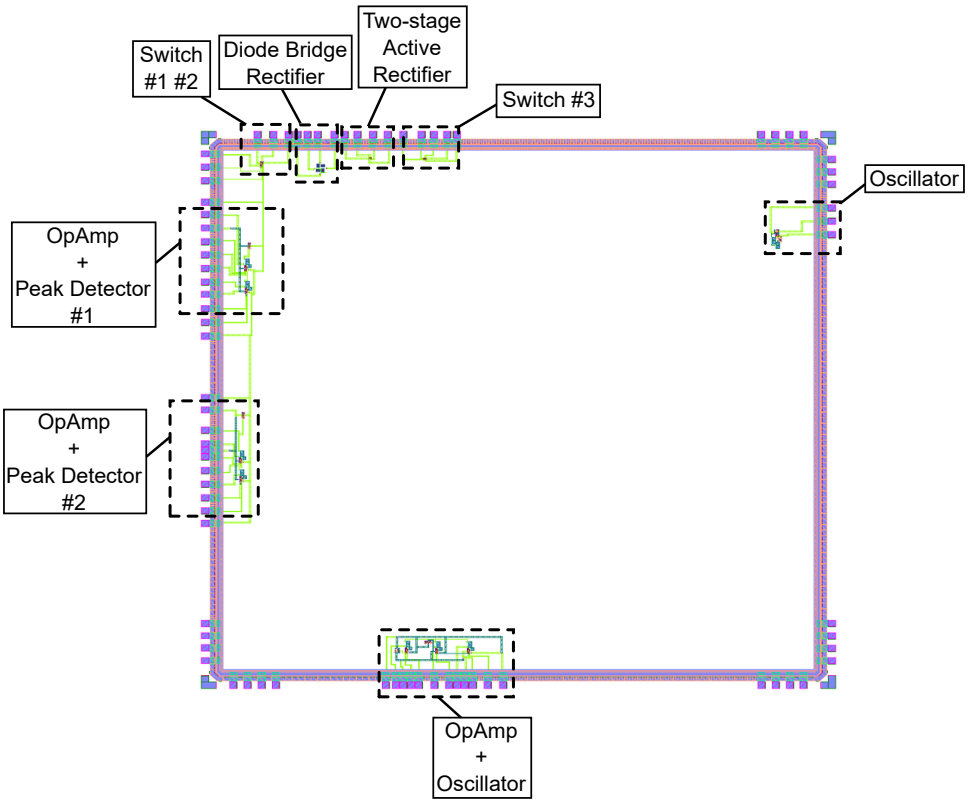


Figure 73: Complete layout of the energy harvesting system with each sub-circuit labeled.

Figure 75 shows the layout design with all the sub-circuits projected in section 3.3 to construct the two-stage active rectifier.

3.4.2 Chip Fabrication

The initial analysis of the die followed the protocol AN10706 from the NXP Semiconductors (POR). The guideline on how to handle bare dies, unlike packaged chips, is rigorous. The dies were delivered in two bare die containing trays, one from each wafer. Special attention has to be taken since the ICs are extremely sensitive to electric fields and over voltages, mechanical damage and surface contamination.

An analysis is made to find any mechanical damages. A glass protection layer protects the circuits against mechanical influences, but the pads and bumps are exposed. Any mechanical forces in the shipping process could bend the die and generate piezo-voltages damaging the circuits or generating cracks and indents. Therefore, it is necessary to use the appropriate tools to handle bare die, avoiding damages.

A class 1000 clean room is used in the process. A random choice of dies was visualized under a microscope, with magnifications from $2.5\times$ to $100\times$. The dies are handled with a vacuum pick up tool, on top of a grounded

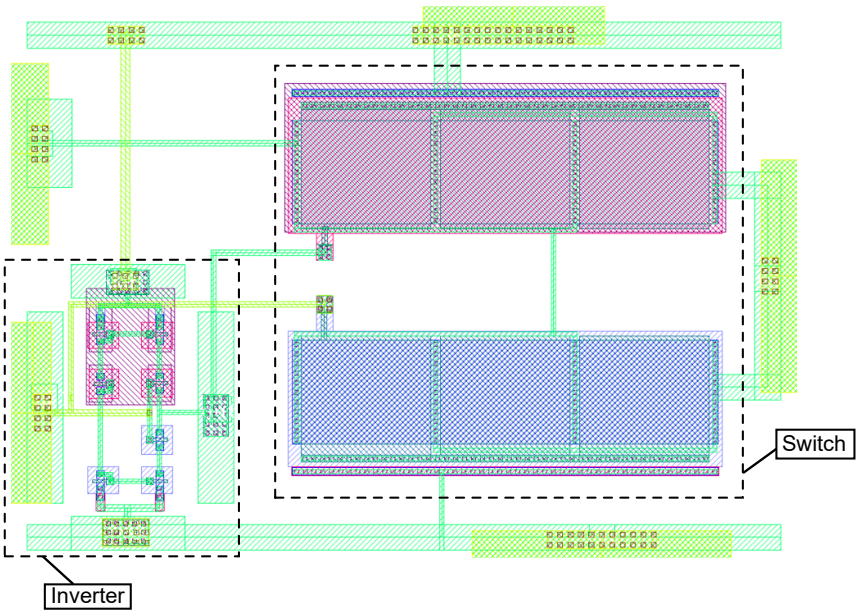


Figure 74: Layout design of the analog circuit, including the inverter and the standard switch.

workbench surface. Afterwards, the dies are stored in a secure and clean area to isolate and protect the products. The storage locker assures temperature between $8\,^{\circ}C$ to $45\,^{\circ}C$, humidity between 25% to 75%, and no exposure to direct sunlight.

The following figures show the die under the microscope split into several regions of interest. Figures 76 and 77 depict a micro-graph view of the proposed two-stage active rectifier and both analog switches, respectively, on a chip.

The dies are wire bounded so the electrical analysis and circuit assembly can be performed.

Table 17, summarizes the fabrication report of the piezoelectric energy harvester power management system on an IC die. The fabrication was a success, with 50 chips already made. Only a few quantities were fabricated to prove the concept behind the design and still be open to improvements. Section **??** gives more details concerning the chip fabrication.

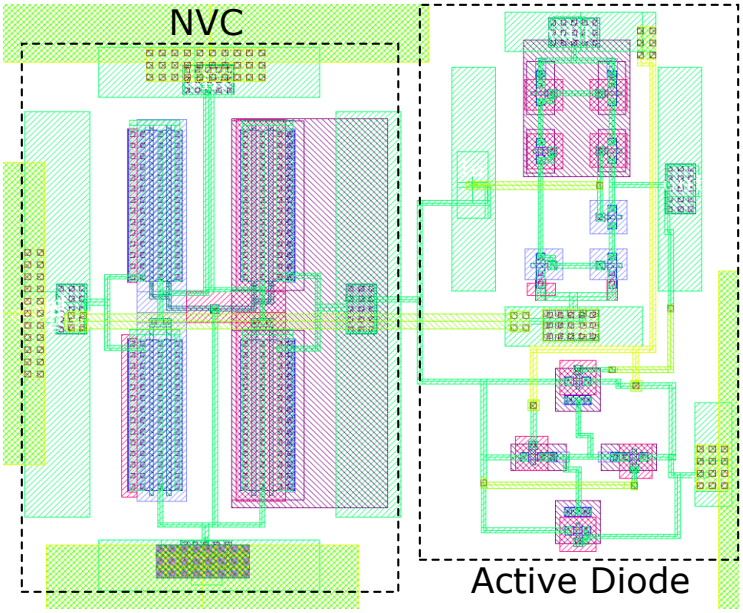


Figure 75: Layout design of the two-stage active rectifier, including the negative voltage converter and the active diode.

Table 17: Integrated circuit die fabrication report.

Technology code	MSGL13GE-B-48-1PAM9C04.1
Technology Limit File	Q5Y0-MA.lim
Wafer quantity	2
Equipment ID	s600q4308
CARD ID	495
Manufacturing date	2020-02-15 18:49:00
Lot ID	DPB813
Die quantity	50 pcs

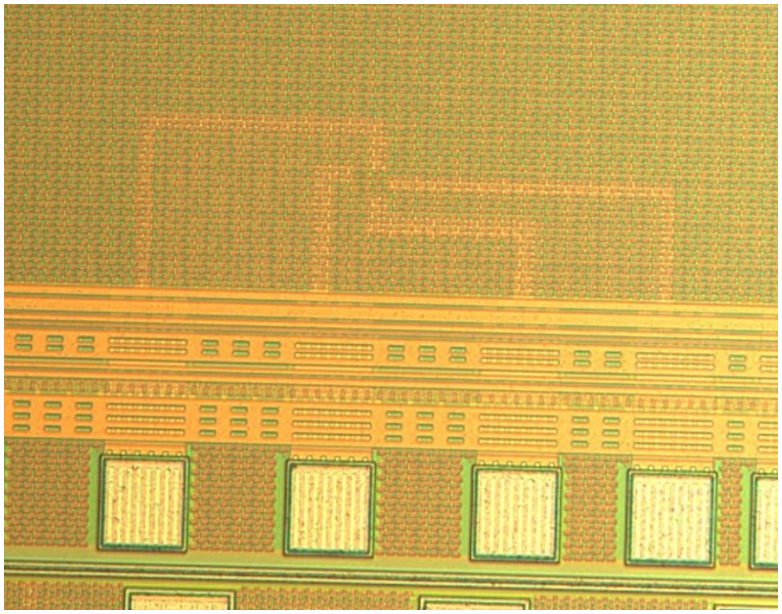


Figure 76: Microscope view, with 50× amplification, of the two-stage active rectifier implemented on the IC chip.

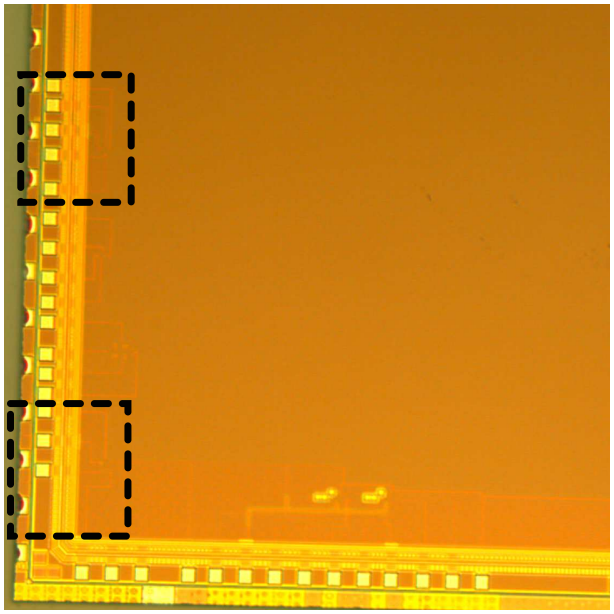


Figure 77: Microscope view, with 25× amplification, of the analog switch on the fabricated chip.

4

CONCLUSION

4.1 Conclusions

The employment of an energy harvester to power a sensor node can make devices self-sufficient, enabling more cost-effective maintenance, and avoiding pollution, resulting in a favourable impact for the environment. This research dissertation contributes to the advance of high efficiency integrated energy extraction circuits.

The main requirements for energy harvesting circuits are efficiency and autonomous operation. The circuit should operate at very low power consumption, as the energy produced by the transducer is already extremely low. As such, the circuit efficiency is of the utmost importance. The harvesting circuit should also operate independently from other devices on the final fabrication, allowing to work without the aid of external source.

A physical layout was developed for fabrication purposes, $0.13\,\mu m$ CMOS technology was chosen with consideration to robustness, cost and performance.

The developed work presents three main contributions. Firstly, the analog switch, based on the up-conversion technique. It was verified to be very useful for applications requiring temperature variation compensation and fast response to the input. The analog switch also has a low ON resistance and very high OFF resistance, providing an appropriated isolation during the nonconducting state. Secondly, the high gain and low power two-stage voltage amplifier was designed, outputting a significantly high voltage signal. Although this circuit is not resistor-less, it has a low power consumption. Lastly, the high efficiency and low power consumption two-stage active rectifier was designed, with ver good performance. By replacing the passive diodes by MOSFETs, the proposed active rectifier minimizes the voltage drop along the conducting path. A two-stage concept which consists of a passive stage with a negative voltage converter, and an active stage containing a NOT gate to drive the active diode switch, was designed. The circuit rectifies the input AC signals in a range between $0.6\,V$ and $4.5\,V$, reaching a maximum

output voltage of $3.45\,V$. The power conversion efficiency is 40.4% and a voltage efficiency of up to 90%. Low power consumption of $17.7\,\mu W$ is achieved by the rectifier, with the comparator consuming $113.9\,nW$.

The proposed design is suitable for the amplification, switching and rectification of low or ultra-low piezoelectric signal. Additionally, the integration of the circuits to CMOS designs should be straightforward, even with already existing designs.

From this study, it is possible to observe a novel method to process an incoming signal from a scavenging energy system, using an analog switch, a voltage amplifier and an active rectifier. It is also possible to conclude that the use of this system to manipulate low power and amplitude signals, such as piezo-element voltages, is manageable. However, a more accurate technique for the voltage amplification must be developed, since the resistors and capacitors can be a problem to achieve even more accurate results.

Extensive research was done in the circuit, focusing on power consumption reduction. The final layout design was conducted to fabrication, which allows for further studies and improvements. Although the system was made having in mind an integrated energy harvesting extraction interface for wireless sensor networks devices, it also has other applications in the industrial, commercial and biomedical sectors.

4.2 Future Work

The results of this study are promising and show the possibility of developing a harvesting interface circuit. In the future, more sub-circuits necessary for the concept will be developed. These components, analogous with the presented in this work, will follow the same baselines, such as low power consumption and high-efficiency structures.

Even though simulation analysis can output very accurate results, to perform a complete circuit analysis, real-world experiments should be done, as the custom IC development is still a costly and time-consuming operation. In order to move forward, it is important to test the fabricated IC. Nevertheless, some unexpected complications happened during the wire bonding prrocess, and as a consequence, the experimental results are not ready yet. Thereby, the future work will focus on the testing of the IC, using the real piezoelectric energy harvester. These experiments will allow for a comparison with the simulation works, showing which parameters can be fully trusted from simulation and the true performance of the circuit.

A system like this will bring several advantages for existing electronic devices, due to its easy integration in other systems. In this way, a step forward is taken for future portable and lightweight devices.

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SUPPORT MATERIAL

A.1 List of Publications

- **Ana C. R. Ferreira (first author)**, Rui Carvalho, Zhaochu Yang, J. H. Correia, Tao Dong. "**A Low-power Two-Stage Active Rectifier for Energy Harvesting Applications**". The 15th Edition of IEEE International Symposium on Medical Measurements and Applications (MeMeA). Virtual. 1 June - 1 July, 2020.

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- **Ana Ferreira (first author)**, Zhaochu Yang, José H. Correia, Tao Dong. "**A CMOS Low-power Two-Stage Active Rectifier for Energy Harvesting Applications**". IEEE Transactions on Power Electronics. Submission: May of 2020.

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