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“A Novel Topology of Multilevel Bidirectional and Symmetrical Split-Pi Converter,”

IEEE International Conference on Compatibility, Power Electronics and Power Engineering, Setubal,
Portugal (virtual conference), 2020.

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A Novel Topology of Multilevel Bidirectional and Symmetrical Split-Pi Converter

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Abstract—The paradigm of smart grids has encouraged new developments of power electronics converters, for instance, in the perspective of renewables and electric mobility applications. Aligned with this perspective, this paper proposes a novel topology of a multilevel bidirectional and symmetrical (MBS) split-pi dc-dc converter. As a central distinguishing feature, it operates with three voltage levels in both dc sides (0, $v_{dc}/2$, v_{dc}), meaning that the voltage stress in each semiconductor is reduced when compared with the conventional split-pi converters, and it operates with controlled variables (voltage and current) based on the interleaved principle of operation, although it is not an interleaved split-pi converter. As demonstrated along the paper, the MBS split-pi converter can be controlled with current or voltage feedback in any of the dc interfaces, while the common dc-link voltage is controlled by the dc interface where the source is connected. The adopted current and voltage control schemes, as well as the pulse-width modulation, are presented and comprehensively explained. The validation is presented for the main operation modes, where it is possible to verify the claimed distinguishing features of the proposed MBS split-pi converter.

Keywords—Split-Pi, Bidirectional Converter, Multilevel converter, Symmetrical Converter, Dc-dc Converter.

I. INTRODUCTION

Nowadays, mainly due to the environmental concerns, the paradigm of smart grids is emerging toward to optimize the energy production and consumption [1–3], as well as to contextualize smart cities within smart grids concerning societal impacts [4]. Accordingly, technologies of power electronics are absolutely indispensable for different sectors [5–7], including future distribution grids [8], renewables [9], power quality issues in hybrid ac/dc microgrids [10], concerns about protection [11], and electric mobility [12–16]. Regarding dc-dc topologies, extensive reviews about the conventional dc-dc converters are offered in [17] and [18], but to control, at the same time, the input current and the output current, the conventional topologies are not properly flexible. The topology of a split-pi converter consists in a bidirectional arrangement of two interconnected dc-dc converters sharing a common dc-link and with two independent dc interfaces, which is used to obtain an output voltage that can be higher, equal, or lower than the input voltage [19]. Usually, the input-side is controlled as

boost-type and the output-side as buck-type. This is valid in both bidirectional modes, where each side can act as a source, as a load, or as a source/load (e.g., batteries). Compared with the conventional dc-dc structures, the split-pi converter offers much more flexibility in terms of operation modes: (a) with controlled input-side current and controlled output-side current; (b) with controlled input-side current and controlled output-side voltage; (c) with only controlled output-side current; (d) with only controlled output-side voltage. An important feature is that these possibilities are valid in both sides, i.e., independently of where the source or the load is located. As main applications, structures of split-pi converters can be used, e.g., in electric mobility applications, motor control drivers, multiphase systems, battery management systems, energy storage systems, regenerative braking, and interface of renewables [20–22].

This paper proposes a novel topology of multilevel bidirectional and symmetrical (MBS) split-pi converter. Similarly to conventional split-pi converters, it permits a flexible operation in terms of controlled input-side current and/or output-side current or voltage, and, compared with advanced split-pi topologies, it permits interleaved characteristics for all the operation modes. Besides, as main differentiating feature and contribution of this paper, the proposed split-pi converter operates with a multilevel feature for all operation modes. When compared with the interleaved split-pi converter, the proposed converter requires exactly the same number of switching devices (i.e., the double when compared with the conventional split-pi converter) and the same number of passive elements, which is also relevant to highlight. Moreover, as the proposed MBS split-pi converter operates with a multilevel feature, it is possible to reduce the requirements of passive filters, even when compared with the interleaved split-pi converter. Summarizing, the main contributions are: (a) a novel split-pi converter that can be controlled by current or voltage in the input-side or output-side; (b) controlled variables in all the operation modes (input-side and output-side) with a ripple frequency that corresponds to the double of the switching frequency (i.e., the same feature of an interleaved split-pi converter, but without requiring more switching devices or passive filters); (c) operation with a multilevel feature in all operation modes according to the

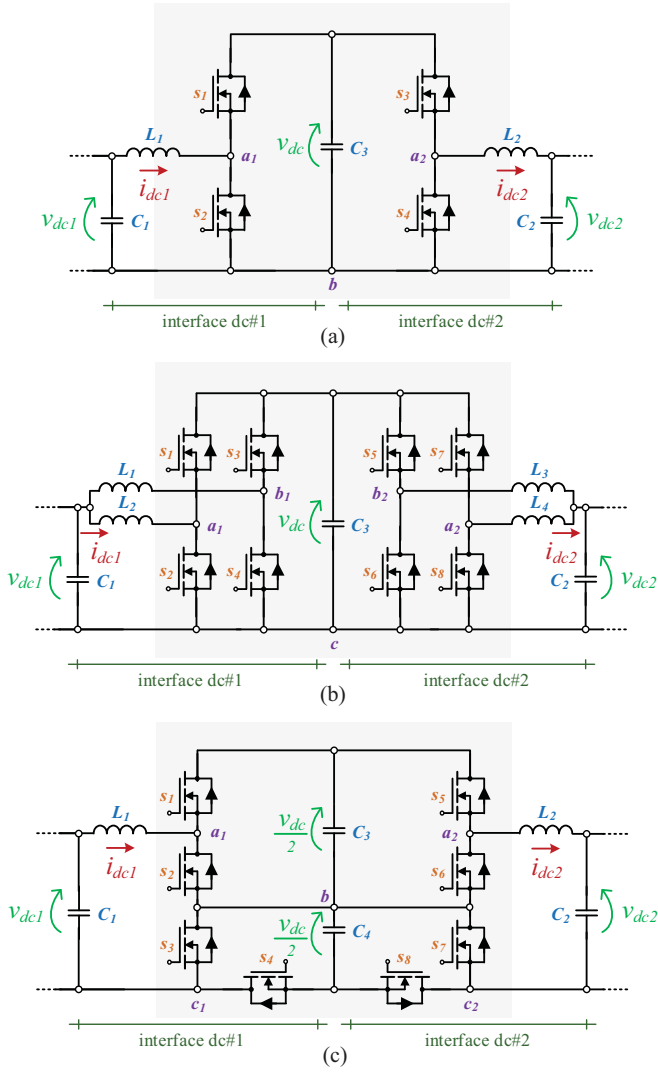


Fig. 1. Split-pi bidirectional topologies: (a) Conventional converter; (b) Interleaved converter; (c) Proposed multilevel and symmetrical converter (MBS split pi converter).

voltages of the input-side, output-side and dc-link, but maintaining the same features of controllability (conventional split-pi converter) and controlled variables with the double of the switching frequency (interleaved split-pi converter); (d) a precise model-based current or voltage control and pulse-width modulation (PWM) for the proposed MBS split-pi converter, guaranteeing all the previous features.

II. PROPOSED MBS SPLIT-PI CONVERTER: PRINCIPLE OF OPERATION

Fig. 1(a) presents the conventional bidirectional split-pi converter, Fig. 1(b) the bidirectional interleaved split-pi converter [23], and Fig. 1(c) the proposed structure of the MBS split-pi converter. A common feature of these three converters is the possibility of operation in bidirectional mode. The proposed split-pi converter is denominated as symmetrical due to the symmetry of the voltages in the switching devices. Regarding the number of switching devices, the proposed structure requires the same number as the interleaved topology. A differentiating aspect is related with the dc-link, since the proposed structure requires a split dc-link to guarantee the

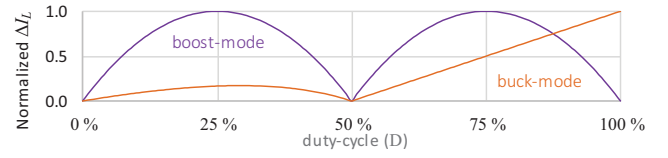


Fig. 2. Normalized current ripple (ΔI_L) as function of the duty-cycle (D) during the operation as buck-type or boost-type.

operation with a multilevel feature. Despite the required number of switching devices (eight), they are not used at the same time, i.e., in the maximum only four switching devices are used in each operation mode. This characteristic is valid for all operating modes. Fig. 2 shows the normalized current ripple (ΔI_L) as function of the duty-cycle (D) during the operation as buck-type or boost-type. When a dc interface is operating as buck-type, the average value of the current in the switching devices (\bar{I}_s) is determined as a function of the duty-cycle. For the switching devices s_1 and s_4 (or s_5 and s_8), the average value is determined as:

$$\bar{I}_{s\{1,4\},\{5,8\}} = D \bar{I}_{L\{1,2\}}, \quad (1)$$

while for the switching devices s_2 and s_3 (or s_6 and s_7) is determined as:

$$\bar{I}_{s\{2,3\},\{6,7\}} = (1 - D) \bar{I}_{L\{1,2\}}. \quad (2)$$

In the contrary, when an interface is operating as boost-type, the mean value of the current in the switching devices s_1 and s_4 (or s_5 and s_8) is determined as:

$$\bar{I}_{s\{1,4\},\{5,8\}} = (1 - D) \bar{I}_{L\{1,2\}}, \quad (3)$$

while for the switching devices s_2 and s_3 (or s_6 and s_7) is determined as:

$$\bar{I}_{s\{2,3\},\{6,7\}} = D \bar{I}_{L\{1,2\}}. \quad (4)$$

Regarding the mean value of the voltages in each switching device (\bar{v}_s), when an interface is operating as buck-type, the mean value of the voltage in the switching devices s_2 and s_3 (or s_6 and s_7) is determined as:

$$\bar{v}_{s\{2,3\},\{6,7\}} = \frac{1}{2} \bar{v}_{dc\{\#1,\#2\}}, \quad (5)$$

while for the switching devices s_1 and s_4 (or s_5 and s_8) is determined as:

$$\bar{v}_{s\{1,4\},\{5,8\}} = \frac{1}{2} \bar{v}_{dc} - \bar{v}_{s\{2,3\},\{6,7\}}. \quad (6)$$

In the contrary, when an interface is operating as boost-type, the mean value of the voltage in the switching devices s_1 and s_4 (or s_5 and s_8) is determined as:

$$\bar{v}_{s\{1,4\},\{5,8\}} = \frac{1}{2} \bar{v}_{dc\{\#1,\#2\}}, \quad (7)$$

while for the switching devices s_2 and s_3 (or s_6 and s_7) is determined as:

$$\bar{v}_{s\{2,3\},\{6,7\}} = \frac{1}{2} \bar{v}_{dc} - \bar{v}_{s\{1,4\},\{5,8\}}. \quad (8)$$

Based on the analysis of equations (1) to (8), it is possible to identify that the operation with duty-cycles near 50%, as well as with similar values of voltages in both interfaces (dc#1 and dc#2), represents the optimal point of operation to distribute the currents and voltages with the objective of optimizing the losses through the switching devices.

III. PROPOSED MBS SPLIT-PI CONVERTER: CONTROL AND MODULATION

By analyzing the MBS split-pi converter, it is possible to verify that each dc interface can be individually controlled.

A. Current Control and Modulation

For simplicity, the following analysis is performed considering the interface dc#1 as the input-side (source) and the interface dc#2 as the output-side (load).

1) Current Control in the Output-Side

Through the analysis of Fig. 1(c), the relation of voltages in the output-side is proven as:

$$v_{L2}(t) + v_{dc\#2}(t) - v_{a2c2}(t) = 0, \quad (9)$$

where the voltage v_{a2c2} is the voltage level of the MBS split-pi converter (between a_2 and c_2), while v_{L2} is the voltage in the inductor L_2 and $v_{dc\#2}$ is the voltage of the interface dc#2. As the voltage in the inductor can be rewritten, yields:

$$\frac{di_{L2}(t)}{dt} + \frac{1}{L_2}v_{dc\#2}(t) - \frac{1}{L_2}v_{a2c2}(t) = 0. \quad (10)$$

For a digital implementation based on the forward Euler method, (10) results in:

$$\frac{(i_{L2}[k+1] - i_{L2}[k])}{T_s} + \frac{1}{L_2}v_{dc\#2}[k] - \frac{1}{L_2}v_{a2c2}[k] = 0. \quad (11)$$

By analyzing (11), it is possible to identify the current in the instant $[k+1]$ is, precisely, the current that must be reached at the end of the control period $[k, k+1]$. Therefore, instead of $i_{L2}[k+1]$, it must be considered the reference of current. Also by analyzing (11), it is possible to identify the voltage $v_{a2c2}[k]$ is, precisely, the reference of voltage that must be produced during the control period $[k, k+1]$. As the objective is to control the current similarly to an interleaved converter, the same reference of voltage is compared with two carriers, with a phase-shift of 180 degrees, but with the same amplitude and frequency. In this case, as it is controlled the output-side, the switching devices s_5 and s_8 are switched, while s_6 and s_7 are turned-off.

2) Current Control in the Input-Side

Quite the opposite of previous case, to control the input-side current, the relation between the voltages is:

$$v_{L1}(t) - v_{dc\#1}(t) + v_{a1c1}(t) = 0, \quad (12)$$

where the voltage in the inductor L_1 can be rewritten, resulting in:

$$\frac{di_{L1}(t)}{dt} - \frac{1}{L_1}v_{dc\#1}(t) + \frac{1}{L_1}v_{a1c1}(t) = 0, \quad (13)$$

and using the Euler method, the digital implementation is:

$$\frac{(i_{L1}[k+1] - i_{L1}[k])}{T_s} - \frac{1}{L_1}v_{dc\#1}[k] + \frac{1}{L_1}v_{a1c1}[k] = 0, \quad (14)$$

also in this case, the reference of voltage ($v_{a1c1}[k]$) is compared with two triangular carriers. In this case, as it is controlled the input-side (i.e., as boost-type), the switching devices s_2 and s_3 are switched, while s_1 and s_4 are turned-off.

B. Voltage Control and Modulation

Also for this situation, the following analysis is performed considering the interface dc#1 as the input-side and the interface dc#2 as the output-side.

1) Voltage Control in the Output-Side

In this case, as the objective is to control the output-side voltage, a relation with the duty-cycle can be considered as:

$$v_{dc\#2} = D \left(\frac{v_{dc}}{2} + \frac{v_{dc}}{2} \right), \quad (15)$$

or considering the relation of voltages:

$$v_{L2}(t) + v_{dc\#2}(t) - v_{a2c2}(t) = 0, \quad (16)$$

and substituting the voltage in the inductor and applying the forward Euler method, the digital implementation results in:

$$\frac{(i_{L2}[k+1] - i_{L2}[k])}{T_s} + \frac{1}{L_2}v_{dc\#2}[k] - \frac{1}{L_2}v_{a2c2}[k] = 0, \quad (17)$$

where the voltage $v_{dc\#2}[k]$ corresponds to the reference of voltage that the converter must control and the voltage $v_{a2c2}[k]$ the voltage that is compared with the two triangular carriers.

2) Dc-Link Voltage Control

The dc-link voltage control is a particular case, which is directly related with the interface side that acts as a source (in this exemplificative case, it is considered the interface dc#1 as a source). The dc-link voltage can be controlled directly through the duty-cycle according to:

$$\left(\frac{v_{dc}}{2} + \frac{v_{dc}}{2} \right) = \frac{v_{dc\#1}}{(1-D)}, \quad (18)$$

or it can be controlled associated with the input current, i.e., the same interface is responsible to control both the input-side current and the dc-link voltage. In this last case, the reference of current is determined by the power necessary to control the dc-link and the power necessary for the output-side, as:

$$i_{L1}^* = \frac{i_{L2} v_{dc\#2} + p_{dc}}{v_{dc\#1}}, \quad (19)$$

where p_{dc} is determined by a proportional-integral controller used to control the dc-link voltage.

IV. PROPOSED MBS SPLIT-PI CONVERTER: VALIDATION OF OPERATION MODES

This section introduces the validation performed in the software PSIM v9.1, according to Table I.

TABLE I. PARAMETERS USED IN THE SIMULATION

MOSFETs	STW45NM50
Switching Frequency	100 kHz
Sampling Frequency	100 kHz
L (input/output)	500 μ H
C (dc-link)	800 μ H
C (input/output)	100 μ H

A. Steady-State Operation with Current Control in Both Sides and Fixed Values of Voltage in Both Sides

The obtained results during this case are presented in Fig. 3. As an illustrative case of operation, the interface dc#1 was considered as a source, while the interface dc#2 was considered as a load. The current in the input-side is controlled for a reference of current of 10 A and the current in the output-side also for 10 A. Fig. 3(a) and Fig. 3(b) show the controlled currents in both sides. This particular case (i.e., both sides with the same value of current) occurs since it was considered the same value of voltage for the input-side (source) and for the output-side (load), namely 150 V. As this value of voltage is

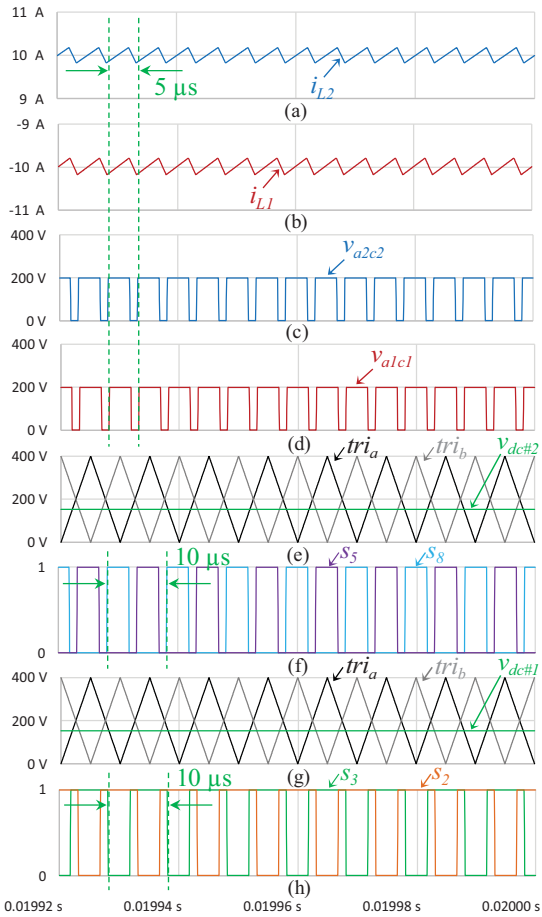


Fig. 3. Steady-state operation with current control in both input and output sides: (a) Current in the output-side; (b) Current in the input-side; (c) Voltage produced by the MBS split-pi for the interface dc#2; (d) Voltage produced by the MBS split-pi for the interface dc#1; (e) Triangular carriers and reference for the output-side; (f) Gate-pulse patterns for the MOSFETs s_5 and s_8 ; (g) triangular carriers and reference for the input-side; (h) Gate-pulse patterns for the MOSFETs s_2 and s_3 .

lower than half of the dc-link voltage (400 V for the total dc-link voltage), the MBS split-pi converter has a voltage (v_{a1c1} and v_{a2c2}) varying between 0 and half of the dc-link voltage ($v_{dc}/2$), a situation that occurs for both sides as shown in Fig. 3(c) and Fig. 3(d). As a main feature, it is possible to verify that the voltage of the converter (v_{a1c1} and v_{a2c2}), as well as the current ripple, has the double of the switching frequency (however, this is not an interleaved split-pi converter as shown in Fig. 1(b)). Regarding the output-side, Fig. 3(e) shows the two carriers (tri_a and tri_b) and the reference value ($v_{dc\#2}$) used to obtain the gate pulse patterns for the MOSFETs s_5 and s_8 , lagged 180 degrees and shown in Fig. 3(f). As the output-side of the converter is operating as buck-type, the gate pulse patterns are never overlapped, i.e., MOSFETs s_5 and s_8 are never turned-on at the same time. On the other hand, regarding the input-side, Fig. 3(g) shows the two carriers (tri_a and tri_b) and the respective reference value ($v_{dc\#1}$) used to obtain the gate pulse patterns for the MOSFETs s_2 and s_3 , also lagged 180 degrees (c.f., Fig. 3(h)). Quite the opposite, as the input-side is operating as boost-type, the gate pulse patterns are overlapped, meaning that during some moments the MOSFETs s_2 and s_3 are turned-on at the same time. As shown, all the MOSFETs are

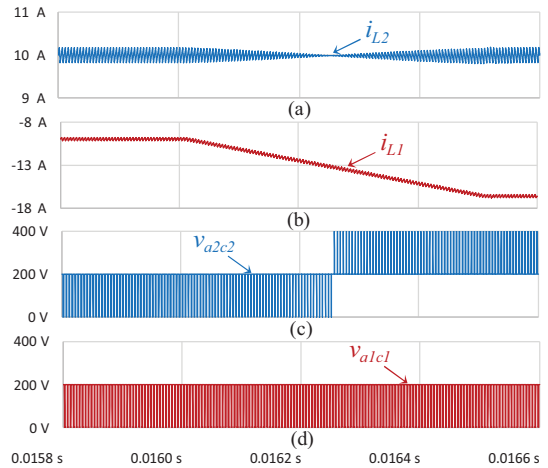


Fig. 4. Transient-state operation with current control in both input and output sides, but with the output-side voltage increasing: (a) Current in the output-side; (b) Current in the input-side; (c) Voltage produced by the MBS split-pi for the interface dc#2; (d) Voltage produced by the MBS split-pi for the interface dc#1.

switched at 100 kHz, but due to the proposed modulation with two carriers, the resultant voltage has the double of the frequency, i.e., 200 kHz.

B. Transient-State Operation with Current Control in Both Sides and Variable Voltage in the Output-Side

In Fig. 4 is shown the validation of the MBS split-pi converter when the output-side voltage increases from a value lower than half of the dc-link voltage to a value higher than half of the dc-link voltage. In this situation, a value of 10 A was fixed for the output-side current, and, as expected, the input-side current will increase to maintain the requirements of the output-side. The input-side voltage was considered as fixed in 150 V, while the output voltage changes from 150 V to 250 V. The dc-link voltage was controlled for a value of 400 V (200 V in each capacitor). As shown in Fig. 4(a), the output-side current is accurately controlled for the reference of 10 A and the input-side current changes from 10 A to 16.7 A (Fig. 4(b)), meaning a power variation from 1500 W to 2500 W. Due to this transient-state, the voltage of the converter (v_{a2c2}) also changes in the output-side. As the input-side voltage is always lower than half of the dc-link voltage (only the current changes), the voltage of the converter (v_{a1c1}) always varies between 0 and half of the dc-link ($v_{dc}/2$). Quite the opposite, as the output-side voltage changes from 150 V to 250 V, the voltage of the converter assumes three distinct values (0, $v_{dc}/2$, and v_{dc}), proving the multilevel feature of the MBS split-pi converter (Fig. 4(c)). During this transient-state, independently of the moment, it always operates with a current ripple with the double of the switching frequency, which is an important feature. As shown in Fig. 4, a particular case occurs when the output-side voltage is equal to half of the dc-link voltage (i.e., 200 V in this case), meaning that the current ripple is cancelled. This situation represents an attractive operation for the MBS split-pi converter, since the input-side can be controlled to regulate the dc-link voltage according to the output-side voltage aiming to minimize the current ripple in the output-side. In other words, the current ripple is minimized when the output-side voltage is close to half of the dc-link voltage.

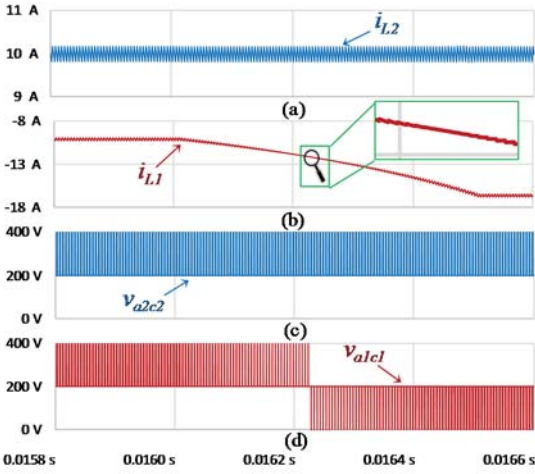


Fig. 5. Transient-state operation with current control in both input and output sides, but with the input-side voltage decreasing: (a) Current in the output-side; (b) Current in the input-side; (c) Voltage produced by the MBS split-pi for the interface dc#2; (d) Voltage produced by the MBS split-pi for the interface dc#1.

C. Transient-State Operation with Current Control in Both Sides and Variable Voltage in the Input-Side

In the sequence of the previous case, a similar case is presented in Fig. 5. However, in this case it is considered the output-side current fixed in a value of 10 A, the output-side voltage fixed in a value of 250 V, and the input-side voltage varying from 250 V to 150 V, forcing to increase the input-side current to maintain the required operation power for the output-side (in this case, a fixed operating power of 2500 W). In this case, the voltage of the converter (v_{a2c2}) always changes between $v_{dc}/2$ and v_{dc} in the output-side, while the voltage (v_{a1c1}) changes between 0, $v_{dc}/2$, and v_{dc} in the input-side, illustrating the multilevel feature of the MBS split-pi converter. Also in this transient-state, it is possible to verify that the current ripple is cancelled when the input-side voltage is equal to half of the dc-link voltage ($v_{dc}/2$), while the other features are maintained in every circumstance.

D. Transient-State Operation with Current Control in Both Sides and with a Sudden Variation of 50% of Power

Fig. 6 shows in detail a transient-state when the input-side voltage has a fixed value of 150 V, the output-side voltage a fixed value of 250 V, and the output-side power is suddenly reduced to half (i.e., from 2500 W to 1250 W), meaning a sudden variation in the output-side current. The variation in the output-side and input-side currents is shown, respectively, in Fig. 6(a) and Fig. 6(b). As shown in Fig. 6(c), even with the sudden variation, the dc-link voltage is controlled for 200 V in each capacitor. Due to the sudden variation of the output-side current, during about 20 μ s, the voltage of the converter (v_{a2c2}) assumes the three voltage levels (0, $v_{dc}/2$, and v_{dc}) in order to guarantee that the current tracks its reference as fast as possible. As this sudden variation is also reflected in the input-side current, the voltage of the converter in this side (v_{a1c1}), also assumes the three voltage levels (0, $v_{dc}/2$, and v_{dc}). When the current reaches its final reference (i.e., when the MBS split-pi converter reaches again the steady-state), the voltage of the converter assumes again the initial voltage levels

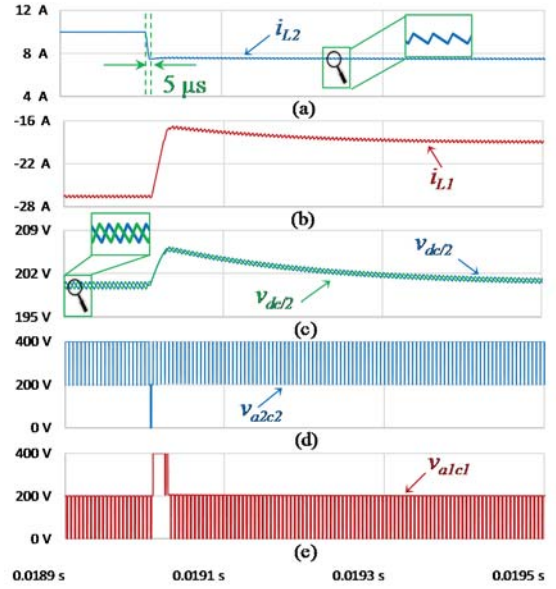


Fig. 6. Transient-state operation with current control in both input and output sides, but with a sudden variation of 50% of power: (a) Current in the output-side; (b) Current in the input-side; (c) Voltages in the dc-link; (d) Voltage produced by the MBS split-pi for the interface dc#2; (e) Voltage produced by the MBS split-pi for the interface dc#1.

(between 0 and $v_{dc}/2$ in the input-side, v_{a1c1} , and between $v_{dc}/2$ and v_{dc} in the output-side, v_{a2c2}).

E. Steady-State Operation with Voltage Control in the Output-Side and with Current Control in the Input-Side

Fig. 7 shows a case when the output-side voltage is controlled for a reference value of 350 V and the current is determined by the characteristics of the load (in this case, it was considered a load of 40 Ω , meaning an operating power of about 3 kW). In this exemplificative case, it was considered a voltage of 150 V for the input-side voltage, meaning that the input-side current is controlled in order to guarantee that the dc-link voltage is properly controlled (as shown in Fig. 7(c)) and the output-side requirements in terms of power are accomplished. Fig. 7(a) and Fig. 7(b) show, respectively, the output-side and input-side currents, Fig. 7(d) and Fig. 7(e) show the voltages of the converter (showing the operation with three voltage levels, 0, $v_{dc}/2$, and v_{dc}), and Fig. 7(f) shows the controlled output-side voltage. As expected, also in this case, the main features of the MBS split-pi converter are maintained (controlled variables with the double of the switching frequency and multilevel voltages).

V. CONCLUSIONS

A novel topology of a multilevel bidirectional and symmetrical (MBS) split-pi dc-dc converter is proposed, e.g., for applications as renewables, electric mobility, and energy storage systems (such as the interface of batteries and ultracapacitors). As main innovative features, it can be highlighted the multilevel voltages and the operation with controlled variables (voltage and current) with double of the switching frequency. These features are presented in detail and supported by an analytic comparison with the conventional bidirectional split-pi converter and with the interleaved split-pi converter. The validation of the MBS split-pi converter was

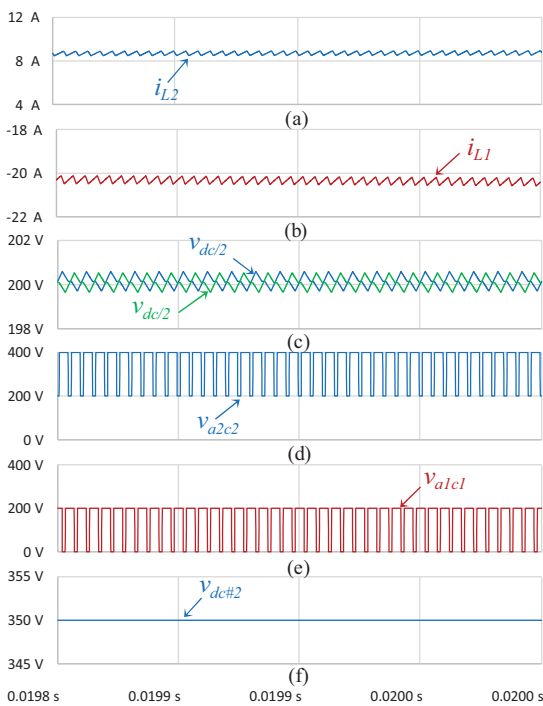


Fig. 7. Steady-state operation with voltage control in the output-side and with current control in the input-side: (a) Current in the output-side; (b) Current in the input-side; (c) Voltages in the dc-link; (d) Voltage produced by the MBS split-pi for the interface dc#2; (e) Voltage produced by the MBS split-pi for the interface dc#1; (f) Voltage in the output-side.

performed considering the operation modes, both in terms of controlled current in both dc interfaces, controlled voltage in the output-side, as well as controlled dc-link voltage. Moreover, the operation in steady-state and transient-state was considered for all the validated operation modes, for an operating power of 3 kW, allowing to validate the proposed pulse-width modulation (PWM) and control algorithms, both for voltage and current feedback. Based on the obtained results, it is possible to verify the claimed advantages of the MBS split-pi converter for all the operation modes considered in this paper.

ACKNOWLEDGMENT

This work has been supported by FCT – Fundação para a Ciência e Tecnologia with-in the Project Scope: UID/CEC/00319/2019. This work has been supported by the FCT Project newERA4GRIDs PTDC/EEI-EEE/30283/2017, and by the FCT Project DAIPESV PTDC/EEI-EEE/30382/2017. Tiago Sousa is supported by the doctoral scholarship SFRH/BD/134353/2017 granted by FCT.

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