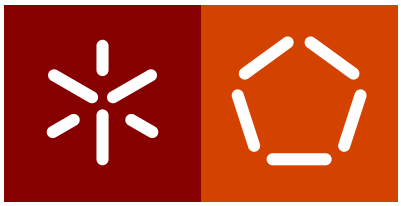


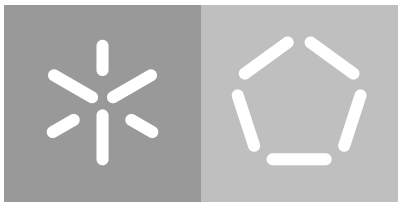
Universidade do Minho
Escola de Engenharia
Departamento de Eletrónica Industrial

Rui Carvalho

CMOS analog/digital circuit components for low power applications

Power management circuit for piezoelectric energy harvester

October 2019



Universidade do Minho
Escola de Engenharia
Departamento de Eletrónica Industrial

Rui Carvalho

CMOS analog/digital circuit components for low power applications

Power management circuit for piezoelectric energy harvester

Master dissertation
Master Degree in Micro and Nanoelectronics

Dissertation supervised by
Tao Dong
Luis Goncalves

October 2019

DIREITOS DE AUTOR E CONDIÇÕES DE UTILIZAÇÃO DO TRABALHO POR TERCEIROS

ACKNOWLEDGEMENTS

My primary appreciation goes to my project supervisor Professor Tao Dong and for all the support and supervision, imperative to the progress of my master's thesis.

Likewise, I have to thank my supervisor at Universidade do Minho, Professor Luís Goncalves. Throughout my academic period, is lectures and relationship with his students, merits distinguishing.

I want to acknowledge the funding support from the National Natural Science Foundation of China (Grant No. 61531008), by the Innovative Research Team of Chongqing (CXTDX201601025).

I am grateful, as well, to Zhaochu Yang from Sensovann AS, which cooperation in the project was essential to its development, the project discussions with him were invaluable. And to Nuno Pires for our useful discussions and always valuable advice.

I am also grateful for the cooperation with the Institute of Applied Micro-Nano Science and Technology, and the Chongqing Key Laboratory of Micro-Nano Systems and Smart Transduction.

I would like to thank all my fellow student colleagues at the University of Southeast Norway for the assistance and support throughout my studies.

Finally, to all my course colleagues and friends at Minho, who together we overcame all steps throught our academic years.

Special thanks, to my parents, I am where I am now for them. Further thanks to all my family.

Thank you. Obrigado!

STATEMENT OF INTEGRITY

I hereby declare having conducted this academic work with integrity. I confirm that I have not used plagiarism or any form of undue use of information or falsification of results along the process leading to its elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

RESUMO

A principal contribuição desta dissertação é a implementação de circuitos integrados de muito baixo consumo e alta eficiência, prontos a ser implementados num circuito de extração de energia com base num elemento piezoelétrico.

Esta tese foca-se no desenvolvimento de um circuito de referência de corrente e um amplificador operacional com baixa exigência de consumo. Uma revisão da literatura é realizada, incluindo introdução à tecnologia *Complementary Metal-Oxide-Semiconductor (CMOS)*, e implementação de conhecidos circuitos de baixo consumo. Várias implementações de referência de tensão e corrente são consideradas, e amplificadores operacionais também.

Uma referência de corrente auto polarizada com extremo baixo consumo é desenvolvida e verificada. Um amplificador operacional original é proposto com uma topologia de seleção de corrente mínima. Este circuito é constituído por três estágios, com um estágio de saída de classe AB, e um circuito translinear. O circuito tem em consideração redução de ruído na sua implementação.

Os circuitos são desenvolvidos com base na tecnologia $0.35\mu m$ CMOS. Uma layout foi também desenhada com o propósito de fabricação. A tecnologia foi escolhida tendo em conta o seu custo versus desempenho.

A referência de corrente produz uma corrente de 12nA, permanecendo estável para tensões de alimentação de variáveis, com uma tensão mínima de 1.6V. O circuito mostra um coeficiente de temperatura satisfatório. O amplificador operacional funciona com tensão de alimentação mínima de 1.5V, com um consumo baixo de 8mW, com uma corrente mínima mantida no estágio de saída.

Palavras Chave: CMOS, baixo consumo, circuito integrado.

ABSTRACT

This dissertation presents a study in the area of mixed analog/digital CMOS power extraction circuits for energy harvester.

The main contribution of this work is the realization of low power consumption and high efficient circuit components employable in a management circuit for piezoelectric-based energy harvester. This thesis focuses on the development of current references and operational amplifiers addressing low power demands. A brief literature review is conducted on the components necessary for the power extraction circuit, including introduction to CMOS technology design and research of known low power circuits. It is presented with multiple implementations for voltage and current references, as well for operational amplifier designs.

A self-biased current reference, capable of driving the remaining harvesting circuit, is designed and verified. A novel operational amplifier is proposed by the use of a minimum current selector circuit topology. It is a three-stage amplifier with an AB class output stage, comprised by a translinear circuit. The circuit is designed, taking into consideration noise reduction. The circuit components are designed based on the $0.35\mu m$ CMOS technology. A physical layout is developed for fabrication purposes. This technology was chosen with consideration of robustness, costliness and performance. The current reference is capable of outputting a stable 12nA current, which may remain stable in a broad range of power supply voltages with a minimum voltage of 1.6V. The operational amplifier operates correctly at voltages as low as 1.5V. The amplifier power consumption is extremely low, around 8mW, with an optimal quiescent current and minimum current preservation in the output stage.

Keywords: CMOS, low power, integrated circuit.

CONTENTS

1 INTRODUCTION 1

2 STATE OF THE ART 5

2.1 CMOS technology 5

2.1.1 Modelling 9

2.2 Current and voltage references 13

2.2.1 Fundamentals 16

2.2.2 Current references 22

2.2.3 Summary 27

2.3 Operational amplifiers 27

2.3.1 One-stage AB amplifiers 28

2.3.2 Two-stage AB amplifiers 31

2.3.3 Summary 48

3 DEVELOPMENT 49

3.1 Self-biased current reference 49

3.1.1 Simulation Results 52

3.1.2 Discussion 54

3.1.3 Summary 58

3.2 Class AB operational amplifier 58

3.2.1 Minimum current selector 59

3.2.2 Proposed amplifier circuit 66

4 CONCLUSION 82

4.1 Conclusions 82

4.2 Prospect for future work 83

A SUPPORT MATERIAL 92

A.1 Technology parameters 92

A.1.1 CMOS AMS 0.35 NMOS 92

A.1.2 CMOS AMS 0.35 NMOS 94

A.1.3 Fabrication parameters extracted 95

A.2 Physical layout 98

A.3 International journal article 106

A.3.1 A low-power CMOS current reference for piezoelectric energy harvester interface 106

LIST OF FIGURES

Figure 1	Power difference between sensor usage and harvester generation.	2
Figure 2	CMOS physical structure. (Sedra and Smith, 2014)	7
Figure 3	CMOS channel. (Sedra and Smith, 2014)	8
Figure 4	NMOS and PMOS layout. (Sedra and Smith, 2014)	9
Figure 5	NMOS typical output (Galup-Montoro et al., 2007b).	10
Figure 6	CMOS threshold voltage based reference (Miller and Moore, 1999).	17
Figure 7	Zener diode based voltage reference.	18
Figure 8	Output current depending on gate voltage of a NMOS $T = 20 - 100°C$	19
Figure 9	Fifteen polysilicon resistors in series.	20
Figure 10	Switched-capacitor as resistor implementation.	21
Figure 11	Classic current reference (Vittoz and Fellrath, 1977).	22
Figure 12	Resistorless CMOS current reference (Enz and Vittoz, 1996).	24
Figure 13	Autonomous CMOS current reference (Oguey and Aebischer, 1997).	25
Figure 14	SCM CMOS current reference (Serra-Graells and Huertas, 2003).	26
Figure 15	Operational amplifier with crossed transistors.	29
Figure 16	Operational amplifier with adaptive biasing.	30
Figure 17	Common source output stage.	32
Figure 18	Ideal transfer characteristic.	32
Figure 19	Floating voltage source.	34
Figure 20	Floating voltage source with transistor and with resistor.	34
Figure 21	Floating voltage source with minimal current.	35
Figure 22	Translinear mesh output stage.	36
Figure 23	Output stage without feedback.	37

Figure 24	Amplifier without feedback.	37
Figure 25	AB output using current mirror.	38
Figure 26	AB amplifier using current mirror.	39
Figure 27	Feedback control in AB output stage.	40
Figure 28	Pseudo source follower.	41
Figure 29	Common mode feedback output stage.	42
Figure 30	Feedback control output stage with folded mesh.	43
Figure 31	Feedback control output stage.	43
Figure 32	Minimum current output stage.	44
Figure 33	AB output stage with inverters.	46
Figure 34	Common source/drain output stage.	47
Figure 35	Self bias current reference.	50
Figure 36	Measured current reference of (35).	51
Figure 37	Proposed nano scale self biased temperature and voltage independent low power current reference.	52
Figure 38	Simulation results depending on source voltage at ambient temperature.	53
Figure 39	Voltage reference results at ambient temperature.	54
Figure 40	Measured current with temperature variation.	55
Figure 41	Voltage reference measurements with temperature variation.	56
Figure 42	Simulation results of the power supply rejection ratio depending on the frequency.	57
Figure 43	Common source output stage.	59
Figure 44	Translinear structure with minimum current.	60
Figure 45	Minimum current circuit.	61
Figure 46	Simulated standard transfer characteristic.	62
Figure 47	Experimental standard transfer characteristic.	63
Figure 48	Modified translinear topology.	64
Figure 49	Simple minimum current output stage simulated current.	65

Figure 50	Modified minimum current output stage simulated current.	66
Figure 51	Principle of the AB class compact amplifier.	67
Figure 52	Amplifier with minimum current class AB control.	69
Figure 53	AC characteristic of AB class *Operational Amplifier (opamp)*. Simulated.	72
Figure 54	DC characteristic of the amplifier.	73
Figure 55	Transient response of circuit.	74
Figure 56	Noise spectral density in V/Hz.	76
Figure 57	Noise spectral density in dB.	76
Figure 58	Circuit used for PSRR simulation.	77
Figure 59	Open loop gain referred to VDD supply.	78
Figure 60	opamp PSRR for VDD supply.	78
Figure 61	Open loop gain for to VSS supply.	79
Figure 62	opamp PSRR for VSS supply.	79
Figure 63	Simulation of the CMRR of class AB opamp.	80
Figure 64	Open loop output impedance.	81
Figure 65	Closed loop output impedance.	81

LIST OF TABLES

Table 1 *Advanced Compact MOSFET (ACM)* equations. 14

Table 2 Proposed Circuit Transistor Size 51

Table 3 Research Comparison 57

Table 4 Aspect ratios and inversion levels of the transistors of the AB amplifier. 71

ACRONYMS

A

ACM Advanced Compact MOSFET.

B

BJT Bipolar Junction Transistor.

C

CMFB Common Mode Feedback.

CMOS Complementary Metal-Oxide-Semiconductor.

D

DC Direct Current.

E

EDA Electronic Design Automation.

G

GBW Gain-Bandwidth Product.

I

IC Integrated Circuit.

M

MCSC Minimum Current Selector Circuit.

MEMS Microelectromechanical Systems.

MOSFET Metal-Oxide-Semiconductor Field-Effect Transistor.

O

OPAMP Operational Amplifier.

OTA Operational Transconductance Amplifier.

P

PSD Power Spectral Density.

PSRR Power Supply Rejection Ratio.

PTAT Proportional To Absolute Temperature.

PVT Process-Voltage-Temperature.

S

SCM Self-Cascode MOSFET.

W

WSN Wireless Sensor Networks.

Z

ZTC Zero Temperature Coefficient.

1

INTRODUCTION

During recent years, more and more low power devices emerge in various applications. Personal devices, e.g. smartphones and wearables, having a big market. Medical and scientific devices, such as medical implants, pacemakers, smart sensors, nanorobotics or *Wireless Sensor Networks (WSN)*, have a great necessity for power reduction. Commonly, on low power sensors, consumption is around $10 - 100\mu W$ depending, obviously, on the kind of application. Personal devices also have an increasing need for reduced consumption, worsen by the utilization growth of smartphones and wearable devices.

The employment of an energy harvester to power a sensor node can make the devices self-sufficient, enabling more cost-effective maintenance. Through a transducer element the energy harvester device generates electric energy from other energy type, such as mechanical, magnetic, thermal and photovoltaic. Vibrational transducers are frequently used in harvester implementations. The main ways to convert vibrational power into electric energy are through piezoelectric, electrostatic and electromagnetic transducers. Piezoelectric crystals create an electric charged when its material is deformed, through vibrating or moving it. A piezoelectric energy harvester can be implemented in several different mediums. A recent one is the integrated *Microelectromechanical Systems (MEMS)* package. This implementation allows the direct integration of the harvesting system with the energy demanding WSN. These harvesters are generally used in applications with vibrating or moving structures, like industrial machines, engines, vehicle wheels, high-buildings, human and animal movement, and so forth. Piezoelectric elements are the most used material, due to it easy integration and high power density generation (Roundy et al. (2005) reports as high as $375nW/cm^3$).

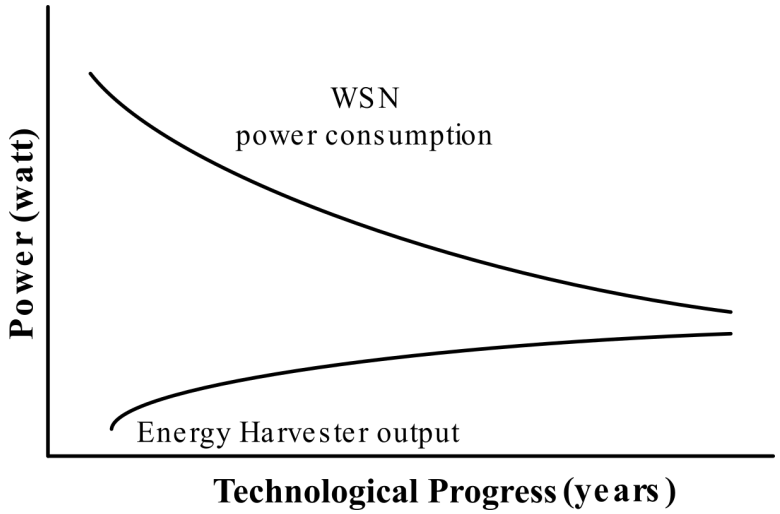


Figure 1: Power difference between sensor usage and harvester generation.

The main problem in the use of these energy sources is the difference between the power generated by them and the power consumed by the WSN. Technology developments have allowed this discrepancy to decrease, Fig. 1, although a breakthrough is needed for an intersection to be achieved. A solution is to increase the power generated by the transducer elements, as this energy is hugely reduced. The energy given by the transducers can be improved by designing the piezoelectric element taking into account the typical vibration frequency of the application. The power output from a piezoelectric material is directly proportional to the vibrating frequency, being the energy produced optimal when the natural frequency of the piezoelectric crystals match the vibrating frequency of the environment. The development of this frequency specific devices is costly and not convenient, as for every different application a new design had to be produced. Thereby the power generated by the energy harvester is mostly enhanced in the power management circuit.

The power management circuit of an energy harvester extract the energy generated by the transducer element, converts it into usable electric energy for the specific application and stores it or relocates it to the requesting devices. Investigation done on extraction circuits for piezoelectric energy harvesters have been exhaustively studied, to increase the efficiency of the extracted energy. The main requirements for the circuits are efficiency and autonomous operation. The circuit should operate at very low power consumption,

as the energy produced by the transducer is already extremely low. As such the circuit energy efficiency is of the utmost importance. The harvesting circuit should also operate independently from the other devices on the final application. This autonomy allows the energy harvester to operate without the aid of external source, ensuring the sensor, or other device, is powered as needed. It is also important the circuit adapts to environment changes in order to maximize efficiency the circuit should attempt to match the excitation frequency of the transducer, and be, as well, prepared for sudden amplitude changes in the oscillation.

For the management circuit implementation, due to its complexity, the best performance can only be achieved by custom *Integrated Circuits (ICs)* compared to the use of discrete components. The custom IC allows for the development of circuit components specific to the needed requirements. Enabling the reduction of power even further. A common technology used for IC implementations is the CMOS process. The CMOS technology has been widely used in monolithic integrated circuit design Roy and Prasad (2009), making it possible to create highly efficient circuits. Further improvements are feasible due to the scalability of the technology Taur (1999) when specific design rules are used. The rules are based on the resolution of the process, the λ parameter, defined by the minimum width of a polysilicon structure. Being a well researched technology, several low power techniques (Kaur and Noor, 2011) can be applied to the circuit. Energy consumption reduction methods, as the decrease of leakage (Roy et al., 2003) and dynamic power (Chandrakasan and Brodersen, 1995), chip capacitance minimization, technology scaling (Davari et al., 1995), use of multiple thresholds (Anis and Elmasry, 2003), have been used and considerably improved. A significant part of these techniques are well researched and used in several existing applications.

The basis for this project is the upconversion power extraction circuit for low frequency energy harvester proposed by Li et al. (2014). The circuit proposed is of very high efficiency for a wide frequency range. The goal of the present work is to design low power circuit components capable of implementing the energy harvester extraction circuit (Li et al., 2014), in an effort to increase the circuit efficiency further.

The energy harvester management circuit requires several building blocks. One main block is the operational amplifier, due to its highly adaptable behaviour. The operational amplifier

can be configured to operate as a signal comparator, a peak detector, a voltage oscillator, and as a signal amplifier, indicated by the name itself. The vast range of applications performed by this device make it especially suitable for signal processing applications.

The present study main goal is to develop and design an operational amplifier, which complies with the requested parameters by the extraction circuit, while remaining very low power. Included in this essay is also the design and simulation of a nano scale current reference. The reference is capable of biasing the remaining building blocks from the main circuit. Exceptionally useful for the correct working behaviour of the operational amplifier circuit.

2

STATE OF THE ART

2.1 CMOS TECHNOLOGY

The CMOS technology is used in the implementation of ICs. It is used for multiple purpose circuits from analog to digital design, suchlike comparators, logic ports, microcontrollers, computing processors, imaging sensors, etc. Nowadays CMOS is the most used technology in IC fabrication. Its main advantages are the very low power consumption, low heat dissipation, high signal to noise ratio and high integration density. As a result of these characteristics, the technology is used frequently in the implementation of low power and high precision devices. CMOS originates from the union of two different *Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET)* types, hence the name complementary, the p and n-type MOS transistors. This combination allowed for a better symmetry in electronic circuits, allowing for a bigger noise reduction and faster signal switching.

The study of analog circuits is widely beneficial for all types of electronic devices, whether digital or analog. Analog techniques, in addition to being the interface of the digital devices to the physical world, also help reduce the consumption and dissipation of power for some applications. This decrease, associated with the search for increasingly higher frequencies of operation, allows the construction of portable equipment, as well as the increase in the scale of integration and speed of processing. Such power limitations and operating frequency reveal the little-remembered face of digital technology, which is nothing more than a particular use of analog circuits.

In this context, integrated circuits are developed for lower supply voltages, 1 to 3V, to maintain reliability for circuits with ever smaller dimensions. At the same time, the operating currents are reduced to the magnitude of 10^{-10} to $10^{-6}A$ per transistor are reduced. At such low current levels, the MOS does not work in the classic region of strong inversion, but in moderate or weak. The description of the transistor behaviour in this regime became essential for the analysis and design of circuits. The initial difficulty is the choice of variables that identify the inverse regime safely. In the conventional strong inversion regime, voltage can be used to determine the functioning of the component. Although, when dealing with values close to the threshold voltage, the use of voltage to describe the component behaviour is no longer recommended. This issue progressed by using the current as the main variable, whether the approach made experimentally or analytically.

In analog circuits, the operational amplifier is one of the most common components. The *Operational Transconductance Amplifier (OTA)* is currently being used as a basic block in the most diverse integrated applications, such as filters to switched capacitors, integrated circuits for medicine, telecommunications, among others.

The MOSFET is the most widely used transistor in the manufacture of ICs. Compared to bipolar junction transistors, for example, the MOSFET is very small in size and has simple manufacturing process (Sedra and Smith, 2014). Therefore, it is possible to place vast numbers of MOSFETs in small areas. Figure 2 shows the details of the physical structure of the MOSFET. The transistor is manufactured on a p-type substrate, which consists of a silicon crystal plate that provides physical support for the device. Two highly doped n-type regions, indicated in the drawing as source n+ and drain n+ (source and drain) are generated on the substrate. A thin layer of silicon dioxide (SiO_2), which serves as an insulator, is placed over the drain, source and substrate areas. A thin layer of metal is deposited on top of the silicon dioxide to form the gate. Metal contacts are placed over the drain and source. This is the structure of the NMOS transistor, where the substrate is p-type. While the drain and source regions are n-type. Reversing the type of these regions, we have the PMOS transistor.

In Figure 3, the drain and source regions are grounded. A positive voltage is applied to the gate. Since the source is grounded, the voltage at the gate is V_{gs}. The positive voltage in

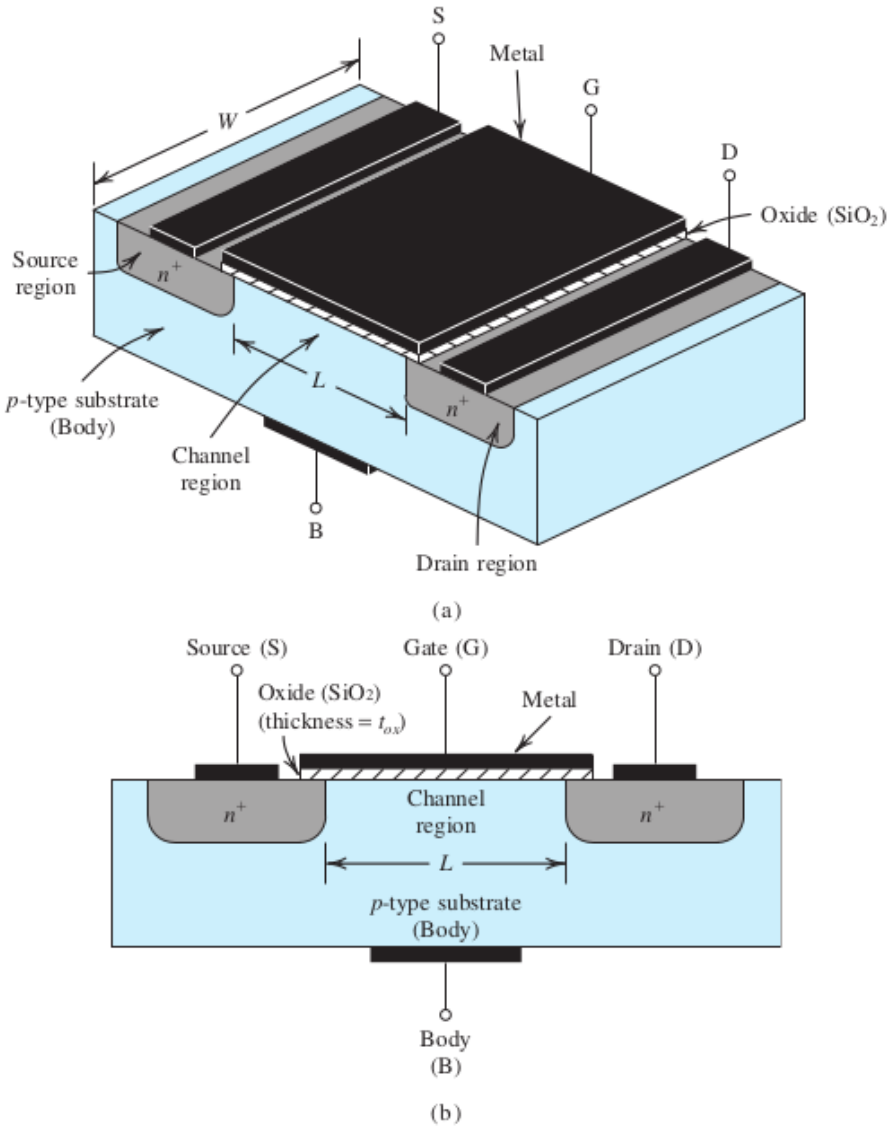


Figure 2: CMOS physical structure. (Sedra and Smith, 2014)

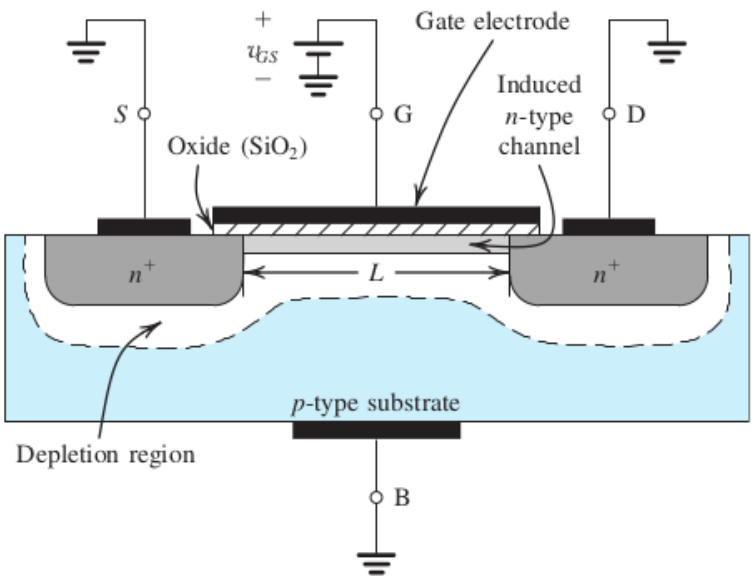


Figure 3: CMOS channel. (Sedra and Smith, 2014)

the gate causes the free holes, i.e. are the positive charges, to be repelled from the region of the substrate under the gate. The holes are pushed down into the substrate, creating a region with a more negative charge, which is called the depletion region. At the same time, the electrons from the drain and source regions are attracted to the substrate region just below the gate area. This movement of charges generates an n-type region under the gate, connecting the drain and source, which are also n-type. An electrical conduction channel is thus formed between the drain and source terminals. In this state, if a potential difference is applied between drain and source, the current will flow between the two terminals.

The region of the gate and the substrate beneath it form a capacitor, with the silicon dioxide in between, serving as a dielectric. The positive voltage in the gate causes an accumulation of positive charge in the gate metal plate, which induces a negative charge in the substrate area. An electric field is then established, whose intensity controls the concentration of the negative charge in the substrate. The negative charge on the substrate is what defines the size of the n-type induced region; consequently, the positive voltage at the gate is determines the size of the induced channel between the drain and the source. MOSFET behaves as a variable resistance controlled by the port voltage. An ideal electronic

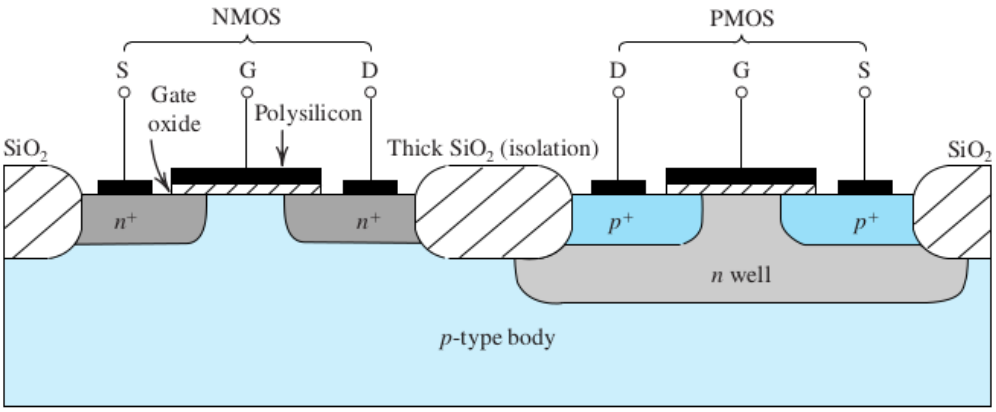


Figure 4: NMOS and PMOS layout. (Sedra and Smith, 2014)

switch has zero resistance when actuated, a infinite resistance when open, and zero response time. The simple MOSFET transistor does not have these characteristics. It has a variable and non-linear resistance. Figure 4 shows the structure of CMOS transistors. The NMOS transistor is manufactured directly on the p-type substrate, while the PMOS transistor needs an n-type region created particularly.

2.1.1 *Modelling*

A theoretical analysis of the upcoming circuits can be fully deduced from the ACM model, in which the expressions are simple, requiring few parameters and valid in any inversion regime.

Initially, the core of the integrated circuits currently developed in MOS technology is the MOSFET, whose ideal physical representation can be seen in Figure 4. The channel is the region located below the gate insulator, between the drain and source diffusion.

Transistor modelling is required for analysis and design. The MOS ACM model is used in this work. It relates the physical and electrical properties of the transistor with unique expressions, simple and continuous, valid in all regions of operation preserving the fundamental properties, such as symmetry between drain and source, and load conservation. The fundamental approximation of the model is the incrementally linear relationship between

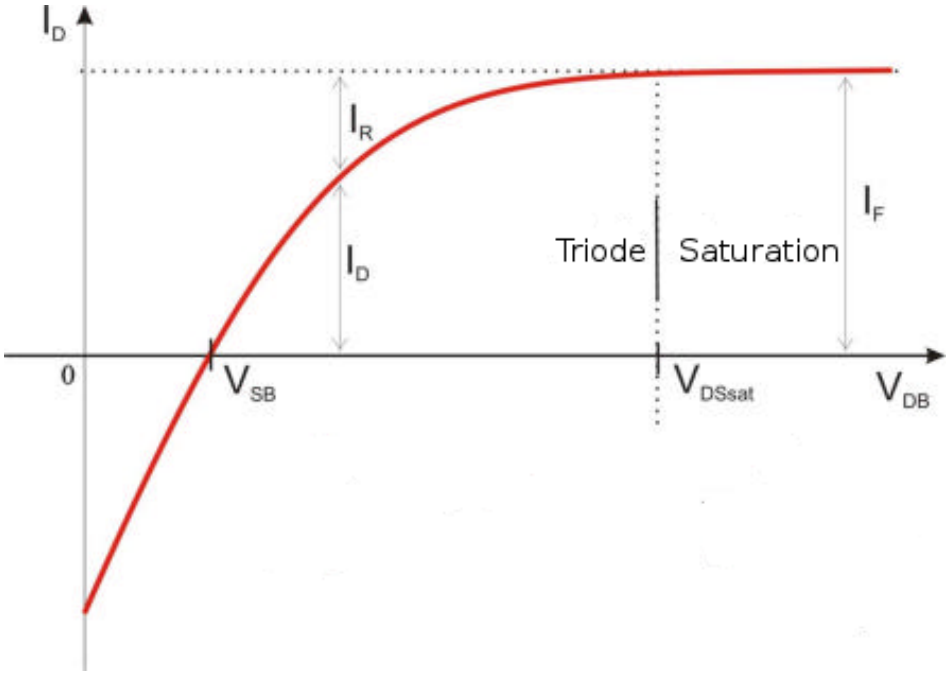


Figure 5: NMOS typical output (Galup-Montoro et al., 2007b).

the density of the inversion load and the surface potential. The MOSFET drain current is expressed as simple functions of two components of the drain current (1), forward current (I_F) and reverse current (I_S).

$$I_D = I_F - I_R \tag{1}$$

The current depends on the gate (V_G) and source voltages (V_S) referred to the substrate terminal. According to equation (1), in the saturation region $I_F \gg I_R$, and the current of can be expressed only in terms of direct current. Thus, the following approach will be adopted in saturation (2).

$$I_D \approx I_F \tag{2}$$

ACM (Oguey and Aebischer, 1997; Galup-Montoro et al., 2007a; Sánchez-Sinencio and Andreou) is a current-based model that uses the inversion level concept to determine the operating region of MOSFET. The drain current can still be written as (3).

$$I_D = I_S \cdot (i_f - i_r) \tag{3}$$

$$I_S = \frac{1}{2}\mu C_{ox} n \frac{W}{L} \phi_t^2 \tag{4}$$

I_S is the normalized current; i_f is the normalized direct saturation current, also known as the inversion coefficient; i_r is the normalized reverse saturation current. The transistor is considered to operate in weak inversion when $i_f < 1$ and in strong inversion when $i_f > 100$. For intermediate values of i_f between 1 and 100, it is assumed that the transistor is in moderate inversion. On the other hand, the current I_S is the fundamental parameter of the ACM model, containing the basic information on technology, temperature and dimensions of the transistor. Here, ϕ_t is the thermal stress; n is the slope factor that can be considered independent of polarization to facilitate approximate calculations; μ is the mobility of carriers, C_{ox} is the oxide capacitance per unit area; W is the width of the channel and L is the length of the channel. Another very useful parameter in the design is the Square Normalization Current, I_{SQ} (5), a technological parameter slightly dependent on V_{GB} through μ and n.

$$I_{SQ} = \frac{1}{2}\mu C_{ox} n \phi_t^2 \tag{5}$$

The relations between the standardised currents and the voltages at the NMOS transistor terminals are given by equations1 (6) and (7).

$$V_{SB} = V_P - \phi_t \left[\sqrt{1 + i_f} - 2 + ln \left(\sqrt{1 + i_f} - 1 \right) \right] \tag{6}$$

$$\frac{V_{DS}}{\phi_t} = \sqrt{1 + i_f} - \sqrt{1 + i_r} + ln \left(\frac{\sqrt{1 + i_f} - 1}{\sqrt{1 + i_r} - 1} \right) \tag{7}$$

$$V_P \approx \frac{V_{GB} - V_{TO}}{n} \tag{8}$$

In equation (8), V_{TO} is the threshold voltage in equilibrium; V_P is the pinch-off voltage and V_{GB} is the voltage between the gate and the substrate. An important concept, the saturation voltage V_{DSsat} defined in equation (9), borders between the triode regions and saturation, from the level of inversion to which the transistor is subjected.

$$V_{DSsat} = \phi_t \left(\sqrt{i_f + 1} + 3 \right) \tag{9}$$

The noise in a MOSFET (Johns and Martin, 2008) device can be represented as a noise current source between the source and the drain. Several physical mechanisms contribute to the noise current. The most relevant for the present work and circuit application are the thermal and flicker noise. The thermal noise is created by the thermal agitation of carriers in the channel. And the flicker noise is the fluctuation of the number of carriers due to the hole traps in the oxide, near the surface of the semiconductor. The *Power Spectral Density (PSD)* of thermal noise (Galup-Montoro et al., 2007b) in long channel MOSFETs is given by equation (10).

$$S_t = \frac{4k_B T \mu}{L^2} C_{ox} n \phi_t \left[\frac{2}{3} \left(\sqrt{1 + i_f} + \sqrt{1 + i_r} - \frac{\sqrt{1 + i_f}\sqrt{1 + i_r}}{\sqrt{1 + i_f} + \sqrt{1 + i_r}} \right) - 1 \right] \tag{10}$$

Where k_B is the Boltzman constant, T is the absolute temperature and $C_{ox} = C'_{ox} WL$. This expression is valid in all regions of transistor operation and at all levels of inversion.

In turn, the power spectral density of flicker noise (Hung et al., 1990) is given by equation (11), where K_F is the technology dependent flicker noise constant.

$$S_t(f) = \frac{N_{ot}}{WLN^{*2}} \frac{1}{f} (i_f - i_r) + ln \left(\frac{1 + i_f}{1 + i_r} \right) \tag{11}$$

$$N^{*2} = \frac{nC'_{ox}\phi_t}{q} \tag{12}$$

$$N_{ot} = \frac{K_F C'_{ox}}{q^2} \tag{13}$$

Table 1 shows the main equations of the ACM model used in this work.

2.2 CURRENT AND VOLTAGE REFERENCES

Current references are the foundations of most mixed-signals electronic circuits. But very few designs provide enough accuracy so as to be used in most modern and delicate systems. In this section, current references technological progress is reviewed, from original to newer, state-of-art, CMOS topologies will be studied and compared. In addition to the background research, additional experimental results are performed for a better understanding of the technology at hand.

CMOS transistors need to be polarized with a known stable operation point. In order to achieve this polarization, voltages and currents are provided through a reference circuit. The references should remain stable and accurate through different variations. They are expected to be independent of the voltage source and to be known, possible to calculate, correlation with temperature changes.

Analog circuits use voltage and current references notably, which are used to polarize a circuit directly or to compare signals with a known value.

Low voltage CMOS circuits can be polarized with current references, in the interest of achieving lower power consumption. The current can be scaled down independently to the voltage source, to achieve the expected power performance. The minimal power consumption will be given by the leakage current in the subthreshold region, and the leakage currents through the PN junctions (between bulk and diffusion regions). These leakages can reach a magnitude from femto to pico Ampere.

New advances on a single chip CMOS technology for accurate operations in the analog and digital domains, request a need for accurate current references. Simply putting, the purpose of a current reference circuit, as the name indicates, is to distribute a current.

Symbol	Equation
I_D	$I_S.(i_f - i_r)$
I_S	$\mu.C'_{ox}.n.\left(\phi_t^2/2\right).W/L$
I_{SQ}	$\mu.C'_{ox}.n.\phi_t^2/2$
$g_{ms(d)}$	$\left(2I_S/\phi_t\right).\left(\sqrt{1+i_{f(r)}}-1\right)$
g_{mg}	$\frac{g_{ms}-g_{md}}{n}$
$V_{SB(DB)}$	$V_P-(+)\phi_t\left[\sqrt{1+i_{f(r)}}-2+\ln\left(\sqrt{1+i_{f(r)}}-1\right)\right]$
V_P	$(-)\frac{V_{GB}-V_{TO}}{n}$
V_{DS}	$(-)\phi_t\left[\sqrt{1+i_f}-\sqrt{1+i_r}+\ln\left(\frac{\sqrt{1+i_f}-1}{\sqrt{1+i_r}-1}\right)\right]$
V_{DSsat}	$(-)\phi_t\left(\sqrt{1+i_f}+3\right)$
Sin_t	$\frac{4.k_B.T.\mu}{L^2}.C_{ox}.n.\phi_t.\left[\frac{2}{3}.\left(\sqrt{1+i_f}+\sqrt{1+i_r}-\frac{\sqrt{1+i_f}.\sqrt{1+i_r}}{\sqrt{1+i_f}+\sqrt{1+i_r}}\right)-1\right]$
$Sin_f(f)$	$\frac{N_{ot}}{W.L.N^{*2}}.\frac{1}{f}.\frac{1}{(i_f-i_r)}\ln\left[\frac{1+i_f}{1+i_r}\right]$
f_C	$\frac{\pi.N_{ot}}{2.N^{*2}}.f_T$
f_T	$\frac{\mu.\phi_t}{\pi.L^2}.\left(\sqrt{1+i_f}-1\right)$

Table 1: ACM equations.

Circuits can quickly achieve this simple task with no more than a couple of transistors. Although, in this project, low power and high efficiency are key features. Moreover, as such, the objective for this circuit cell is to design an high accuracy, while still low power, current reference.

Several different electronic circuits use the current reference, as operational amplifiers, phase locked loops, analog to digital converters, and other high-performance analog circuits — these circuit base themselves in the reference cell, to be able to maintain stable and accurate outputs. The reference is also used as a fixed point for comparing and sampling purposes, and this point should settle even in an ample range of *Process-Voltage-Temperature (PVT)* variations.

A central problem has been on focus in several types of research, the temperature variation impact on the expected output from these circuits. Consequently, novel references have been designed to compensate temperature variations, as well as different power supply voltages. State-of-art structures have achieved output variations lower than 1% even for temperature differences of 100°C. Another effort in the improvement of such devices are voltage supply variations. A well-researched method is the self-biasing, which generates a reference voltage autonomous from the power supply.

However, in the search for higher precision accuracy, other problems, such as the precision of similar devices due to fabrication processes. In CMOS technology, several parameters, as the stability, performance and reliability, from a transistor are altered explicitly by PVT conditions. The following research attempts to deal with these problems and further ones which might emerge. The goal is to develop a current reference circuit with highly accurate under different PVT conditions.

2.2.1 *Fundamentals*

Voltage References

The voltage reference circuit is used to generate a current reference with low sensitivity to PVT variations. To design a satisfying voltage reference, the scope of attributes have to be checked. The reference, as expected, should maintain a consistent voltage output when submitted to different conditions; such as supply voltage changes, temperature variations, and process discrepancies. It is expected that two similar devices which are fabricated with the same process, should have equal or roughly equal voltage output, when submitted to different conditions.

Several topologies to design voltage reference have been developed through various different methods. With CMOS technology a convenient method to develop a voltage reference is to use the intrinsic threshold voltage. In case a more accurate voltage is needed, the inherent Zener diodes generated by p-n junctions can be used. Another useful technique is to acquire the bandgap voltage of silicon extracted from bipolar transistors, due to fabrication processes limitations this method is not always available.

A reference can be generated from a threshold voltage. The threshold voltage (V_{th}) can expressed by (14).

$$V_{th} = V_t \cdot \alpha T \tag{14}$$

In the expression V_t is the threshold voltage when the transistor is at absolute zero temperature, with α being the temperature factor established by the CMOS circuit. The temperature factor is usually kept through a different device when the same fabrication technology is used. Besides, due to fabrication discrepancies, the zero temperature threshold voltage (V_t) is expected to change. If the technology allows for the generation of more

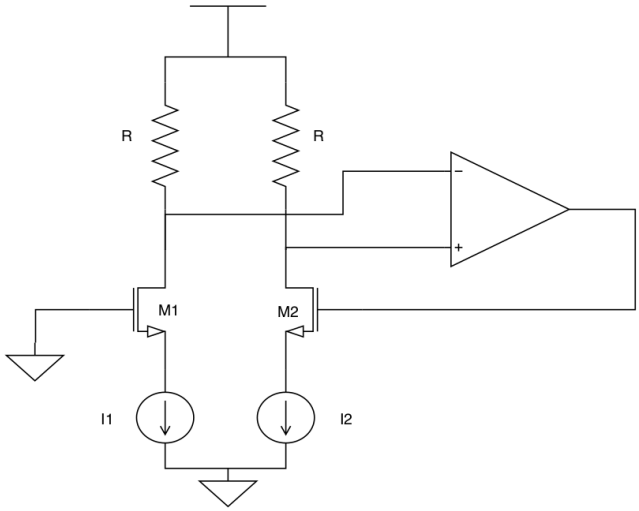


Figure 6: CMOS threshold voltage based reference (Miller and Moore, 1999).

than one threshold voltage in the same device, a PVT independent constant voltage can be implemented by subtraction of two of the these mirrored values.

$$V_{gs} = \sqrt{\frac{I_{ds}}{k}} + V_{th} \tag{15}$$

Assumed that I_{ds} and K of two transistors are the same, subtract the gate voltage between the two transistors, and yield a voltage equal to the difference of their threshold voltages (16), as depicted in Figure 6

$$V_{gs2} - V_{gs1} = V_{th2} - V_{th1} \tag{16}$$

In the circuit, the value of the transistor with the lower threshold voltage is subtracted from the other one. The output of the operational amplifier is used as the feedback, and the circuit will keep the inputs to the opamp equal. Consequently, the current in the two transistors will be the same, if the resistors are equivalent. This means the opamp will actively attempt to establish V_{gs2} to keep the equivalent current in both nodes. The resulting voltage is strictly the difference between threshold voltages, with any variation auto-corrected.

Another fundamental voltage reference is generated by the breakdown voltage of a Zener diode (Teichmann et al., 2003). In CMOS processes a Zener diode can easily be formed by

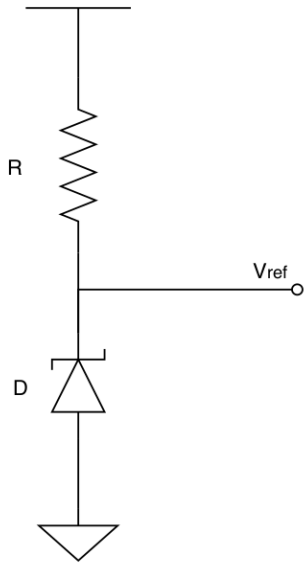


Figure 7: Zener diode based voltage reference.

a p-n junction. To extract the breakdown voltage of the diode, a trivial circuit is shown in Figure 7. The reverse breakdown voltage is highly accurate and reasonably insensitive to power supply voltage changes, although it has evident abrupt changes with temperature variations. Additionally, the diode incites the noise due to the use of its breakdown voltage, which may have very high fluctuation. This can be improved by burying the diode in a deeper substrate from the surface. Nevertheless, the generated voltage is mostly unusable in ultra-low voltage devices, due to the noise factors still existed even in buried Zener diodes, and its moderately high breakdown voltage. If the case is to develop of an external voltage reference for fixed comparison of processed signals, the Zener references will be a great choice.

In CMOS devices, it is possible to find a voltage capable of offsetting the temperature variation when applied to the gate of the transistor, the *Zero Temperature Coefficient (ZTC)* as shown in Fig. 8. This is a consequence of the temperature dependence of the threshold voltage and the electron mobility of the device. An output current constant through temperature variations is possible in n-type MOSFETs when the transistors are sized correctly and with a precisely chosen doping.

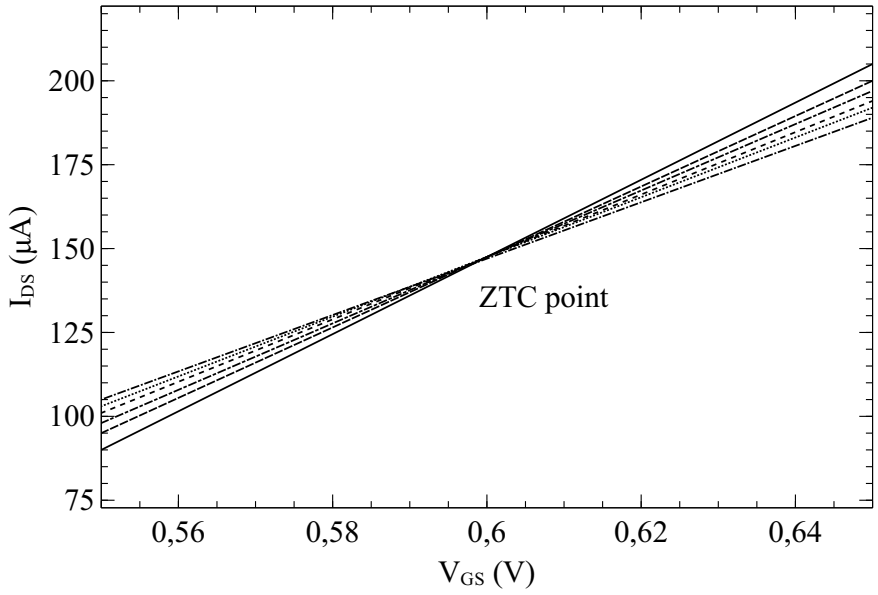


Figure 8: Output current depending on gate voltage of a NMOS $T = 20 - 100°C$

As Fig. 8 shows that there is a point which is independent of the temperature variation; the voltage is given in the gate of the MOSFET always results in the same output current (I_{DS}). The ZTC point was found at 0.6V by parametric simulations. This is a consequence of the temperature dependence both these values have, which eventually cancel one another.

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{17}$$

Analytically, the result is proven in the drain current (I_D) expression (17). Accurate detection shows the threshold voltage and the electron mobility as the main variables depending on temperature. The parameters are both inversely proportional to the temperature. However in equation (17) only threshold voltage is inverted to the drain current. Meaning the two parameters have contrary effects on the current result. This is what makes the ZTC point possible, where the threshold voltage and the electron mobility fully compensate each other. The resulting current in the saturation region is approximately independent of the temperature.

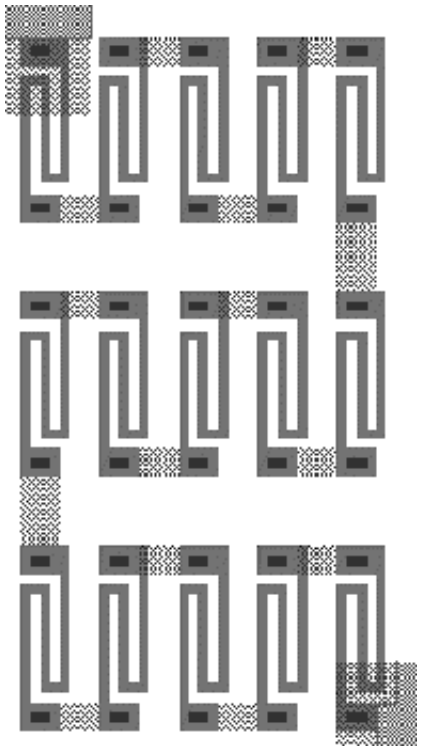


Figure 9: Fifteen polysilicon resistors in series.

CMOS resistors

Most of the topologies for reference circuits employ resistors to generate a current, especially when directly converting from a base voltage reference. The use of these components in CMOS IC design should be avoided due to several problems which arise from their implementation.

To design a resistor in the CMOS process, some different solutions are possible. A transistor can directly be used as a replacement, as long as it is working in the linear region, the so-called ohmic region. In this region the MOSFET works as a variable resistor. However, it is not the perfect solution, as the resistance value is dependent on the input voltage with very bad linearity.

Another solution is to truly implement a physical resistor, which is possible when only a fixed resistance value is needed. Such implementation in CMOS technology is a problem, as it requires a large area when small currents are requested. For rough example, if there

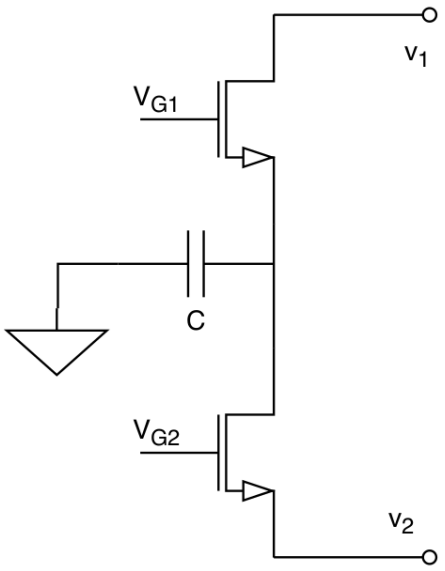


Figure 10: Switched-capacitor as resistor implementation.

is the need for a current of 100nA, even with an arbitrary low voltage as 1.25V, it still requires a resistance of $12.5M\Omega$; a resistor with such a value will occupy a vast space in the glsic, especially when compared to the remaining circuit. Moreover, this is not the only problem appearing from the CMOS resistor implementation; the components have a very high tolerance, which change from fabrication to fabrication, and is non-linear.

In CMOS processes typically, there is not a dedicated method for resistor fabrication. Alternatively, the regular layers used for vias and CMOS devices are used for the resistors. The resistor value is influenced by the material used in its implementation, e.g. aluminium or polysilicon. For example, to create a resistor by using positive N doped polysilicon, the sheet resistance is used to calculate the layer area. In a standard $0.35\mu m$ CMOS process, the sheet resistance is of $290\Omega/\mu m$. Thus to implement the desired resistance of $12.5M\Omega$, the calculated polysilicon area is approximately $43000\mu m$. This material, as mentioned before, presents terrible temperature dependence, with its coefficient around 1350 ppm/°C. A quick analysis of the temperature dependence shows a 7% variation in the resistance value within 100°C range.

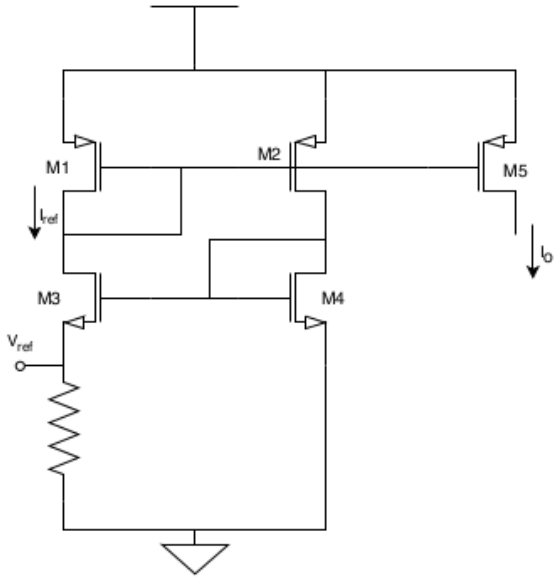


Figure 11: Classic current reference (Vittoz and Fellrath, 1977).

A more advanced solution for large resistances is the switched-capacitor method. In this method, the physical implementation is replaced by the charge and discharge of a capacitor. Figure 10 mimics a conventional resistor. The resistor value is controlled by changing the input signal in V_{G1} and V_{G2}. The capacitor factor is easily regulated, generating a very stable output current. Despite the fact this implementation being the most beneficial, it is necessary to consider the mandatory extra signal and parameters to control the circuit, like the need for an external clock.

2.2.2 *Current references*

Low variation current references are usually derived from voltage references with a voltage to current converter. These implementations in CMOS are rarely transistor only, especially with low power conditions.

A initial current reference is presented, the design is exceptionally elementary, which is composed exclusively of four transistors and a resistor, as shown in Figure 11.

A current mirror is created by the PMOS transistors, consequently forming an equal current in both the NMOS transistors. A voltage reference is created by the NMOS pair, with the proportionality of K, in which the voltage is *Proportional To Absolute Temperature (PTAT)*. It is then applied to a resistor, generating a usable current. Assuming M1 and M2 to be in the weak inversion region, the output current can be calculated by the expression (18). The current (18) is affected by the temperature dependence of a CMOS device, which is expressed by ϕ_t in equation (19), where k is the Boltzmann constant, N_A the specificated doping parameter and N_i the substrate instrinsic doping parameter.

$$I_o = \frac{\phi_t ln(K)}{R} \tag{18}$$

$$\phi_t = \frac{kT}{q} ln\left(\frac{N_A}{N_i}\right) \tag{19}$$

This introductory topology represents a minimum efficiency of 33%, to generate an output current, I_o, similar to the reference current, I_r. The efficiency can be visualized by examining the circuit, that the intrinsic current consumption is two times the one in the output. Although this circuit can be successfully used in low voltage application for particular cases, it is unacceptable in the generation of low polarization currents for low power consumption circuits.

Another problem to use the resistor to convert the voltage reference to current, may bring multiple issues. For example: assume room temperature, T=300K, and an arbitrary proportionality factor, K=10, the reference voltage generated is 60mV. In order to achieve an output current of 6nA, there is a need for a 10 $M\Omega$ resistor. To implement this electrical resistance in CMOS, a substantially higher silicon area is required compared to the remaining circuit. It should also be noted that the electrical resistance in a CMOS implemented resistor is hugely inaccurate, with tolerance discrepancies in fabrication ranging from 10% to 30%.

New research has been done to design CMOS references based exclusively on intrinsic physical properties without being dependent on the threshold voltage. These circuits are solely formed by transistors, yet displaying a temperature dependence, T^{2-m}, in which m

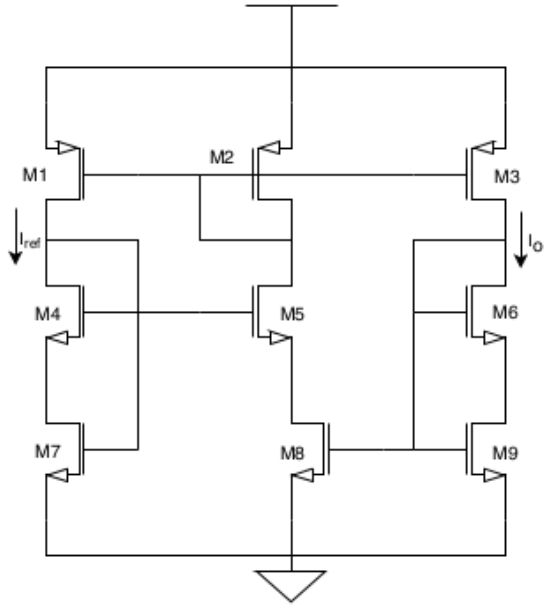


Figure 12: Resistorless CMOS current reference (Enz and Vittoz, 1996).

is the temperature mobility coefficient. Depending on the used technology, employed this value may vary from 1 to 2. The acceptable temperature independence is achieved when m is around 2.

The first example of this kind of current references is in Figure 12. The working principal of this current reference lies in the comparison of the voltage created in the cascoding node of the NMOS transistors, polarized respectively in weak inversion and strong inversion region. Consequently, a current proportional to I_S is generated. Although, this circuit is based on the earlier circuit 11, this topology still present a low efficiency in terms of power consumption. The culprit, in its low efficiency, is the use of very large mirroring factors performed by the PMOS transistors standard current mirrors.

The example circuit 12 generates a current equal to I_{ref}. If this is the requested output, the current reference by itself, will consume 111 times more than I_{ref}. It is simple to find the terrible efficiency, calculated to be 0.9%.

The second autonomous current reference is presented in [06], which was also inspired by the classic structure of 11. As mentioned previously, the resistor can be a disadvantage in

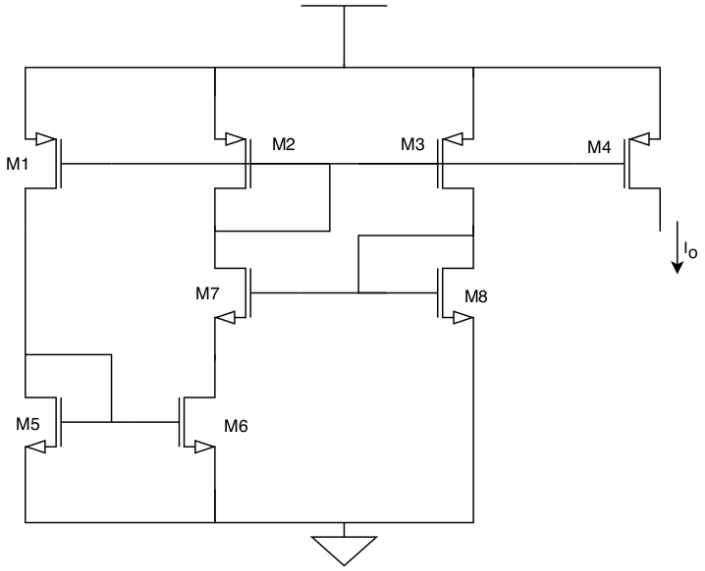


Figure 13: Autonomous CMOS current reference (Oguey and Aebischer, 1997).

many applications. Therefore, Oguey and Aebischer (1997) use a MOSFET operating in the strong inversion triode region to replace it, as illustrated in Figure 13.

Although it is designed in a simple structure (Serra-Graells and Huertas, 2003), it is not suitable for applications with very low operating voltage. The experimental results show the current regulation of 20% /V and dispersion from the nominal value up to 90%. Besides, the dominant number of transistors working in the strong inversion regime reduces the chances of being a candidate for low operating voltage. An analysis using a non-compact model was performed. The results show that the equation does not restrict undesirable operation points ($I_{ref} = 0$).

With arbitrary values for the attributes of Figure 13, let $N = 1$ and $K_2 = 1$, the equation from Oguey and Aebischer (1997) provides for a finite current value other than zero. However, in practice under these conditions, there is no such point of operation, because the transistor M5 would tend to saturate to reach the reference current. As its output voltage is restricted by V_{ref}, then the current begins to reduce until M5 and M6 enter the inversion region where it arrives at zero exponentially. Equations for this circuit with a compact model

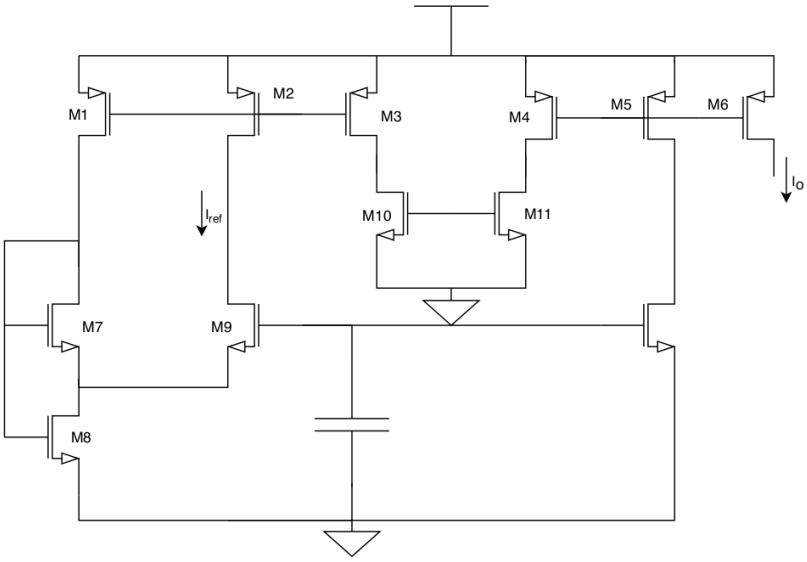


Figure 14: SCM CMOS current reference (Serra-Graells and Huertas, 2003).

for MOSFETs (e.g. ACM), restrict $N \cdot K_2 \geq 4$ so that M5 can work in the triode region in strong inversion.

A third autonomous current reference is introduced by Serra-Graells and Huertas (2003), which is more complex structure as shown in Fig. 14. This circuit uses a *Self-Cascode MOSFET (SCM)* polarized in strong inversion, with a PTAT voltage reference generated employing a current relation. It also employs local feedback to balance the structure and improve the rejection of the power supply. Although it is suitable for low operating voltage, its power efficiency is not very high, due to the relatively large current factors and some transistors operating in the strong inversion.

In the design proposed by Serra-Graells and Huertas (2003), the efficiency of the primary component to produce an output current equal to the lowest reference current is 5%. Additionally, in some cases a compensation capacitor must be included to ensure the stability, which generates an additional increase in the area of silicon. Finally, as proposed by Sansen et al. (1988) and Lee and Park (1996), the circuits are not the most suitable for low operating voltage. In these circuits, the MOSFET polarization is dominant in the strong inversion region, and up to three source-gate voltages (V_{GS}) are stacked.

2.2.3 *Summary*

With regard to the relevant architectures and compensation techniques available form the literature, it can be noticed that every circuit regarding temperature independence relies on one of the following techniques. It is either the sum of two opposed temperature dependent currents. The other technique is to bias the MOS device at a specific voltage, in which its internal parameters automatically cancel each other out, the ZTC point. Although, sometimes such bias point is difficult or even impossible to find.

Supply independence can be achieved mostly by two ways. The first is using the traditional bandgap reference. The voltage reference is achieved by extracting the bandgap silicon voltage, this value is independent of the supply itself seeing it is a physical constant of the silicon itself. The other solution is the use of cascode structures to increase the *Power Supply Rejection Ratio (PSRR)*.

Process compensation is more difficult to achieve. The techniques are usually based on optimal transistor matching and intelligent layout design. Prioritizing circuit symmetry seems the best alternative.

2.3 OPERATIONAL AMPLIFIERS

There are several classes of amplifiers. For class A amplifiers, the maximum output current is equal to the quiescent current and with a maximum efficiency of 25%. The class B amplifiers join high output current with almost zero quiescent current, which has a maximum efficiency at 75%, but crossover distortion is present. A suitable output stage is the common AB-class push-pull source that provides a good compromise between distortion and quiescent dissipation, with intermediate results between class A and class B. The output transistors are polarized with a small quiescent current, which reduces crossover distortion compared to class B. The maximum output current is much higher than its quiescent current, which

improves its efficiency compared to class A. There are other classes of amplifiers, for example, class D, which are more complex than the AB class.

As already mentioned, the opamp is fundamental in the implementation of analog circuits. The frequency response is affected by the *Gain-Bandwidth Product (GBW)* and by the capacitive effects of opamp input and output. The opamp offset generates a *Direct Current (DC)* displacement in the output current. The noise of the opamp is enough to propagate to other components. Thus, the need for a properly designed operational amplifier is evident.

2.3.1 *One-stage AB amplifiers*

Crossed transistors

Typical class AB amplifier, with crossed transistors [15-17] is shown in Figure 15, with crossing differential pair transistors. The maximum output current is not limited by the polarization current source. If bigger aspect ratios are chosen for M1 and M2, higher output currents can be achieved. The transistors M1 and M2 form the basic transconductance stage with AB class input. When $Vin1$ is larger than $Vin2$, M1 conducts, while M2 tends to cut rapidly, bringing the current $I1$ to zero. The increase of $I1$ does not depend on the quiescent current I, and $I1$ maximum current is much higher than I. In the positive cycle, $Vin1$ is greater than $Vin2$ and $I_o = I1$. In the negative cycle, $Vin1$ is smaller than $Vin2$ and $I_o = -I2$. The M1 and M2 transistors conduct only a little more than half of each cycle, which is the characteristic of AB class operation. This structure is not suitable for applications with low supply voltage, since it requires at least $2VGS + 2V_{DSsat}$ for the supply.

Adaptive biasing

Another amplification technique with AB class control at the differential input stage is known as adaptive biasing [12-14]. Callewaert et al. [12], uses positive feedback to implement the AB class operation. Therefore, extra attention has to be paid during the design to avoid

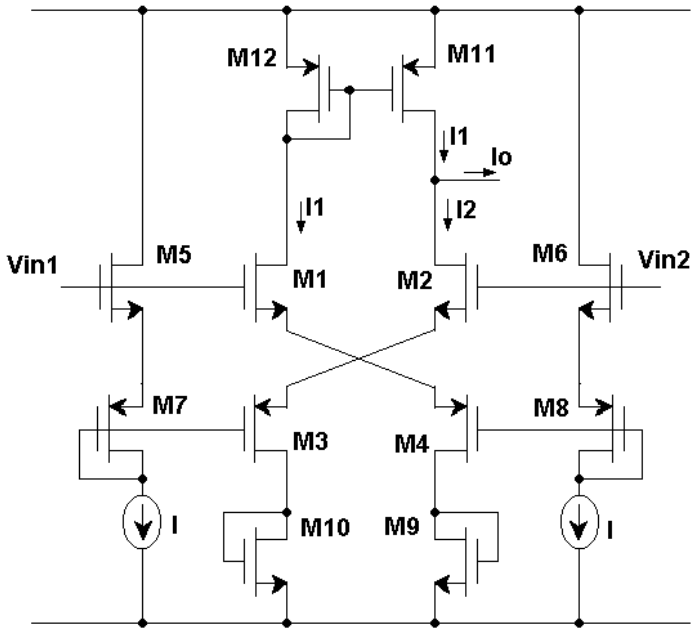


Figure 15: Operational amplifier with crossed transistors.

introducing instability. On the other hand, Harjani et al. [13, 14] propose another technique to implement an AB class amplifier with adaptive biasing using negative feedback.

The circuit proposed by Harjani et al. is based on a self-biased input transistor, illustrated in Figure 16(a). The M1 transistor is the input transistor, and Mb is the auxiliary input transistor. The amplifier op1 and the transistor M3 form a negative feedback loop. Suppose that the source voltage of M1 increases slightly; consequently, the output voltage of op1 will also increase. This increment will force the voltage Vs to drop, which secures the source voltage of the M1 transistor to be virtually equal to the source voltage of Mb. Due to the same voltages in M1 and Mb, the current density will be the same for these two transistors. The output voltage of op1 automatically adjusts to polarize M3 and provide the required quiescent current. In this way, two of these circuits can be combined to form the differential pair shown in Figure 16(a). This figure shows a new AB class opamp with adaptive biasing using positive feedback, where through the feedback mechanism the voltage of the M1 and M2 sources is always forced to follow the lower of the two voltages, Va and Vb; assuming that $Vin+$ increases in relation to $Vin-$. Therefore, the voltage Vb is greater than Va. Forcefully,

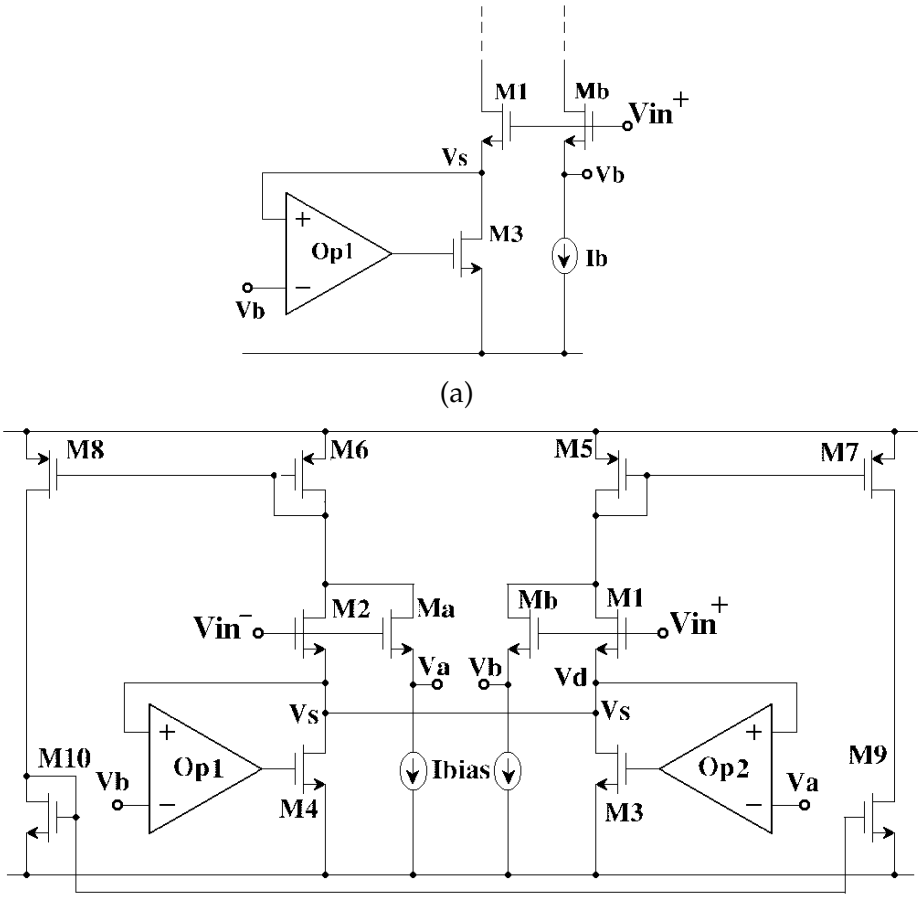


Figure 16: Operational amplifier with adaptive biasing.

the output voltage of op1 is pulled down, which switches M4 off. Due to the negative feedback, the drain voltage of M4 equals Va. Changing the size ratios of M2 and Ma for 10 the result can be, for example, Ib of 0.4 mA and Io_{max} of 800 mA. The minimum supply voltage for this circuit is $V_{GS} + 2V_{DSsat}$.

The two techniques for implementing one-stage AB class amplifiers are quite simple. However they do not maintain the minimum current and their gain is limited to $A_v = gmR_L$, requiring additional stages to increase.

2.3.2 *Two-stage AB amplifiers*

The second category of AB class amplifier consists of two or more stages. It has AB class control acting in the output stage. In this work, the study will be limited to two stages with the objective of preserving the simplicity and power consumption. In applications with low voltage [18] the common drain structure is hardly used because it has a low excursion of the output voltage, even presenting the characteristic of low output resistance. The common source structure, Figure 17, is the most used, presents excursion to the supply voltages (rail-to-rail) and; compared to the common drain structure has higher voltage gain, although with higher output resistance. In the common source structure the transconductance should be large enough to satisfy the stability condition. The quiescent current I_Q should be small so as not to increase the power consumption, and the maximum output current should be sufficient to feed high loads. There should also be a quick switchover between the transistors, i.e. the transistor should be kept connected with a minimum current to improve the switching speed between the transistors.

In Figure 18 we can observe the ideal transfer characteristic for an AB output stage, where I is the output current, I_P and I_N are the currents in the p and n channel transistors, respectively. The quiescent current I_Q is slightly higher than the minimum current $I_m in$. The maximum current depends on the power supply and the size of the transistors.

It is possible to identify two categories of output stages class AB CMOS according to how the quiescent current is controlled.

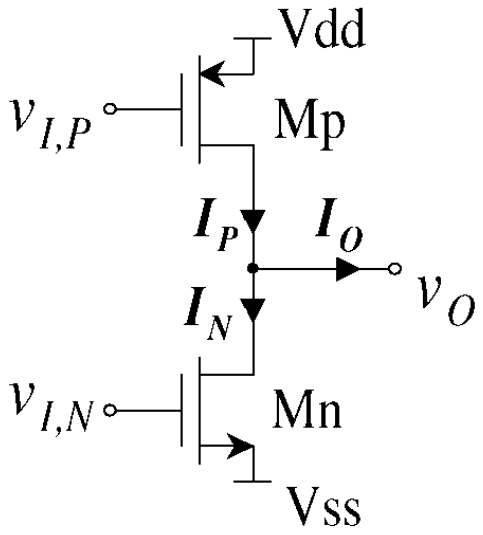


Figure 17: Common source output stage.

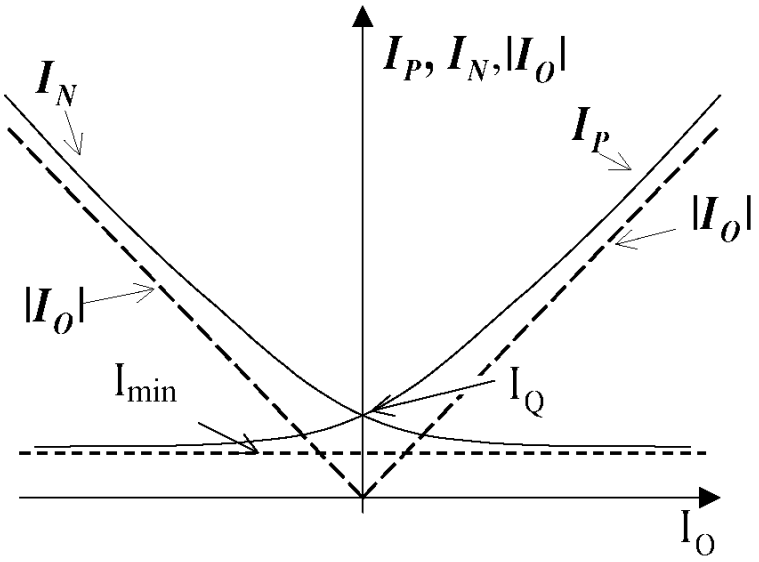


Figure 18: Ideal transfer characteristic.

1. No feedback loop. More stable. However, it has a V GS stacking of s transistors. [18-27, 44].

2. With feedback. It has lower supply voltage than the previous type, and its control is more precise over the quiescent current. However, its speed is reduced and may have stability problems because of the feedback loop [18, 23, 28-31].

The following subdivisions can still be identified regarding to the type of output quiescent current control:

1. Floating source - which is subdivided into level displacement, dynamic polarization with a resistor, switched capacitor and floating gate transistor [19-22].

2. Translinear polarization mesh or pseudo mirror [23, 24, 31 and 44].

3. Current mirror with the output transistors [25-27].

4. Pseudo-emitter follower [23 and 28].

5. With CMFB common mode feedback circuit - when the first stage output is fully differential [29 and 30].

Another important aspect related to class AB amplifiers is the maintenance of the minimum output current. As will be seen later, it is possible to find structures with or without the maintenance of the minimum current.

Floating voltage source

Figure 19 shows an AB class output stage with floating source. This circuit has a Vb polarization source with inverted polarity, which allows the output stage to have a transistor threshold voltage supply of the order.

Figures 20 shows two different ways of implementing the floating source [20, 21]. In the first case, a polarized Mb transistor with a small current I_b is used. In this case, $Vb = VSGMb$. In the second case, an Rb resistor is used instead of Mb and two Ib current sources. The

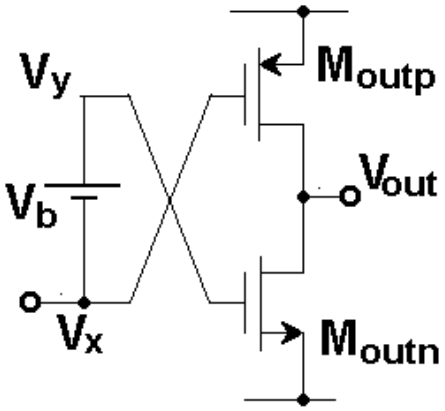


Figure 19: Floating voltage source.

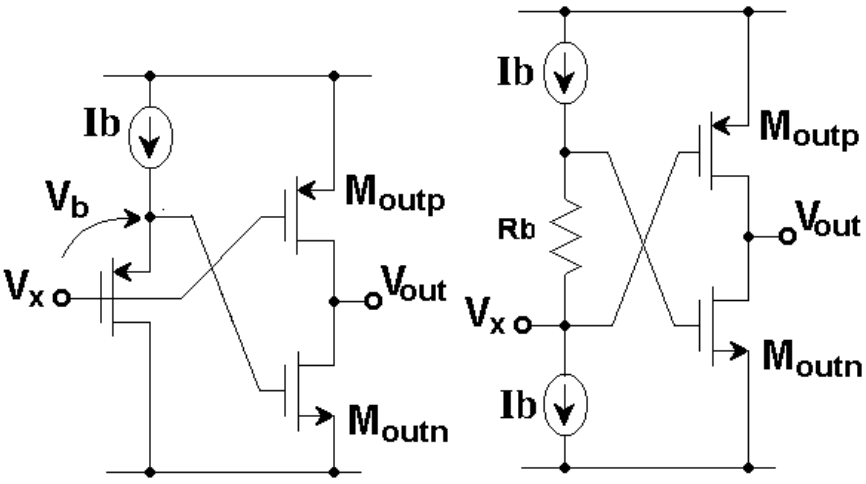


Figure 20: Floating voltage source with transistor and with resistor.

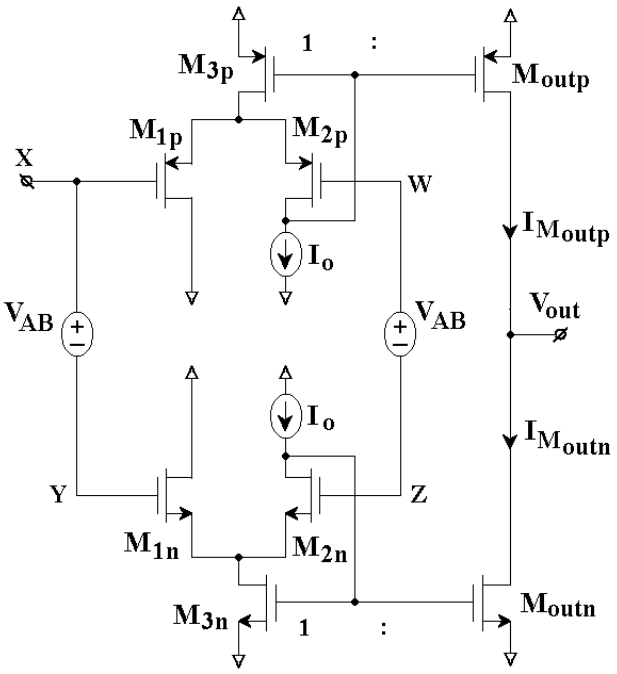


Figure 21: Floating voltage source with minimal current.

floating voltage is given by $V_b = R_b \cdot I_b$. In both cases the quiescent output current is determined by the current source Ib.

Figure 21 shows the implementation of an output stage with a floating source that maintains the minimum current [19] by use of a differential pair for low voltage [22]. The output current I_{Moutp} is proportional to the sum of the currents in M_{1p} and M_{2p}. When the voltage at the node x increases, the current of M_{1p} decreases, thus decreasing the current at the output. When M_{1p} cuts the output current is minimal and proportional to the current of M_{2p} The disadvantage of this structure is the generation of the voltage V_{AB}, which implies an increase in the complexity of the circuit. In [20], Torralba et al., use 12 transistors and two resistors to generate the voltage V_{AB}.

Translinear mesh

The term translinear originated from the characteristic of the *Bipolar Junction Transistor (BJT)* having the transconductance linearly dependent on the collector current [45]. The translinear

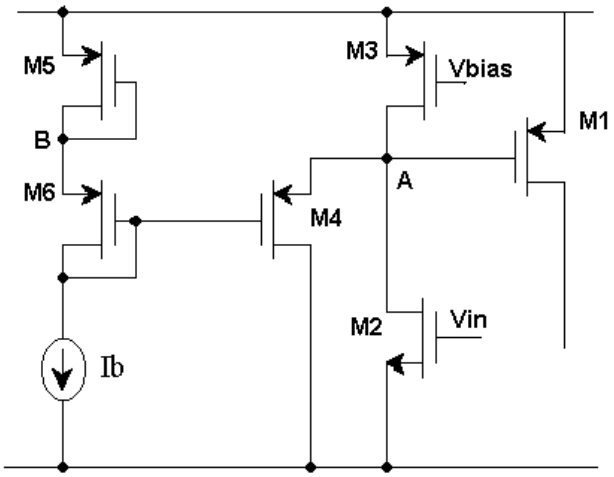


Figure 22: Translinear mesh output stage.

concept can be extended to the translinear mesh of BJT transistors with base-collector voltages connected in series clockwise and counterclockwise and with an equal number of transistors on each side. For the MOS transistor, in weak inversion, the translinear law is the same as for the BJT. However, in strong inversion there is the quadratic translinear law [46]. In both cases, the circuit is independent of technological parameters and temperature variation. The great advantage of translinear circuits is the performance of nonlinear functions by linear elements.

Figure (22) shows the p side of a push-pull circuit. The translinear mesh is formed by M1, M4, M5 and M6 transistors. This circuit is also known as a pseudo current mirror. In the quiescent condition the voltage at node A is equal to that of node B. In this situation the current through M1. Therefore the current in the output branch is given by I_b times the ratio between the size of the M1 and M5 transistors. The main disadvantage of this structure is its supply voltage in the range of $2V_{GS} + V_{DSsat}$.

Monticelli's AB class output structure [18, 24], Figure (23), is widely used in low voltage. The quiescent output current is fixed through two translinear meshes formed by transistors M1, M2, M6, Mn and M3, M4, M5, Mp. The i11 and i12 currents can be obtained from single or cascode transistors. One of the advantages of this structure is that the output transistors, Mp and Mn, never cut. This is achieved through proper design, i.e. when the M6 current

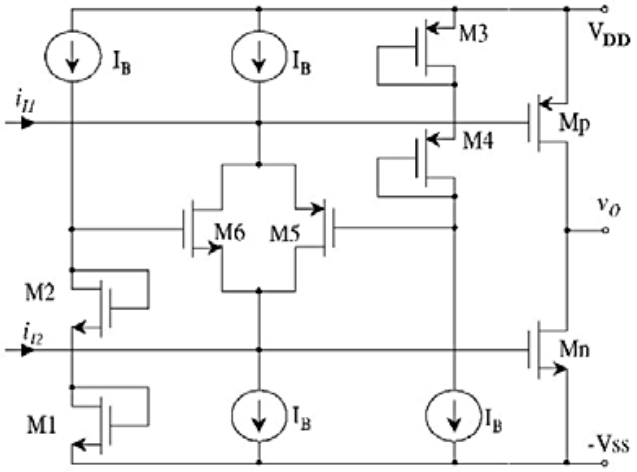


Figure 23: Output stage without feedback.

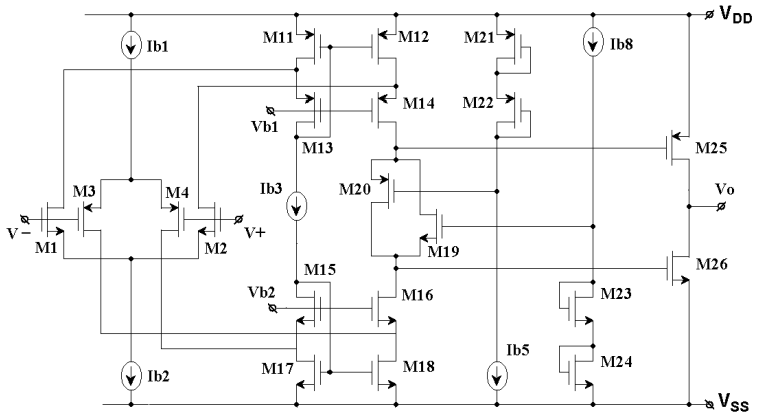


Figure 24: Amplifier without feedback.

passes through M5 the potential at the source of this transistor should be such that it keeps Mp on. In this way, a minimum current is maintained in the Mp and Mn transistors, thus improving the response speed of the output. The structure can still have high voltage gain, depending on whether or not cascode mirrors are used for the current sources. Its minimum power supply is $2V_{GS} + V_{DSsat}$.

Yan et al. [18], present a structure very similar to Monticelli's structure differing in the maximum excursion of the voltages in the gates of the output transistors providing greater excursion, but at the expense of an increase in the polarization current due to the increase of branches to produce the polarization voltages.

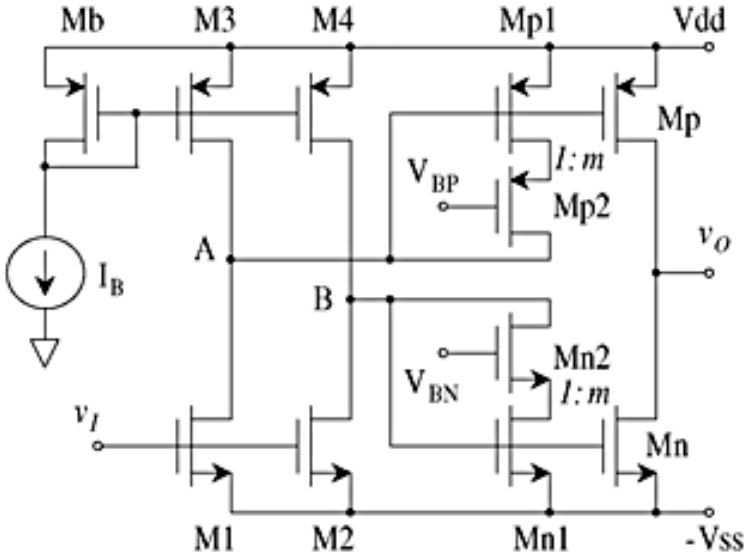


Figure 25: AB output using current mirror.

The amplifier shown in Figure (24) was proposed in [44]. This device is similar to the one proposed by Monticelli, and the difference is in not needing additional sources to polarize the AB class control circuit formed by the M19 and M20 transistors. However, its minimum supply voltage is $Vsup = 2V_{GS} + V_{DSsat}$.

Current Mirror

The quiescent output current is established employing current mirrors with the output transistors. In Fig. 25 it can be seen that the quiescent currents of Mp and Mn are fixed by mirroring the polarisation currents of the Mp1, Mp2 and Mn1, Mn2 transistors. This structure, proposed in [25], has a minimum supply voltage of $V_{GS} + V_{DSsat}$, which can be considered excellent for class AB. Mn2 and Mp2 transistors have a small aspect ratio compared to Mn1 and Mp1 transistors. Current mirrors have m transformation ratio.

The disadvantage in the use of current mirrors in the output stage is that this mirror generates low impedance nodes such as nodes A and B of Fig. 26, overloading the output of the first stage and consequently reducing the gain. However, there are some ways to get around this difficulty. In the circuit proposed by Chih-Wen-Lu et al. [27], Fig. 26, the mirror

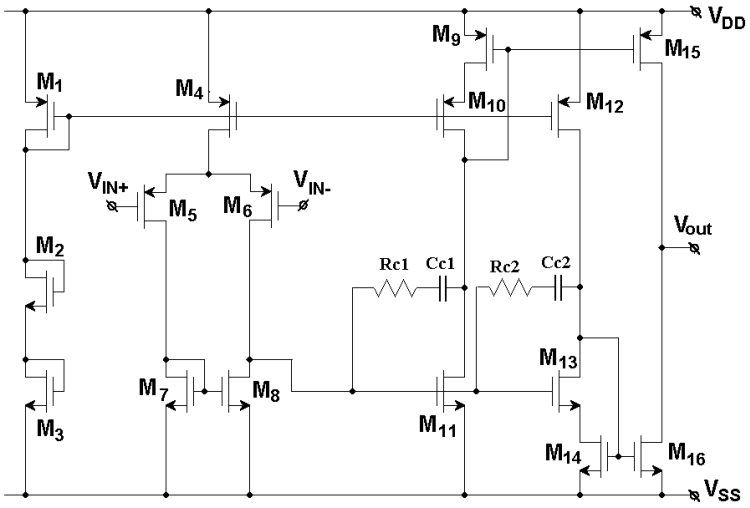


Figure 26: AB amplifier using current mirror.

input is made at the transistor gate (high impedance node). In [19, 26] is also used a mirror in the output stage for the maintenance of quiescent current.

Feedback control

In Fig. 27 [18], it is presented a push-pull output stage with an AB control block that acquires a sample of V_{GS}, or I D from the output transistors and generates an $i_F B$ feedback current that causes V_A and V_B to vary to adjust the polarization of the output transistors. Note that V_A and V_B control i_P and i_N, respectively, and thus the output current i_o.

The great advantage of opamp with AB class feedback control is that it operates at lower supply voltages than the non-feedback one. However, the reduced supply voltage requires a more significant number of circuit branches, usually leading to higher quiescent power consumption, higher active area occupation and lower frequency response.

Below are some topologies for AB class using feedback control.

Pseudo source follower

In order to maintain the low output impedance characteristic of a source follower, in [23] the common source configuration with a feedback circuit is presented, Fig. 28. In this figure, the

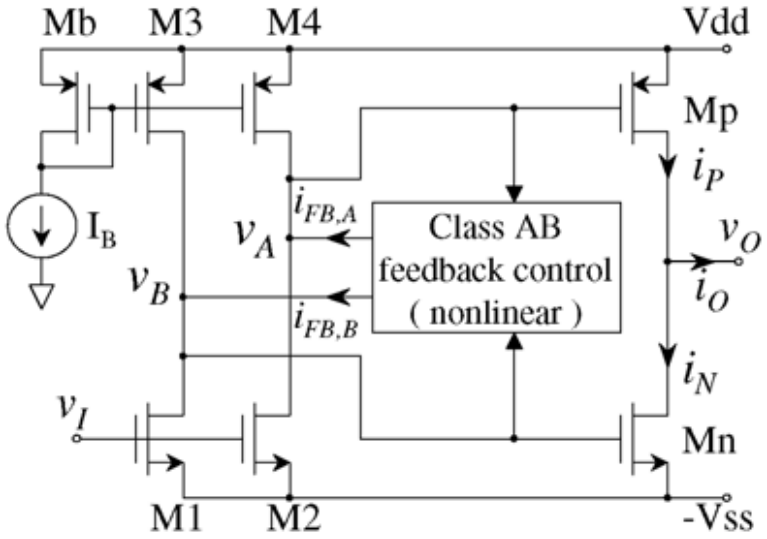


Figure 27: Feedback control in AB output stage.

feedback loop Av1-M1 and Av2-M2 ensures low output impedance. This provides a high current capacity and shifts the output pole to high frequencies even for a large capacitive load.

The two Av1 and Av2 amplifiers must meet three requirements for proper operation; they must be broadband to avoid crossover problems, must have output and rail-to-rail input and must have reduced voltage gain, less than 10, to limit the offset. Otherwise, the offset effect becomes significant at the output.

In [28], some modifications were made in the stage presented in Fig. 28, seeking to reduce the effects of the offset introduced by the amplifiers Av1 and Av2.

Common mode feedback

When the output of the first stage is maintained fully differential, it is used common mode feedback circuit to control their common mode voltage outputs and, therefore, control the quiescent current of push-pull stage transistors of exit. Fig. 29 shows, conceptually, a structure with common mode feedback [23, 29, 30]. The CMFB circuit controls the level of quiescent current in the exit. M3 and M4 generate a lag of 1800 in one of the outputs of A1. When there is no current at the load the differential voltage of output A1 is zero and the

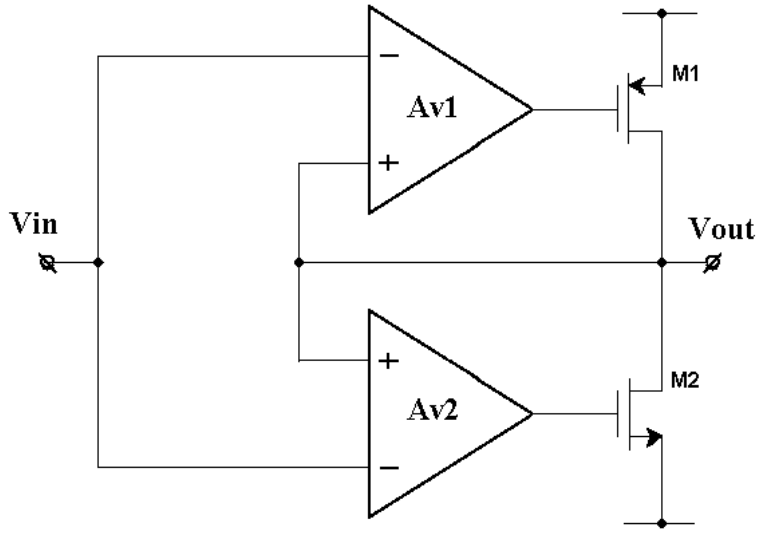


Figure 28: Pseudo source follower.

current in M1 and M2 is the this because the relationship between the aspect ratios of M2 and M4 is equal to the relationship between the M1 and M3 aspect ratios. The quiescent current at the output is controlled by Ib and the ratio of the aspect ratios of M5 and M2, because the feedback circuit forces the common mode voltage at output A1 to be equal to V_D . When the circuit is required to supply or absorb load current, the differential output of A1 comes to be, and this has the effect of turning M1(M2) on and M2(M1) off. A problem of this circuit is that, for high current in the load, M2 (or M1) comes to be completely disconnected with his gate too close to the ground. This produces a delay in the switching of the transistor in the presence of rapid signals. There is no maintenance of the minimum current in the output transistors.

Translinear mesh with feedback

The circuit in Fig. 30 is an example of an AB class output stage fed back using a translinear control loop. Details of this circuit can be found in [31]. The translinear loop is formed by R14, M15, M4, M6, M13 and R13, where M13 = M15 and R13 = R15. The M3-M6 transistors are placed to allow a supply voltage as low as $V_{GS} + 2V_{DSsat}$ and form a summation circuit for the input currents Iin1 and Iin2 . These transistors distribute the signal from the input

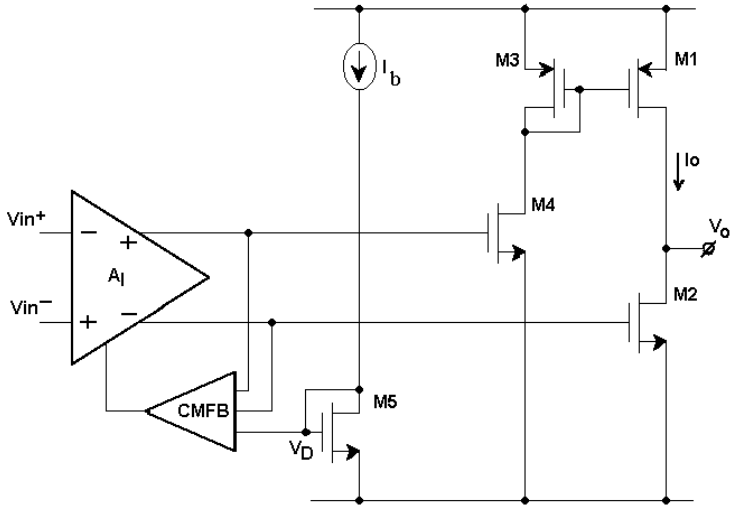


Figure 29: Common mode feedback output stage.

stage to the output transistors. The current in M1 is measured by M11 and is used to generate a voltage through R 13. Current in M2 is measured by M12 that flows through the M19, M17 mirror and generates voltage through R 15. The lower of the two voltages through the resistors, which corresponds to the lower of the polarization currents of the output transistors, controls the output of the decision pair M13, M15, which is connected to the M6 port. This voltage controls the amplifier formed by M4 and M6 which are part of the loop. The amplifier regulates the control voltage equal to the reference voltage created by M14 and R14, controlling the signal at the output transistor port. Thus, the feedback loop is formed by also controlling the minimum current of the output transistors.

Another form of feedback AB control circuit is shown in Fig. 31. The translinear mesh is given by V R , M1, M2, M4 and R4, being M4 = M5 and R4 = R5. The output stage currents are not directly controlled. On the contrary, the push-pull currents are measured via M3 and M8 and then regulated for AB class operation. This allows the output stage to function with extremely low supply voltage.

The V GS voltages of the output transistors are represented by the drop of resistors R4 and R5. These voltages are measured by M3 and M8 and are then compared by the differential pair M4 and M5. The difference is transferred to the input of an M1 and M2 control amplifier

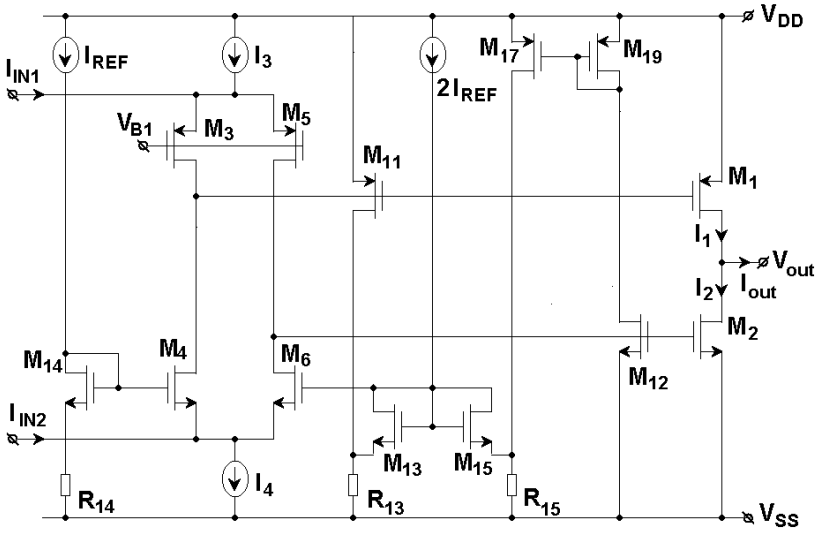


Figure 30: Feedback control output stage with folded mesh.

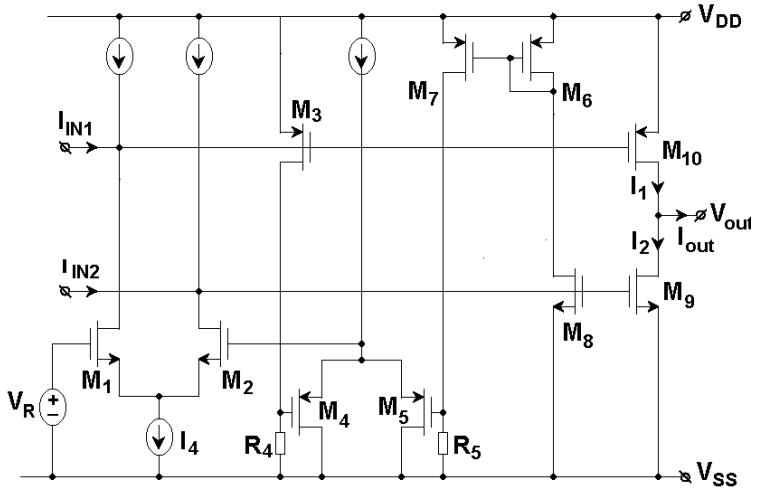


Figure 31: Feedback control output stage.

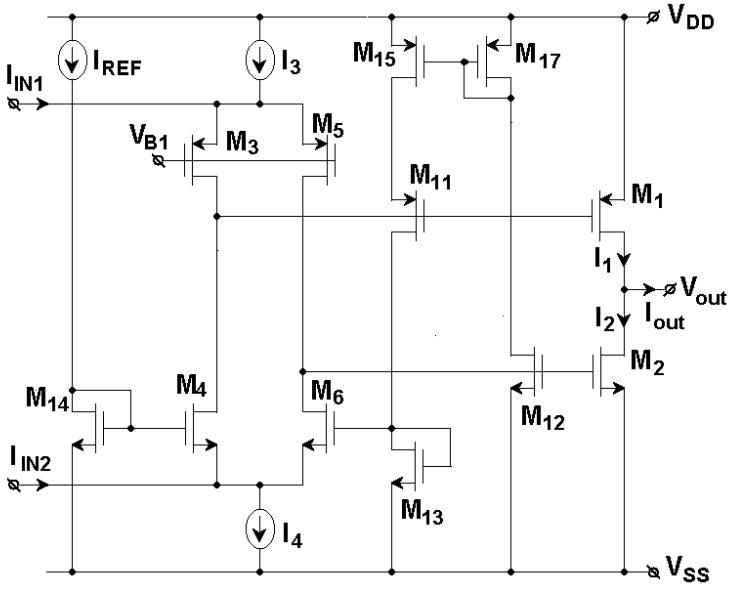


Figure 32: Minimum current output stage.

that controls the polarization of the output transistors, such that the two output currents are set to a single constant value which corresponds to the quiescent value I_Q. The feedback control circuit also controls the minimum current in the output transistors.

The maximum output current can be increased because the voltages at the output transistor ports are capable of reaching one of the supply voltages at less than one saturation voltage. The minimum voltage required to supply this circuit is equivalent to $V_{GS} + 2V_{DSsat}$.

Minimum current circuit

In Fig. 32 is the circuit presented in [31] that uses a minimum current selector circuit that controls both the quiescent current and the minimum output current.

The current of M2 is measured by M12. The M12 drain current flows through the M17, M15 current mirror, which is part of a M11, M15 and M17 minimum current selector circuit. The M15 transistor operates mainly in the linear region. Only when M1 controls high currents does M15 operate at saturation. M11 measures the M1 current. The M11 drain current flows through M13 and controls the AB class M4, M6 amplifier. The AB class amplifier regulates the signal at the output transistor ports in such a way that the current

through M13 is equal to the reference current I_{REF} that flows through M14. If the output stage is in the quiescent state, the M1 drain current is equal to the M2 drain current. In this situation, the M11, M15 and M17 transistors would be designed such that their source-gate voltages are equal making M15 operate in the triode region, and M11-M15 behave as a single transistor of double channel length. So the quiescent current will be expressed by (20).

$$I_Q = 2\frac{W_2 L12}{W_{12} L2} I_{REF} \tag{20}$$

When M1 delivers a high current, its supply port voltage will be high, and the voltage between the positive supply and the M11 source will be sufficient for M15 to operate at saturation. The M17, M15 and M11 transistors operate like a cascode mirror and simply mirror the current from the M12 to M13 transistor. In this way, the current of the M12 transistor is set to a constant value equal to half the quiescent current. The minimum current is set by equation (21).

$$I_{min} = \frac{1}{2} I_Q \tag{21}$$

Low resistance load

Below are three topologies suitable for applications with extremely low resistive load.

In [32], a 1.5V CMOS class AB amplifier is shown with a voltage of power supply that can excite high loads with low distortion. Its output stage includes an elementary shunt stage excited by a transconductance block. Only 7 transistors are required to implement the output stage, including control of current class AB. The quiescent output current is fixed by the pseudo-follower method. If the output impedance of the shunt stage is low, the second pole caused by the capacitive output load C L will be located at a relatively high frequency (approximately $-gm/CL$). This is a fed back circuit where there is no maintenance of the minimum output current.

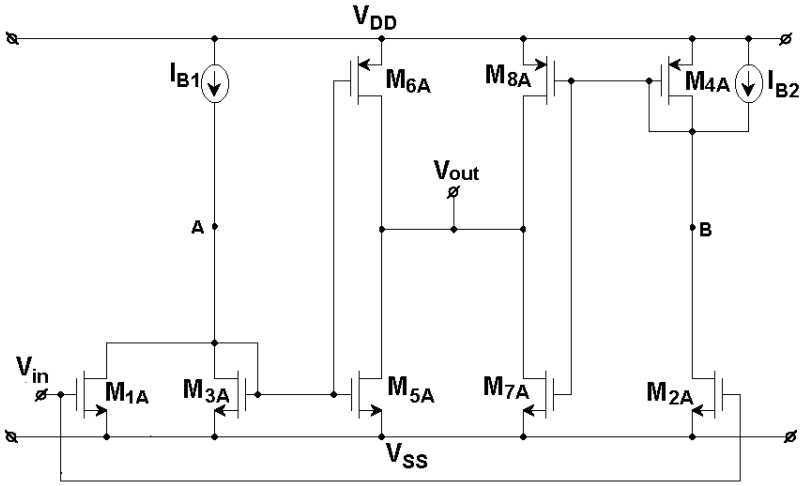


Figure 33: AB output stage with inverters.

The second structure is presented by Palmisano [26]. In Fig. 33 it is observed that the output stage consists of two inverters with common outputs. Each has a transistor in saturation (M5A, M8A) and the other in cut (M6A, M7A).

For a low level of input voltage, M6A and M7A are cut off, and the circuit operates in class A with high linearity. The currents in the M5A and M8A output transistors are supplied by M1A and M4A, respectively. When Vin increases $I_{D1A} = I_{B1}$, M3A and M4A respectively. M5A cut and node A becomes a high-impedance node being carried near VSS. M6A drives and delivers a high current to the output load. M7A remains cut, and the current in M8A also increases, but its value is limited by the low impedance of the node B. In this way, most of the output current is supplied by the M6A transistor, which, was cut into the quiescent state. When Vin decreases, there is a behaviour similar to the other part of the circuit.

The M5A and M8A transistors are designed with a low aspect ratio to ensure low power dissipation. On the other hand, M6A and M7A, which are cut off in the quiescent state, are designed with a high aspect ratio to provide high current capacity at the output. Control of the quiescent output current is achieved by through M3A, M5A and M4A, M8A current mirrors. This structure does not have the maintenance of the minimum current of the output transistors.

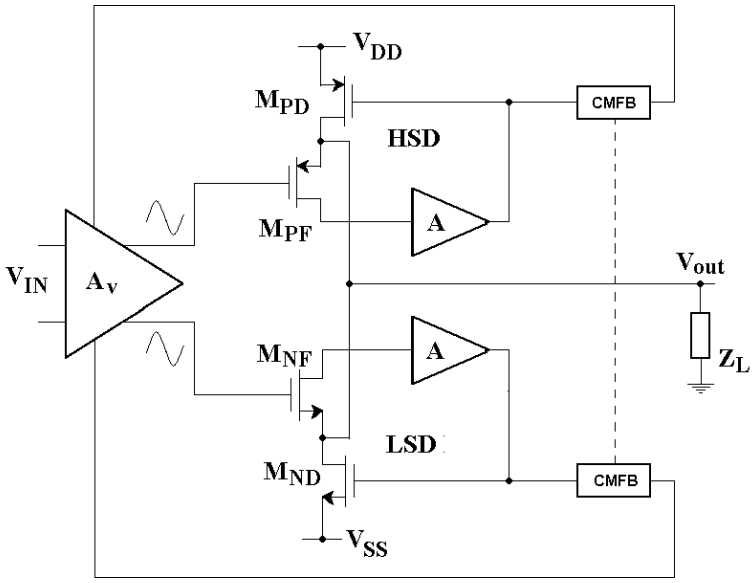


Figure 34: Common source/drain output stage.

Finally, it can be observed the structure presented by Rincó-Mora [33] that proposes an AB class opamp with extremely low output impedance and large current capacity, Fig. 34. Its output is composed of two basic blocks, a driver (HSD) and a recharged lower driver (LSD), which are capable of providing and absorb large amounts of current from the load Z_L. Each driver is composed of a source tracker, $M_{NF}(M_{PF})$ and a common source, $M_{ND}(M_{PD})$, working simultaneously across the entire common mode output range. Source follower ensures low output impedance and the common source rail-to-rail output excursion with a capacity for high current. Each side of the output circuit (HSD, LSD) has a feedback loop. It is reducing the output impedance by the mesh feedback factor. Power in the range of 1.5V, $I_Q = 140\mu A$ and $i_{max} = 7mA$. The disadvantage of this structure is in the complexity of the circuit.

The CMFB circuit ensures AB class operation of the amplifier by stabilizing the quiescent current and the minimum operating current. The CMFB has a differential pair sensitive to the minimum current by controlling it through the Av stage.

2.3.3 *Summary*

AB class amplifiers typically require structures with effective quiescent current control and maintenance of minimum output current. In the literature, the ones that present this type of control are those of Rogervorst et al. [44], without feedback and fed back. The former cannot be supplied with voltages lower than $2V_{GS} + V_{DSsat}$, the latter is fed back and sophisticated. Ramirez-Ângulo et al. [19] presents a structure with minimum current maintenance but needs additional circuits to generate the voltages V_AB , which makes the circuit complex. The structure that presents the best conditions is the one presented by Huijsing et al. [31] with minimum current maintenance. However, this circuit needs an additional circuit (mesh) to generate the polarization voltages of the output transistors, besides having a higher offset generation due to differences in the additional structure voltages.

Observing the various forms of implementation of class AB amplifiers, it can be seen that there are structures without feedback with quiescent current control performed by translinear mesh, floating source and current mirror, where some have the maintenance of minimum current. Other structures are fed back with quiescent current control through the translinear mesh, common mode feedback, pseudo source follower circuit and minimum current selector circuit. With increasing complexity, it is possible to feed resistive loads in the range of tens to hundreds of ohms.

For the work developed here, it is intended to obtain a relatively simple structure (two stages plus control circuit class AB), with efficient control of the quiescent current and maintenance of the minimum current at the output. Along with low power consumption (in the range of 10 mW), with extremely low supply ($V_{GS} + 2V_{DSsat}$), while occupying a relatively small area ($0.02mm^2$). It is essential that the opamp open loop gain is high (above 100dB), so two or more stage structures with cascode mirrors are to be implemented.

3

DEVELOPMENT

3.1 SELF-BIASED CURRENT REFERENCE

According to the consideration described in Section 2.3 an original design is developed. A selection of those circuits, with agreed design specifications, were thoroughly tested and simulated with the select technology. From the simulations results from circuit topology from Hirose et al. (2010) was found to be very significant to the project development.

The aforementioned research article develops a nanoampere current reference, including temperature dependence control. In the article, both p and n-based, separate current references are designed. The subtraction of the symmetrical currents achieves temperature independence. The upcoming Figure 35 presents the aforementioned, p 35(a) and n-based 35(b), circuits separately.

Both were simulated using the *Electronic Design Automation (EDA)* tools with proprietary $0.35\mu m$ CMOS technology. The results showed in Figure 36, with the positive current belonging to the NMOS bias current and the negative one to the PMOS, using 1:1 current mirror connected to the corresponding biasing gate voltages.

In accordance to the research described during the background section an original design is developed. The following circuit design is based on a combination of the features from the research. Several improvements were made, with the aim to increase the power efficiency significantly, while keeping a decreased footprint.

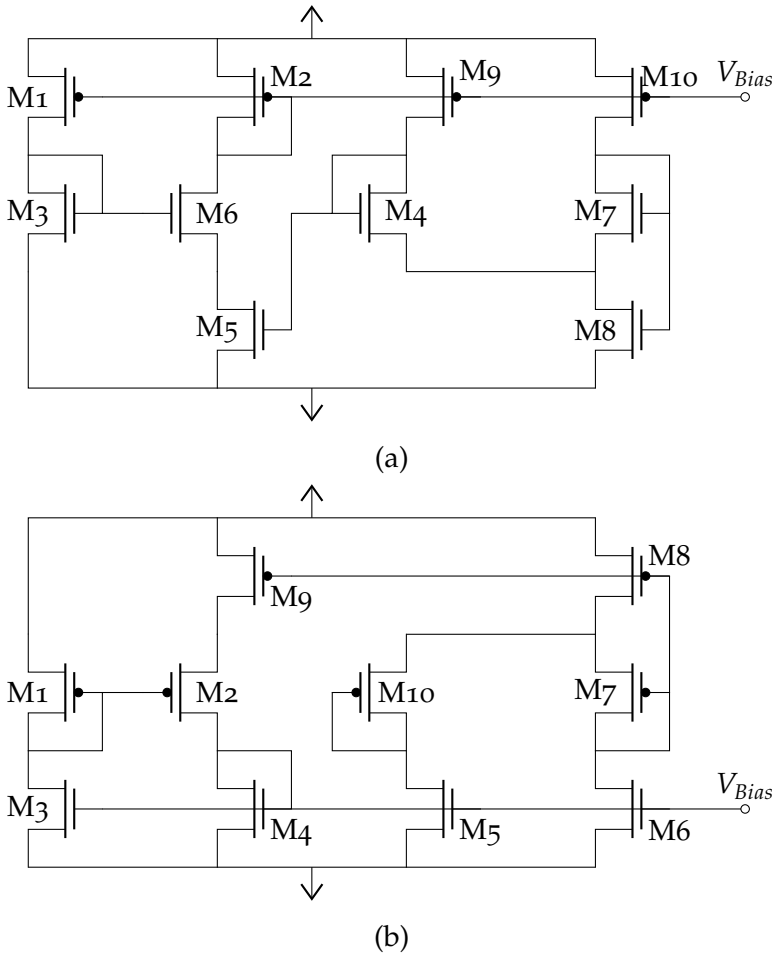


Figure 35: Self bias current reference.

The presented circuit has, as its foundation, current generation cell consisting of p channel transistors. Additionally, the current mirroring is performed by the n-type transistors. The transistors perform in the sub-threshold region, either in the weak or strong inversion.

The output current is mostly dependent on the p-type MOSFET M2, as a consequence of the voltage driven to its gate, incoming from the voltage divider cell. Assuming the PMOS M2 is in the strong inversion region, the output current can be expressed by (22) and (23).

$$I = \beta V_{DS2}(V_{GS2} - V_t) \tag{22}$$

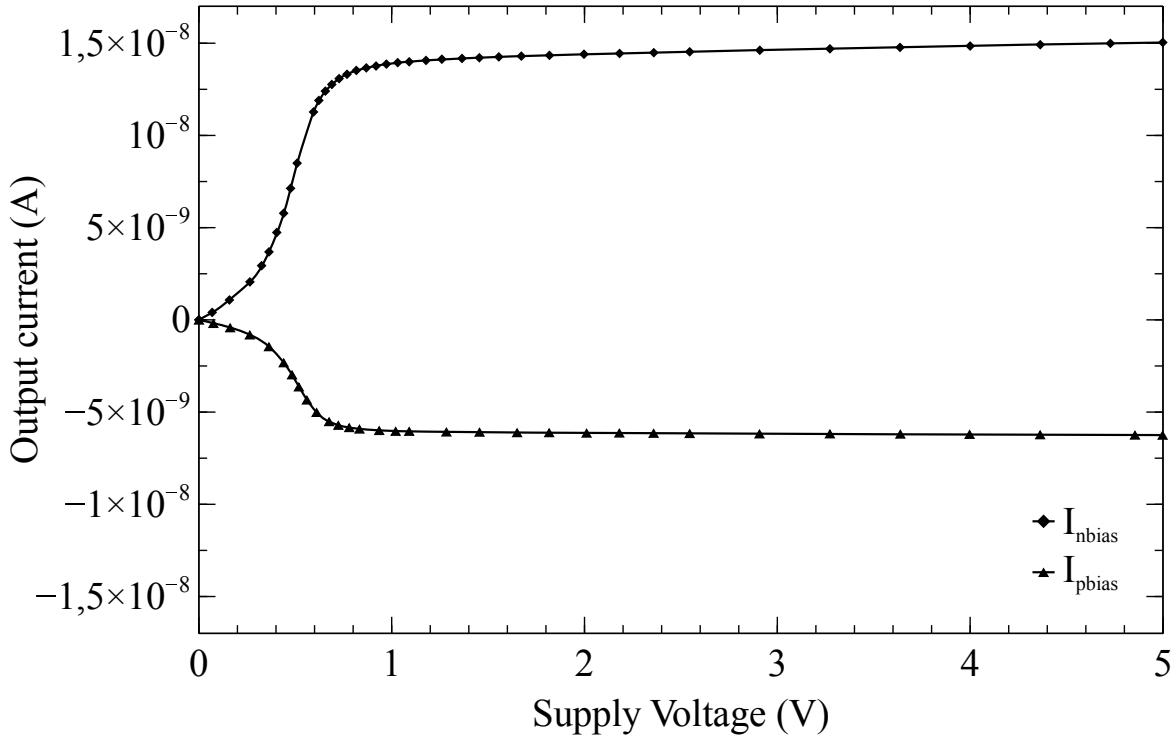


Figure 36: Measured current reference of (35).

Table 2: Proposed Circuit Transistor Size

Transistor	Width (μm)	Length (μm)
M_1, M_9	60	3
M_2	300	3
M_10	252	3
M_3	6	3
M_12	250	3
M_4, M_5, M_6, M_13	6	3
M_7, M_11	6	3
M_8	4	150

With

$V_{GS2} = V_{GS} + \eta V_t ln\left(\frac{K_4}{K_3}\right)$, and

$V_{DS2} = \eta V_t ln\left(\frac{K_5}{K_1}\right)$

$$I = \beta\eta V_t ln\left(\frac{K_5}{K_1}\right)\left(V_{GS1} + \eta V_t ln\left(\frac{K_4}{K_3} -\right) V_t\right) \tag{23}$$

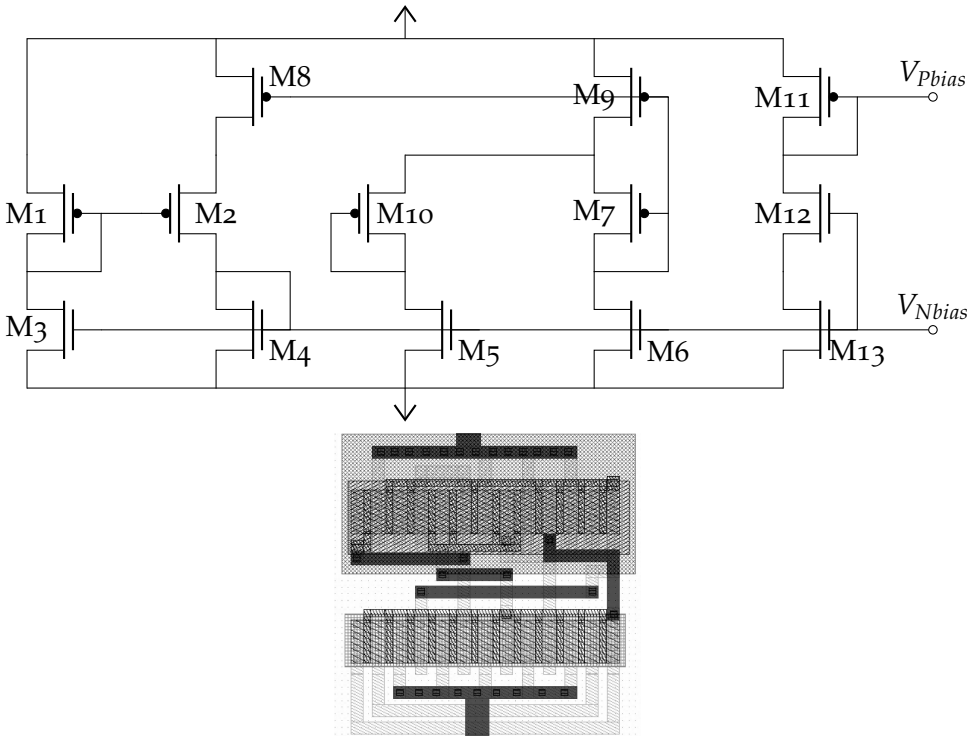


Figure 37: Proposed nano scale self biased temperature and voltage independent low power current reference.

3.1.1 *Simulation Results*

In order to test the proposed circuit, SPICE simulations tools were used. The appropriate $0.35\mu m$ CMOS technology was sourced from the chosen fabrication company.

The obtained results in Figure 38 show that I_P, the current reference sourced from the p-type transistors, can keep a constant current as long the power source is superior to 1.6V. In reflection, I_N generates a very similar current, demonstrating this current reference circuit as moderately suitable for analog/digital design.

In addition to the first simulations, more specific testing was made. The current reference was measured with temperature variations, considering the ambient temperature (20°C) as a reference point, a spectrum from -20 to 60°C was contemplated. This temperature range is identified ample enough for the circuit purposes. The results are exhibited in Figure 40, showing the accentuated disparities on I_N. Despite the fact both currents display an

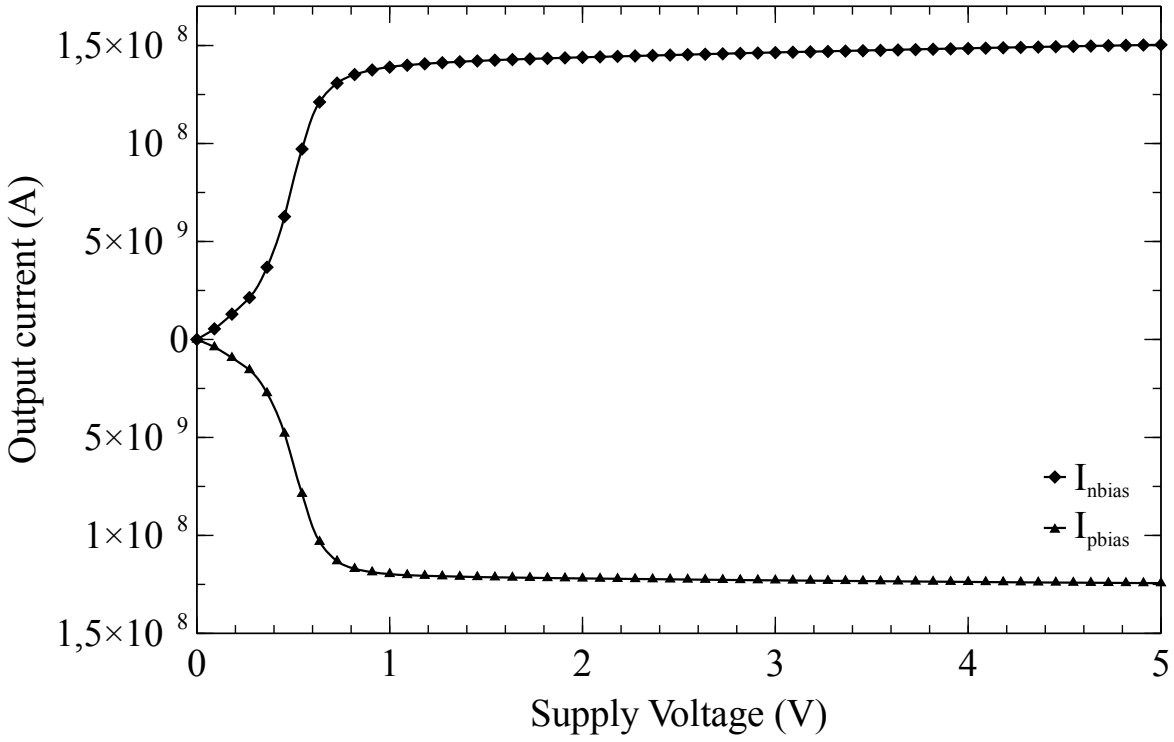


Figure 38: Simulation results depending on source voltage at ambient temperature.

increase with temperature, the current increment is not proportionate, which may originate complications in precision circuit design.

The PSRR was measured, Figure 42, with a voltage supply of 3 V and a filtering capacitor, $C_f = 1pF$, the rejection ration at 100Hz was measured to be around 45dB. The results show the power supply independence capability of the current reference.

Layout design

Using the rules imposed by the CMOS technology process guidelines provided by the foundry, the layout was designed 37. These rules are intrinsic to the device transistors, meaning that sometimes limit the operation functionalities of the application. However, can also be useful when implementing references using the intrinsic, unchangeable values.

In order to future proof the layout design, scalable CMOS rules based on the λ parameter were used conjointly. Over time, CMOS processes incline to be outdated and be replaced by better processes, smaller in size and better performance with lower power consumption.

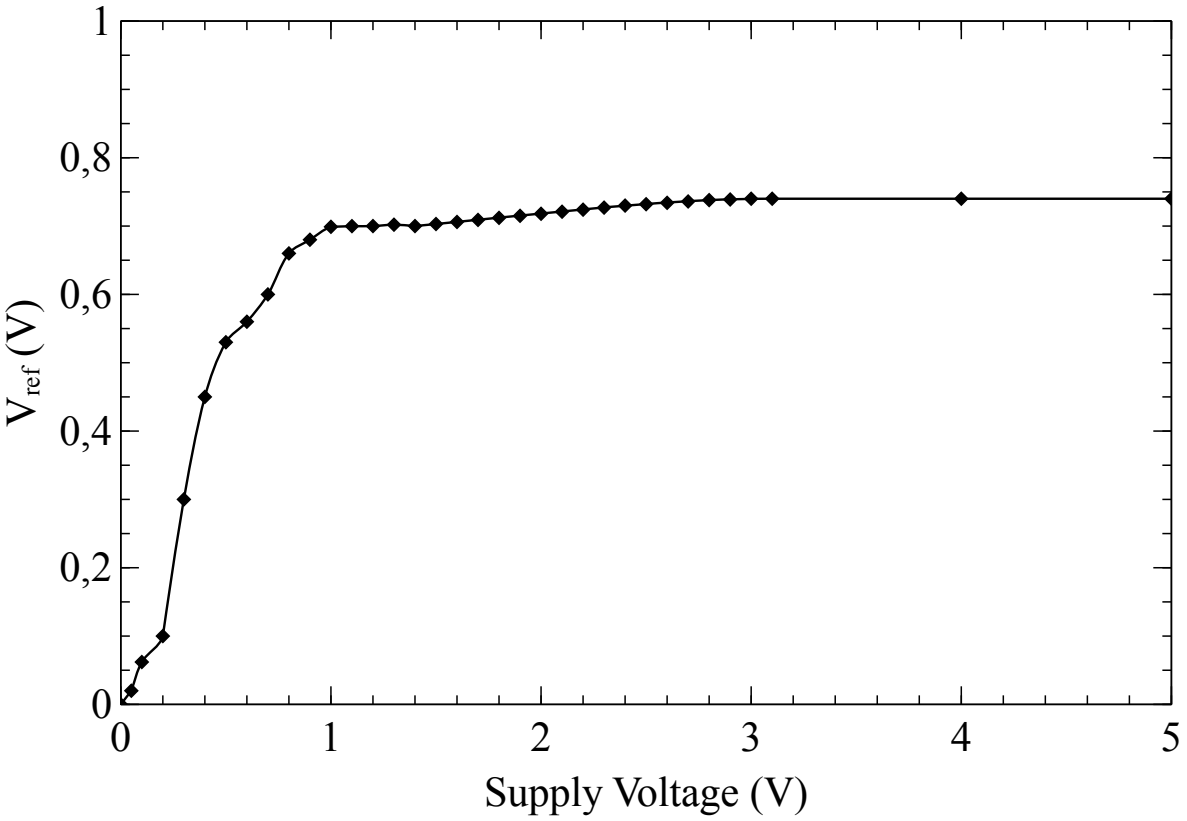


Figure 39: Voltage reference results at ambient temperature.

The design used cannot guarantee full compatibility with the newer processes. Nevertheless, it allows for faster integration with small modifications to the original layout.

3.1.2 *Discussion*

The proposed current reference final design attempts to assemble a circuit. Which encompasses the leading benefits from each specific research, as mentioned earlier. A direct comparison is possible, between the original concepts and the presented final circuit.

One essential objective for the design is the temperature independence of the circuit. The researched technique, using a square rooting interface, was organically added to the proposal. The temperature stability is achieved by using two intrinsic voltages available with a reversed temperature coefficient.

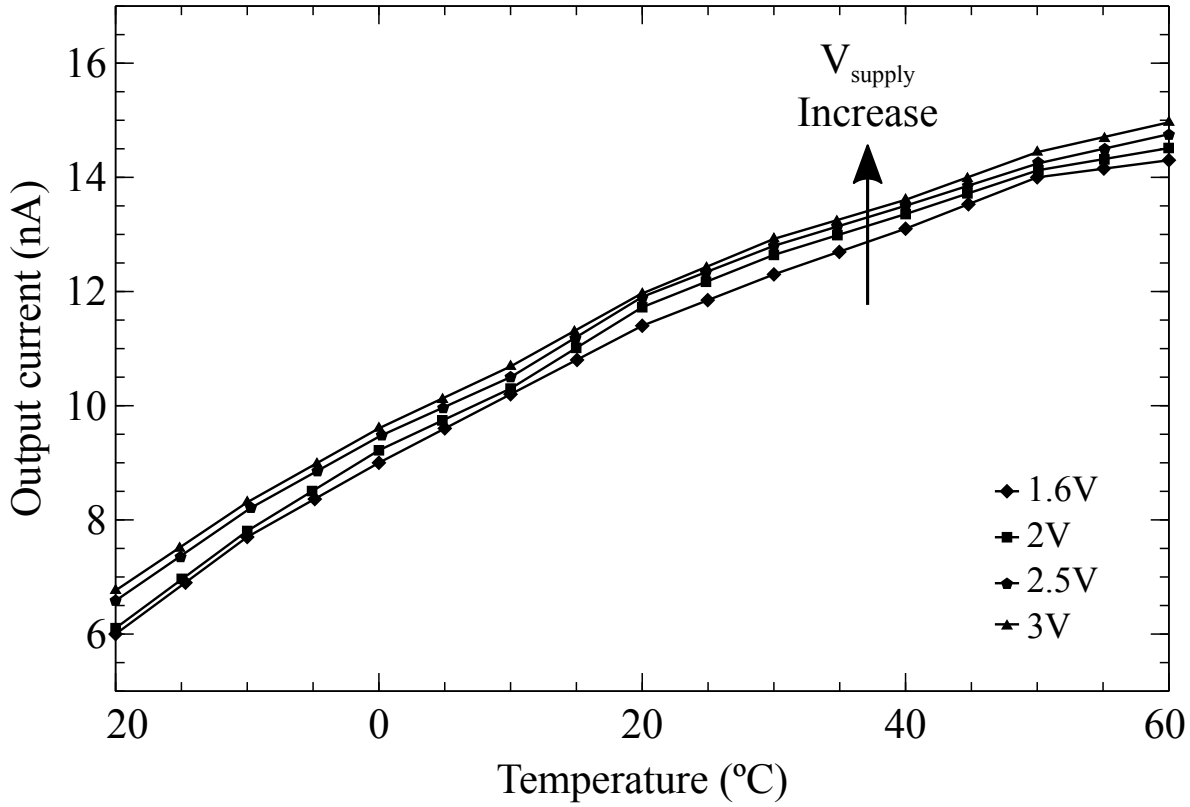


Figure 40: Measured current with temperature variation.

The temperature coefficient of the present design is calculated at 425 ppm/V, a better outcome than the 1190 ppm/V result reported by Hirose et al. (2010). Further temperature variation can be seen from the simulation results in Figure 40. This graphical report shows a slight deviation for the current output upon simulated temperature changes.

Fabrication process discrepancies are also taken into account. Supplementary testing is necessary to confirm the deviations created by the fabrication. Although, the techniques and criteria used in the design should establish a reasonably stable device. The circuit is resistor-less, a component in CMOS technology responsible for the significant anomalies. The previously considered approach, switched capacitor method, was dismissed. The technique expanded the integrated circuit area considerately. Acknowledging the benefits, process stability, versus the disadvantages, area expansion and power misuse. It was deemed inappropriate for the use of this method.

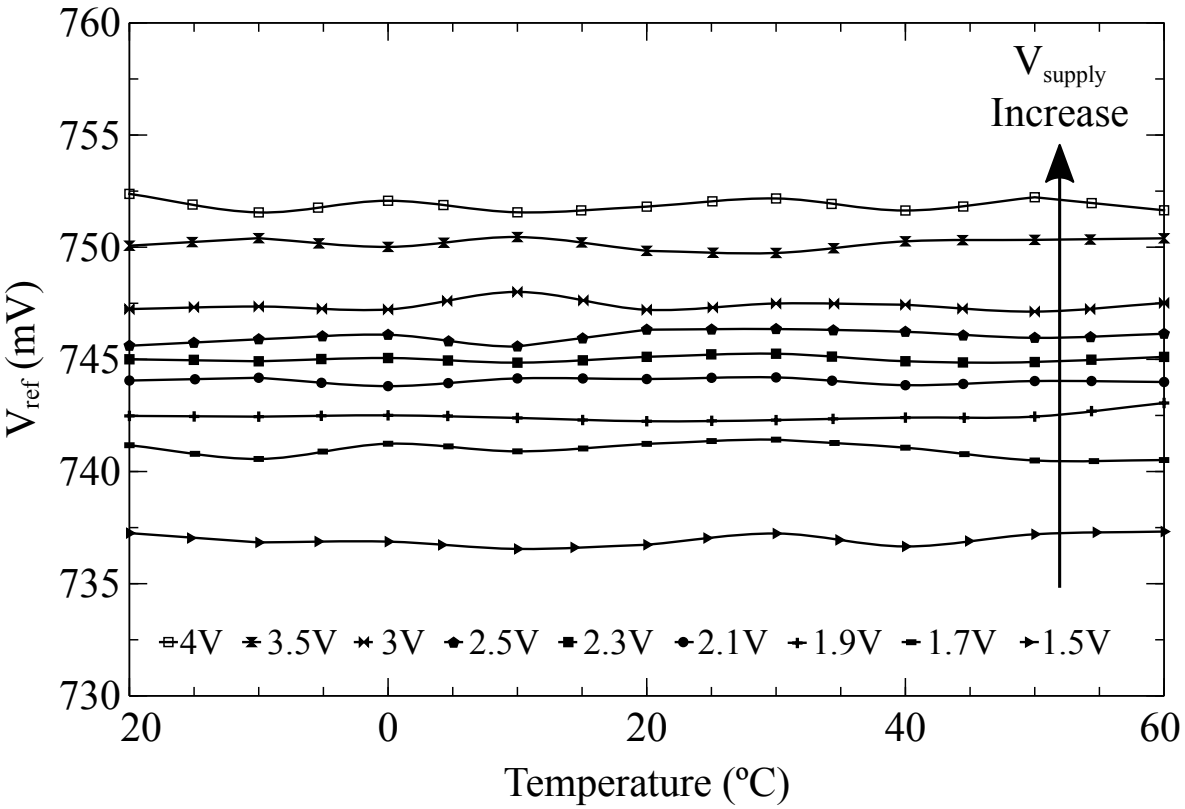


Figure 41: Voltage reference measurements with temperature variation.

The final main goal, the creation of a low power current reference, capable of achieving a nanoampere current output, was achieved. Afore shown in the results section, the circuit produces a nominal current of 12 nA when compared to researches as Hirose et al. (2010) and De Vita and Iannaccone (2007), the circuit attains a similar output performance. However, the proposed new circuit incorporates features which are not available in these similar circuits.

An overview comparison is available in TABLE 3. The presented circuit measured values are compared to similar circuits. The data was acquired by the review of research articles and work reports of the mentioned projects.

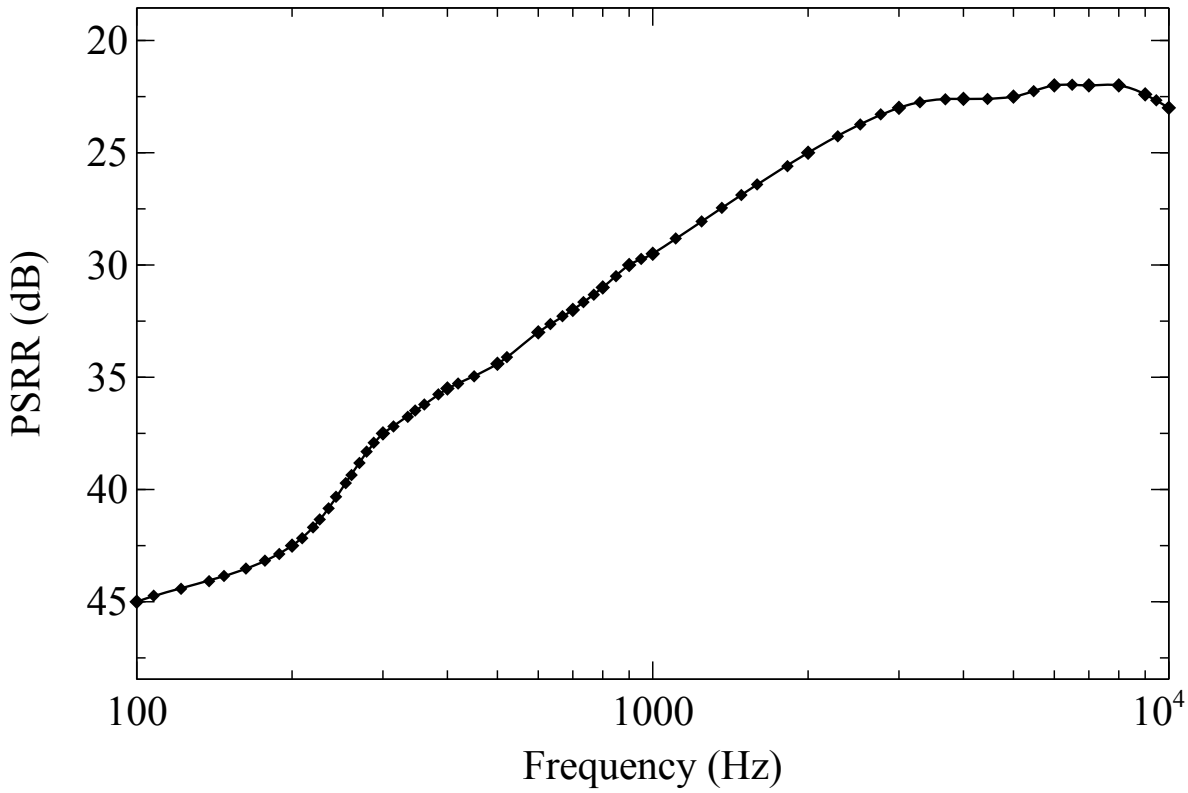


Figure 42: Simulation results of the power supply rejection ratio depending on the frequency.

Table 3: Research Comparison

Parameters	Proposed Circuit	Hirose et al. (2010)	De Vita and Iannaccone (2007)	Sansen et al. (1988)	Georgiou and Toumazou (2002)
CMOS Technology (μm)	0.35	0.35	0.35	3	0.8
Output Current (nA)	12	9.95	9.14	774	430
Minimum Supply Voltage (V)	1.6	1.3	1.5	3.5	2.5
Supply Current (nA)	54	68	37	2000	860
Temperature Coefficient (ppm/V)	425	1190	44	375	600

3.1.3 *Summary*

A high efficiency and low power current reference was designed, outputting a significantly constant current reference in the range of $9 - 12nA$. Compared to previous research, this circuit performs in the normal range, for its purpose, especially with the chosen technology.

The circuits presented a high correlation between analytical and simulation results. During simulations, a sensitivity analysis was performed and included, resulting in measured robustness. The proposed design is suitable for the polarization of low and ultra-low power consumption CMOS circuits. These are also suitable for low voltage operation. Additionally, the integration of the reference cell to CMOS circuit designs should be straightforward, even with already existing designs.

The circuit used CMOS technology, taking into advantage the sub-threshold region of CMOS transistors. The design as in mind energy harvesting interfaces and wireless sensor networks, although it has, likewise, applications for medical or personal mobile devices.

Extensive research was done in the circuit, with all the efforts, focusing on power consumption reduction and output stability. The final layout design is ready for fabrication, continuing the use of the CMOS technology chosen for the simulations. The future work of this project consists in the production testing of an integrated circuit, using the $0.35\mu m$ CMOS technology process, to demonstrate the circuit functionality in real-world applications, and comparison with the obtained results from the performed simulations.

3.2 CLASS AB OPERATIONAL AMPLIFIER

This section presents the study and the development for the design of an operational amplifier with AB class output stage using a minimum current maintenance circuit [45, 46] for the output transistors. The structure of the amplifier is straightforward, its power consumption is very low, and it can operate with supply voltages up to 1.5V in CMOS $0.35\mu m$ technology. The class AB control block is composed of a translinear circuit, whose

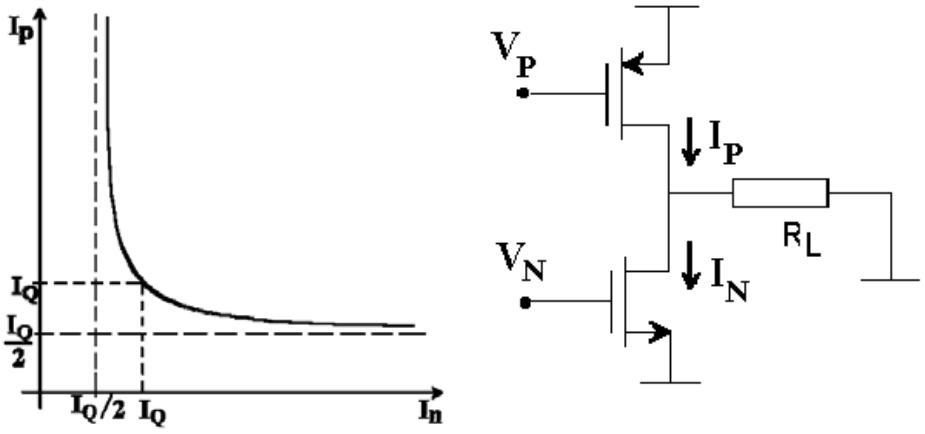


Figure 43: Common source output stage.

analysis and experimental results are presented in this section. The operation of the opamp, together with the simulation result are presented, followed by the layout, observing some basic rules for its preparation.

3.2.1 *Minimum current selector*

In the classical operation of an AB class output stage at least one of the output transistors cuts off. To achieve class AB control, where the minimum current in the output transistors is other than zero, it is essential to use non-linear function blocks that can be performed by a MOS translinear circuit. The relationship between the drain currents of the output transistors is shown in Fig. 56, where it can be observed that at the moment in which the current in the n-MOS transistor (I_N) is maximum the current in the p-MOS transistor (I_P) is minimum and approximately constant and vice-versa. The minimum current tends to be half the quiescent value. This current is necessary to keep the transistor driving while the other is supplying or absorbing the load current, The function presented in this figure is suitable for class AB operation, however, the relationship between quiescent current and minimum current need not necessarily be 2.

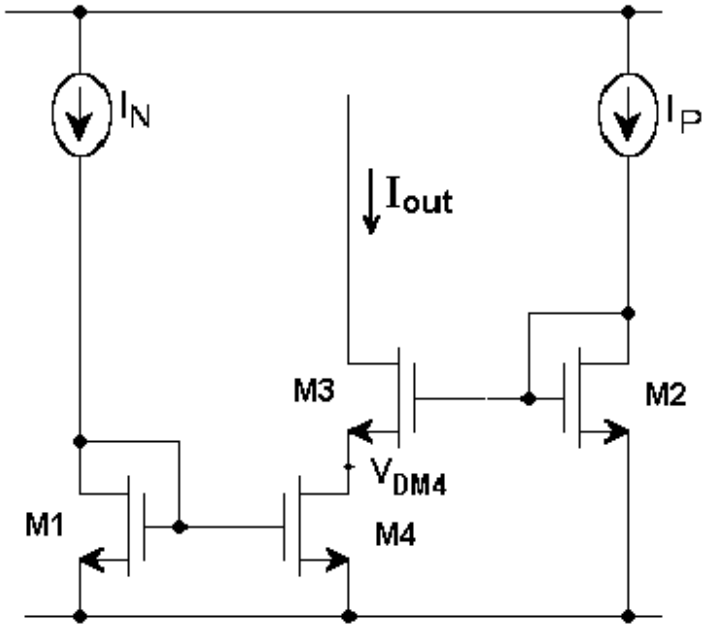


Figure 44: Translinear structure with minimum current.

There are several ways to implement the characteristic represented in Fig. 43. One of them is based on the minimum current selector circuit of Fig. 44 [46]. For the analysis of this circuit, assume that all transistors have the same geometry. When I N is much higher than I_P the voltage V_{DM4} tends to be very small. Thus, $V_{GSM3} \approx V_{GSM2}$ and the output current tends to be equal to I_P. When I N is much smaller than I_P the voltage V DM4 increases making $V_{GSM3} << V_{GSM2}$ and the output current approaches the value of I_N. Finally, when I_N and I_P are equal, the port voltages of M3 and M4 are the same, and the current at the output is equal to half of their value.

Figure 45 shows the circuit used for concept validation presented where again the aspect ratios of all transistors are equal. Current I_{DM2} was fixed at I_B. When I_N is much higher than I_B, the current I_P tends to be equal to I_B. When I_N approaches $2I_B$ to the current I_P tends to be equal to $2I_B$. When I_N is less than $2I_B$, I_P tends towards values higher than $2I_B$. Otherwise, when the currents I_P and I_N are equal, the voltage V_{GM3} is equal to V_{GM4}. M1 and M2 transistors behave as a series association of two transistors (compound transistor)

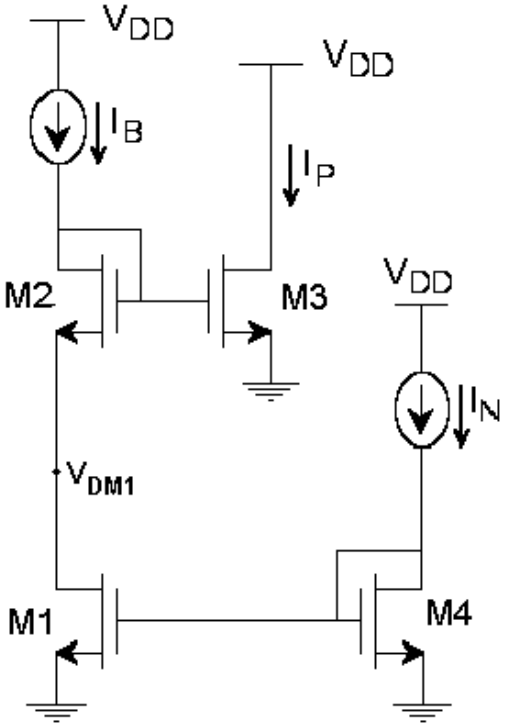


Figure 45: Minimum current circuit.

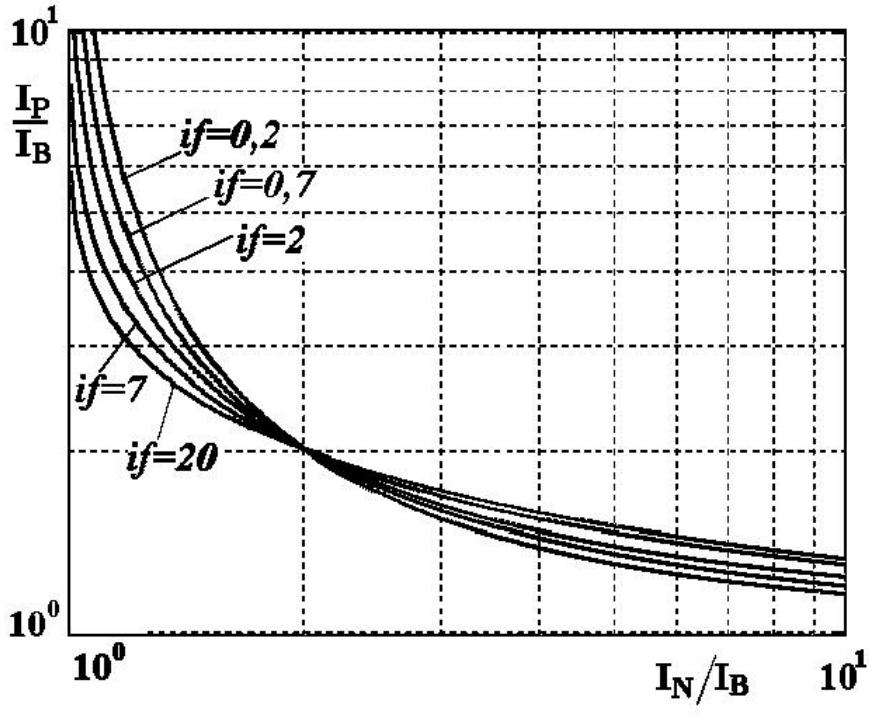


Figure 46: Simulated standard transfer characteristic.

where M2 saturated and M1 in the triode region, this compound transistor forms a mirror with M3 (M4), Fig. 45, but with half the aspect ratio of a single transistor.

The MOS translinear stage shown in Fig. 45 was simulated. The transistors have the same aspect ratio of 50/20. The results obtained are shown in Fig. 46. The simulations were performed for the inversion levels of $i_f = 0.2; 0.7; 2; 7; 20$. In Fig. 46 the I_P curves in function of I_N normalized with I_B are shown.

The intersection point in Fig. 46 represents $V_{GM1} = V_{GM2}$, therefore M1 and M2 form a composite transistor with duplicate L; thus, $I_P = I_N = 2I_B$. At the extremes, if I_N/I_B increases then $I_P = I_B$; when I_P/I_B increases then $I_N = I_B$. It is also observed that the higher the level of inversion, the more asymmetric the transfer characteristic becomes.

Out of the shelf IC packages with several MOS transistors was used for experimental purposes. The transistors used had aspect ratios of 18/5, $V_T = 0.6V$ and current $I_S = 200nA$. The circuit was supplied with 5V. Current I_B was fixed at the values shown below and for each current I_B value, I_N was varied from 1 to 10%.

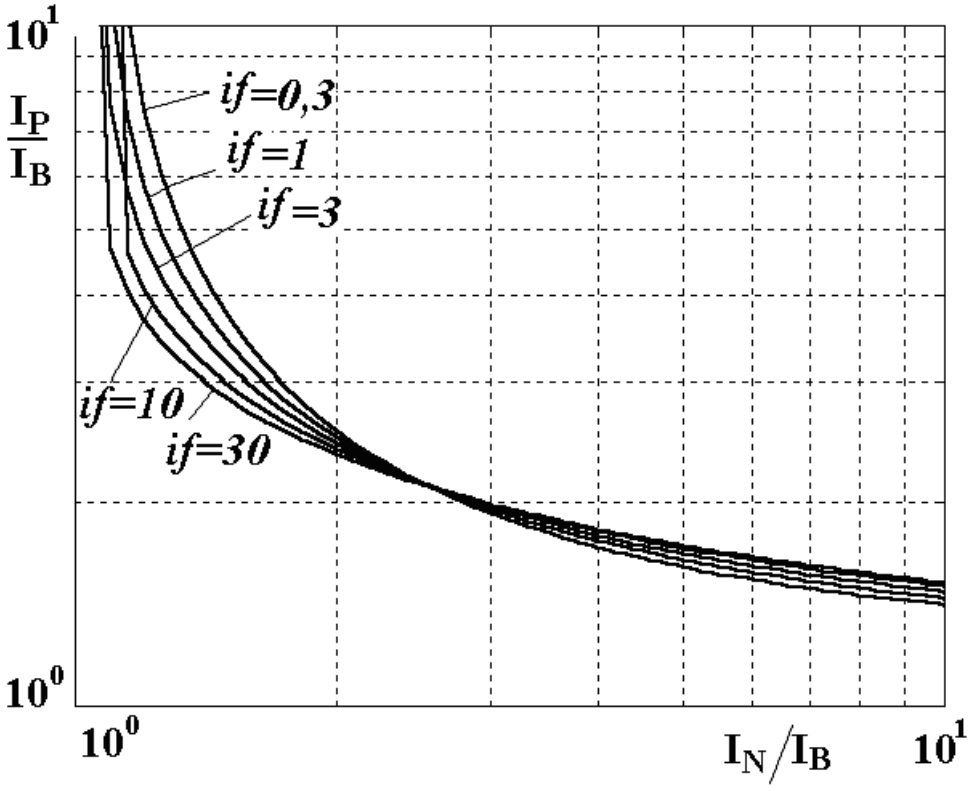


Figure 47: Experimental standard transfer characteristic.

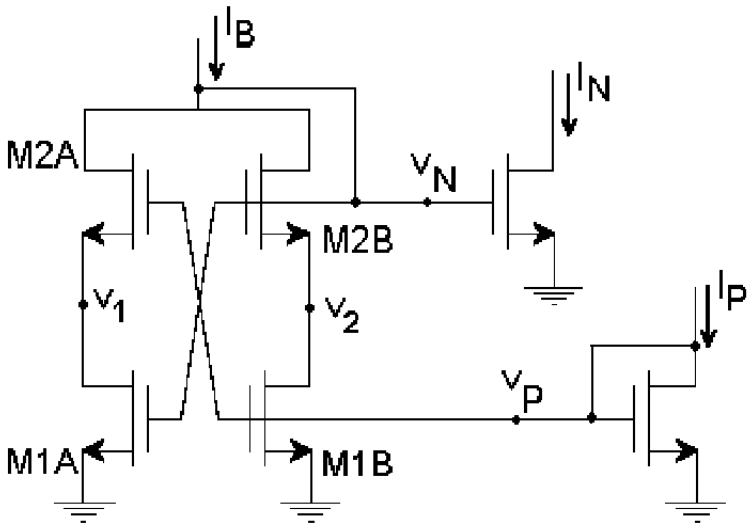


Figure 48: Modified translinear topology.

The experimental results are seen in Fig. 47. The results were very close, when compared to the simulation. The main difference is in the slight displacement of the crossing point between the curves, due to the mismatch between the transistors of the translinear circuit implemented. The discontinuity that appears in the upper left corner in i f =10 and i f =30 is due to the resolution of the measured values. Comparing the results of the simulation and the experimental performance, with the translinear function of Fig. 43, it can be concluded that the translinear circuit of Fig. 44 is adequate for the applications in class AB amplifiers. The minimum current selector circuit, as previously mentioned, has some asymmetry. To convert it into a symmetrical circuit, M1 and M2 can be divided into M1A, M1B and M2A, M2B, respectively, as shown in Fig. 48.

To prove this symmetry, an AC analysis of small signals in the circuit of Fig. 48 is performed. Consider all transistors with the same aspect ratio and that M2A and M2B are saturated. At the quiescent point where v_N and v_P are equal, the voltages v_1 and v_2 are calculated through equations (24) and (25), respectively.

$$v_1 = \frac{g_{mgM2A} v_P - g_{mgM1A} v_N}{2 g_{mdM1A}} \tag{24}$$

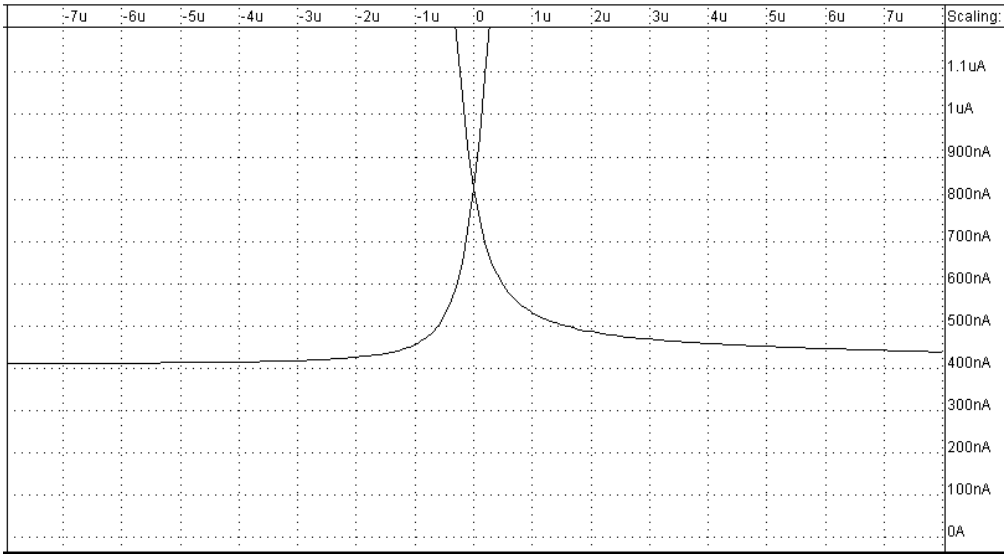


Figure 49: Simple minimum current output stage simulated current.

$$v_2 = \frac{g_{mgM2B} v_N - g_{mgM1B} v_P}{2 g_{mdM1B}} \tag{25}$$

Where g_{mgM1A}, g_{mgM2A}, g_{mgM1B}, g_{mgM2B}, g_{mdM1A} and g_{mdM1B}, are the gate conductivity. Drainage of M1A, M2A, M1B and M2B transistors, respectively. $g_{mgM1A} = g_{mgM1B}$, where g_{mdM1A} is the drain conductance of M1A and g_{msM2A} is the source conductance of M2A. As the dimensions of the transistors are the same, then $g_{mgM1A} = g_{mgM1B}$, $g_{mgM2A} = g_{mgM2B}$ and $g_{mdM1A} = g_{mdM1B}$. If $I_P = -I_N$ we have $v_N = -v_P$, and through the equations (24) and (25) we have to $v_1 = v_2$. The behaviour for small signals of the two output currents are symmetrical as expected, for the minimum current selector circuit.

Figure 49 shows the result of the circuit without division of the transistors and Fig. 50 shows the result with the modified circuit. These figures show the symmetry between the output currents for an AB class amplifier with the suggested changes.

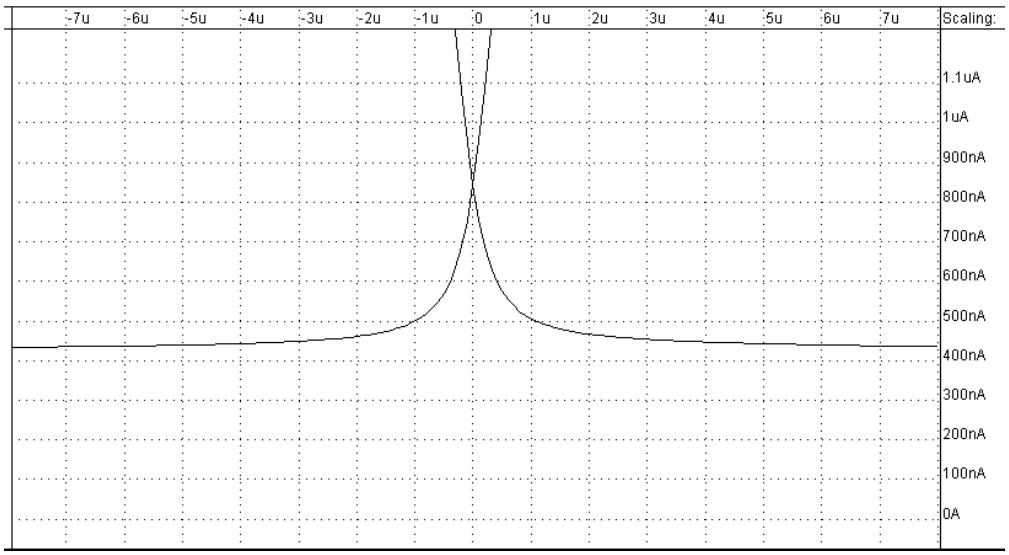


Figure 50: Modified minimum current output stage simulated current.

3.2.2 *Proposed amplifier circuit*

Our AB class opamp structure with feedback loop is based on [29]. Comparing the structure presented in [29], see Fig. 26, with the structure proposed in this work, Fig. 51 and 52, it can be seen that basically the same ideas were used. The lagging circuit (M7 and M8) was used to generate a lag of 180°in one of the outputs of the first stage. The *Common Mode Feedback (CMFB)* control is performed by the minimum current translinear circuit seen in the previous section and the reference voltage V_D of Fig. 32 is fixed by the voltages V_GS of the transistors M7 and M26, Fig. 51 and 52, and the voltage VSS. The innovation factor is the CMFB circuit, which in our case is represented by the polarization circuit, Fig. 51, which in addition to polarization purposes, it controls the class AB operation of the circuit. The proposed circuit simplifies the design and does not require additional sources to polarize the class AB control circuit.

The main requirements of the opamp to be designed are:

1. Low supply voltage. Current integrated circuit technologies require low supply voltage.

2. RC load. It is essential that the quiescent current is low for low static dissipation.

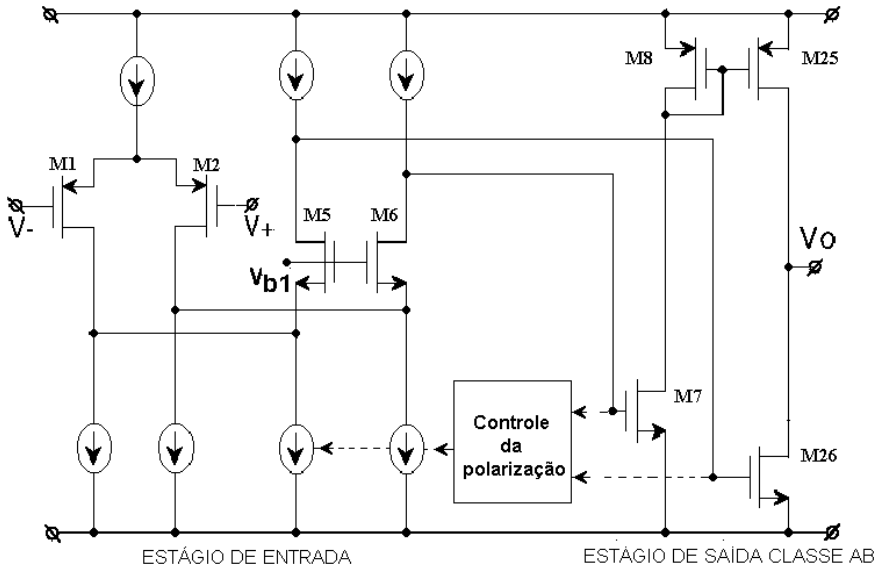


Figure 51: Principle of the AB class compact amplifier.

3. Ensure minimum current (I_{min}) on the inactive output transistor. In the AB class amplifier, a minimum current must be guaranteed to avoid delays when the non-active transistor is requested again.

4. Constant common mode voltage at the input. The input stage does not need to be rail-to-rail (rtr) for the proposed application (inverter amplifier).

5. As a consequence of the low voltage it is indispensable to have rtr in the output to not have significant reduction of the dynamic range.

6. Meet the requirements of the stabilization time. It depends on the switching frequency (less than 5 ms for 50kHz switching frequency).

The p-channel transistor was chosen for the differential input stage of the opamps because the switches and resistors (formed by transistors), used in the switched MOSFET technology, will be of n-channel operating with common mode voltage close to the negative supply voltage.

The proposed opamp, Fig. 52, consists of two stages plus the class AB control circuit. The first stage is formed by a differential amplifier (M1 and M2) with cascode output (M3-M6)

providing high voltage gain. The second is a push-pull amplifier (M25 and M26) operating in AB class performing the nonlinear function shown in Fig. 43. The class AB control circuit is formed by two *Minimum Current Selector Circuit (MCSC)* [47], constituted by the M10-M13 and MD10-MD13 transistors. Two MCSCs are used to maintain symmetry in the structure. However, it is possible to use only one MCSC. Each MCSC circuit is divided into two to improve the symmetry of the currents in the output transistors, see Fig. 48. M7 and M8 transistors are used to generate a lag of 180°in one of the first stage output voltages to control the M25 output transistor. When voltages V_{DM5} and V_{DM6} are equal, that is, when the input voltages are equal, the output current is zero and the quiescent current in the output transistors is given by:

$$I_{Q26} = I_B \frac{W_{26}/L_{26}}{W_{11}/L_{11}} \tag{26}$$

$$I_{Q25} = I_B \frac{W_7/L_7}{W_{11}/L_{11}} \frac{W_{25}/L_{25}}{W_8/L_8} \tag{27}$$

When the voltage V+ ¿ V-, V8 tends to remain approximately constant while V10 tends to follow the increase of V+. This is due to the operation of the MCSC circuit. The current in M26 remains approximately constant and equal to I min, while the current in M25 increases with the increase of V+ tending to I max. The M10-M13 and MD10-MD13 transistors (with the same aspect ratios) fix the minimum current in the output transistors equal to half the quiescent output current. The minimum supply voltage for this amplifier is $V_{GS} + 2V_{Dssat}$. This circuit does not require additional current sources for the polarization of the class AB control circuit. The problem that this circuit presents is the asymmetry imposed by the lagging circuit M7-M8.

For the amplifier design the parameters of CMOS 0.35 um technology were used [48]. The simulations were performed with the SPICE simulator and ACM model [12].

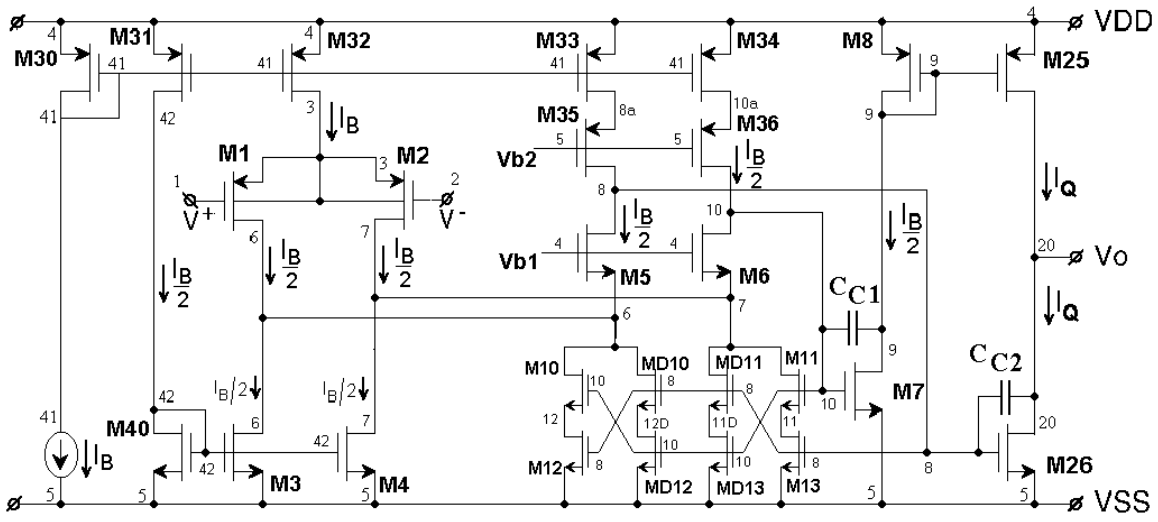


Figure 52: Amplifier with minimum current class AB control.

The minimum current class AB amplifier is designed with the requirements: unit gain frequency of 1MHz for application in the audio range, hold capacitor $C_H = 5pF$ and load conductance given by equation (28).

$$g_L = \mu_n C'_{ox} n \frac{W}{L}(V_p - V_S) \tag{28}$$

Where the aspect ratio for load transistors is equal to $10mm/20mm$, the gate voltage is VDD , the source voltage is VX , and the slope factor n = 1.3. With equation (28), $g_L = 17mS$. The values of C_H and g_L were chosen to satisfy requirements regarding noise, stabilization time and conduction ratio of the switch/(conductance of the load transistor), which must be very small to reduce the influence of non-ideal switch on the transient response. The selection process was iterative. To have an idea, the keys have to have minimum dimensions for minimum load injection, where the length of the channel is the minimum possible and W greater than L to reduce the value of the channel resistance. Due to this, the load transistors must have a W/L ratio, such that their resistance is large compared to that of the switches.

By establishing that the zero frequency of the open loop opamp is approximately 10 times greater than the unit gain frequency, g_{mI} , transconductance of the differential input stage is

obtained. For the input stage with g_{mI}, the minimum current (I_{Bmin}) can be determined to satisfy this transconductance through equation (29) [34] with i f ¡¡ 1 (very weak inversion condition). Thus, $I_{Bmin} = 0,5mA$. The value adopted for the project was 0.6 m A. With this value of current I B , the level of inversion of the transistors of the differential pair i f1.2 = 1 is determined.

$$I_D = n\phi_t g_m \left(\frac{1 + \sqrt{1 + i_f}}{2} \right) \tag{29}$$

$$\frac{W}{L} = \frac{g_m}{\mu C'_{ox} \phi_t} \left(\frac{1}{\sqrt{1 + i_f} - 1} \right) \tag{30}$$

$$\frac{W}{L} = \frac{I_B}{I_{SQ} i_f} \tag{31}$$

With equation (30) and the inversion level obtained previously, the value of the aspect ratio of the transistors of the input differential pair is determined. The minimum quiescent current ($I_Q min$) of the second stage ("push-pull" stage) is also determined by equation (30) [34] where $gm = gmII/2$ and $i_f < 1$. The value of $I_Q min = 1.1mA$ was found. The value adopted for I_Q is 1.5 mA giving twice the inversion level of the input stage. With this level of inversion and with the value of the quiescent current the aspect ratios of the output transistors were determined.

The aspect ratios of the M30 and M32 polarizing transistors are determined using equation (31) [34] with $IB = 0.6mA$ and $i_f = 0$ to maintain a compromise between occupied area and power consumption. The aspect ratios of M31, M33, M34, M21 and M22 transistors are half the aspect ratio of M30. For the M3-M6 and M40 transistors, the level of inversion of the second stage (if = 2) and current IB/2 were used.

For the transistors that compose the MCSC circuits of the proposed opamp, their aspect ratios are given by equation (32),

$$\frac{W}{L}_{10-13} = \frac{7}{2} \tag{32}$$

Transistor	W/L	i_f
M1,2	38/2	1
M25	95/2	2
M26	35/2	2
M3,4,5,6,40	14/4	2
M31,33-36	8/4	10
M7,10-13	7/2	2
M8	19/2	2
M30,32	16/4	10

Table 4: Aspect ratios and inversion levels of the transistors of the AB amplifier.

The aspect ratio of the M7 transistor must be equal to the aspect ratio of the MCSC circuit transistors. The aspect ratio of the M8 transistor is given by equation (33),

$$\frac{W}{L}_8 = \frac{I_B/2}{I_Q}\frac{W}{L}_{25} \tag{33}$$

The compensation capacitor C2 was determined using equation (A3.13) with the values GBW and g mI . While C1 was determined, where C1 = C2 /2. The values of the compensation capacitors are C1 = 0.5pF and C2 = 1pF. The channel lengths (L) were chosen close to the minimum value of the technology (0.8um) to reduce the area occupied. Table 4.1 shows the aspect ratios of the transistors in Fig. 52 for the application described in this work, together with their respective levels of inversion.

To obtain the voltages Vb1 and Vb2, Fig. 52, the polarization circuit presented in chapter 3 can be used. However, these voltages were made equal to V DD and V SS , respectively, in order to simplify and reduce power consumption. For the design values (load transistor and feedback with values of $10mm/20mm$) $I_Dmax = 3.5mA$. Thus, the opamp must supply at least twice this current.

The maximum current at the opamp output is limited by the maximum signal excursion at nodes 8 and 10 when there is no limitation at the voltage signal excursion at the output. Another limitation for the maximum current at the output occurs on the M7 transistor. When the current at M25, Fig. 52, tends to increase, the current at M7 and M8 also increases. The voltage at the M7 port increases and the voltage drop on the M8 transistor increases,

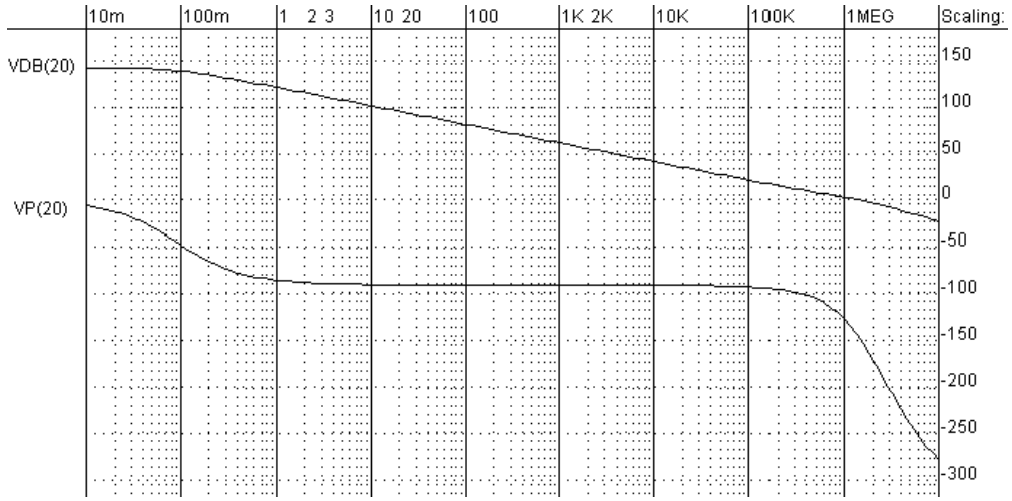


Figure 53: AC characteristic of AB class opamp. Simulated.

decreasing the V DS voltage of M7 tending to take this transistor out of saturation (Appendix 4), restricting the increase of the current at the output.

The projected circuit was simulated with SPICE using the ACM model [12]. Through the DC characteristic of the open loop opamp, a systematic offset voltage of 32nV was verified. Fig. 53 shows the AC characteristic of the open loop. The gain at low frequencies is 140dB.

Figure 54 presents the DC characteristic of the amplifier with input current source I in varying from ± 6 m A and voltage V X, equation (1.6), equal to -0.6V. This figure shows the currents of the M25 and M26 transistors internal to the opamp. The quiescent current is around 1.6 m A and the minimum value tending to 0.8 mA.

The breakpoints around 10 mA are caused by the maximum limitation of the voltage excursion at the opamp output. That is, with the current around 4.5 mA in the load transistors the output voltage tends to saturate. The maximum current that the opamp, designed here, can provide is approximately 95 mA. If we think about optimizing the opamp so that its maximum output current is approximately twice the maximum current at the load (I Lmax), we will be limited by the value of g_m, that is, to reduce I Lmax we must reduce IQ. If IQ is reduced, g_m will also reduce and, consequently, increase the stabilization time that is a fixed parameter by design.

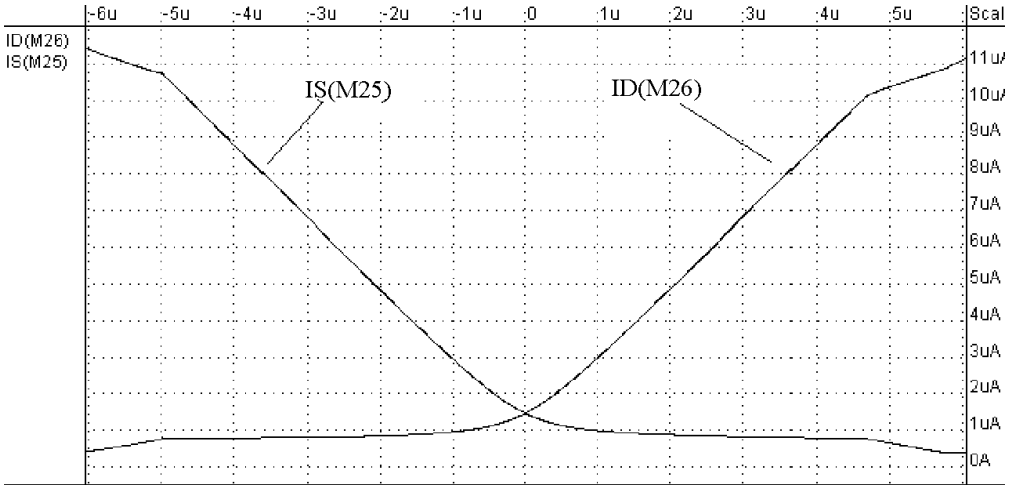


Figure 54: DC characteristic of the amplifier.

In Fig. 55 we have the transient response. Voltages V20 and V54 represent the output voltage and the input voltage respectively. A square wave was applied with a frequency of 50kHz and amplitude of ± 0.01V with a DC level equal to V_X . The output signal stabilized with an error of less than 0.4% after 4 ms of application of the input signal.

The dominant noise sources for MOS transistors are flicker noise and thermal noise. Flicker noise is modeled by a voltage source in series with the value transistor port,

$$S_f = \frac{KFg_{mg}^2}{WLC'_{ox}f} \tag{34}$$

where KF is a technology-dependent flicker noise constant. Note that the spectral density of noise (voltage) referred to the input, equation (34), is dependent on g mg , consequently, the polarization current. The effect of this noise is significant at low frequencies. For the desired frequency range the predominant noise is thermal noise.

Thermal noise is modeled by a current source between the drain and the MOS transistor source. The spectral density for thermal noise (current) in MOSFET is valid from weak to strong inversion [35] is given by,

$$S(f) = \frac{-4\beta\mu_n Q_I}{L^2} \tag{35}$$

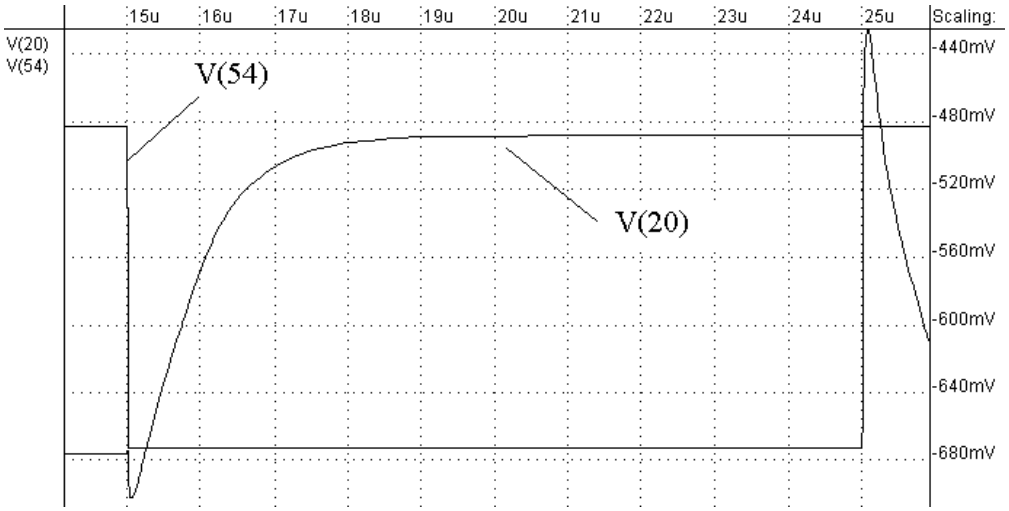


Figure 55: Transient response of circuit.

where Q_I is the total reversal load, $\beta = kT$, k is the Boltzmann constant and T is the absolute temperature. Through the equation (35), it can be observed that the thermal noise in a MOSFET is the same as that produced by a conductance $G_{N,th}$ whose value is

$$G_{N,th} = \frac{\mu_n Q_I}{L^2} = g_{ms} \frac{Q_I}{Q'_{IS} WL} \tag{36}$$

where Q'IS is the inversion load density at the source. In the linear region, the inversion load density is almost uniform, so $Q'_{IS} \approx Q_I/WL$ and the $G_{N,th}$ conductance equals the source transconductance. In saturation, we have that the relationship between $G_{N,th}$ and g_{ms} is given by $G_{N,th} = g_{ms}/2$ in weak inversion and $G_{N,th} = 2g_{ms}/3$ in strong inversion. For the precise calculation of thermal noise, one can refer to [35]. However, for the calculation of thermal noise in the linear region or its estimation in saturation, it can be used,

$$S_I(f) \approx 4\beta g_{ms} \tag{37}$$

$$S_V(f) \approx \frac{4\beta}{g_{ms}} \tag{38}$$

Let's analyze the behaviour of the AB class opamp, Fig. 63. The greatest contribution is given by the input stage, differential amplifier with folded cascode output. The noise is not correlated. The effect of the noise produced by M32 is divided between the M1 branch and the M2 branch, these two contributions are subtracted in the output. The noise contribution of M5, M6, M35 and M36 transistors is negligible compared to the rest of the first stage transistors. The M12, MD12, M13 and MD13 transistors are in the linear region and their contributions to the output is similar to the M10, MD10, M11 and MD11 transistors that have their noise portions given by the equation (38) with the g ms referring to each transistor. For the M1-M4, M33 and M34 transistors, the noise portion at the output is similar to those of the class AB control circuit transistors. The class AB control circuit has its behaviour, in polarization, similar to that of the M33 and M34 transistors.

The results obtained using the SPICE simulator are presented below. This simulation was performed with open loop opamp and 5pF load capacitor. The frequency ranged from 0.1Hz to 10MHz. In Fig. 56 we have the total noise in $V/\sqrt{Hz}$ where it can be observed the great influence of noise 1/f up to approximately 100Hz and above predominating the thermal noise.

For noise at 1kHz the output noise voltage is $50nV^2/Hz$ or $225\mu V/\sqrt{Hz}$, Fig. 57. For this frequency the gain is approximately 61 dB. The reflected noise voltage for the input is

- The integral noise output in the 1Hz to 10kHz band is 1.8V (-5.2dB).
- The integral input noise in the 1Hz to 10kHz band is 19 m V (-94.5dB).
- The integral noise output in the 10Hz to 10kHz band is 0.37V (-8.6dB).
- The integral input noise in the 10Hz to 10kHz band is 17 m V (-95dB).
- The integral noise output in the 100Hz to 10kHz band is 0.04V (-28dB).
- The integral noise input in the 100Hz to 10kHz band is 15 m V (-96dB).

In closed loop , the integral noise at the output, in the range of 100Hz to 10kHz, is $30\mu V$. Therefore, knowing that the maximum voltage excursion at the output is 0.1V, the dynamic range will be 70dB.

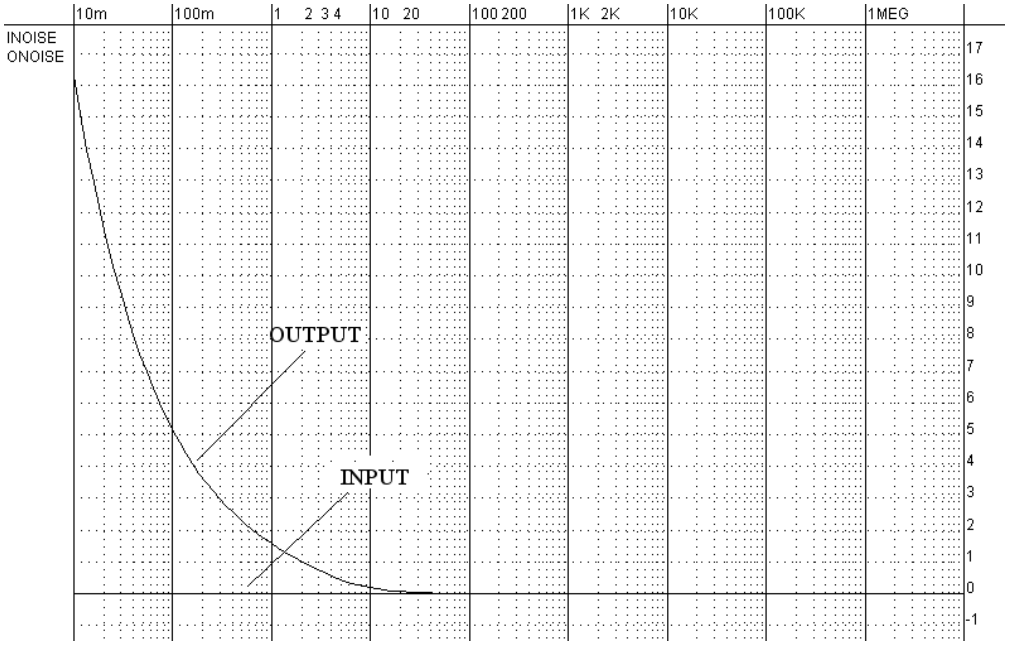


Figure 56: Noise spectral density in V/Hz.

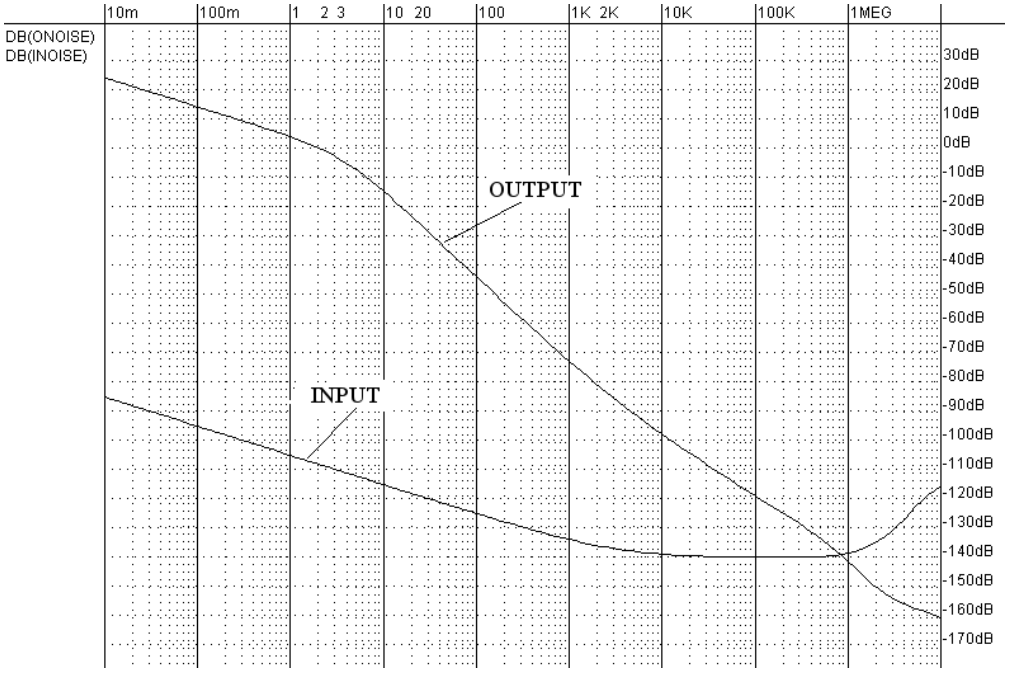


Figure 57: Noise spectral density in dB.

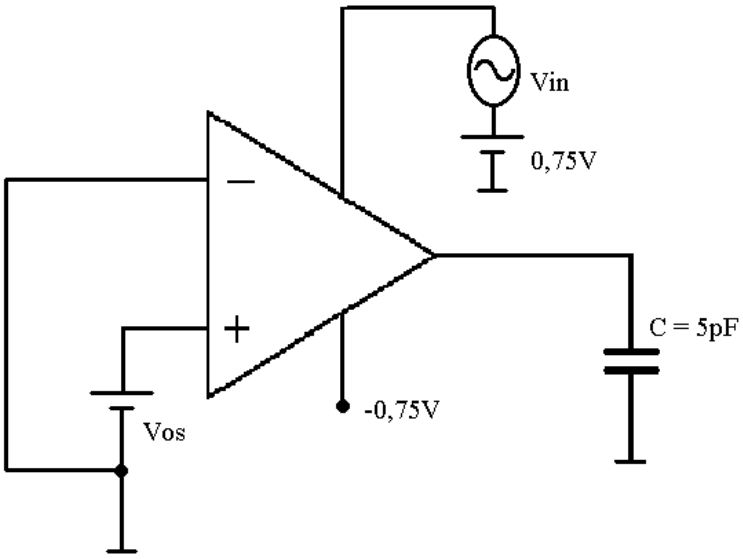


Figure 58: Circuit used for PSRR simulation.

To measure the PSRR the circuit of Fig. 58 was used. Fig. 59 shows the magnitude in the opamp output for the source VDD. The value of the $PSRR_{VDD}$ is shown in Fig. 60 where the PSRR remains constant and equal to 110dB up to approximately 1Hz. Then, it presents a drop of 20dB per decade until close to the unit gain frequency of the opamp.

$$PSRR_{VDD} = \frac{A_V}{A_{VDD}} \tag{39}$$

The configuration used for the simulation of the PSRR was the same as before with the application of the signal variation in the power supply. Fig. 61 shows the magnitude (dB) at the output with respect to the V SS source under the same previous conditions. In this figure, the gain remains constant and equal to -6dB from 10Hz to approximately 100kHz. In Fig. 62 we have the PSRR where it is observed that in DC its value is equal to 130dB and falls with approximately 20dB/dec until close to the unit gain frequency of the opamp.

To obtain, by simulation, the common mode rejection ratio (CMRR), open loop opamp with offset compensation was used. The CMRR value for low frequencies was 150dB, Fig. 63.

To obtain the output impedance, the opamp was simulated in open mesh with grounded inputs and offset compensated, a current source was applied to the opamp output and

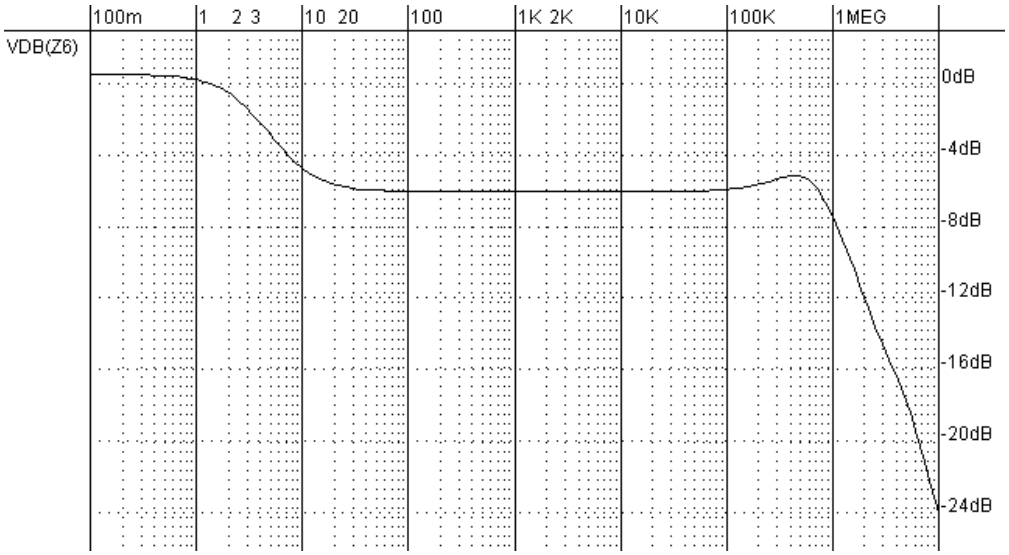


Figure 59: Open loop gain referred to VDD supply.

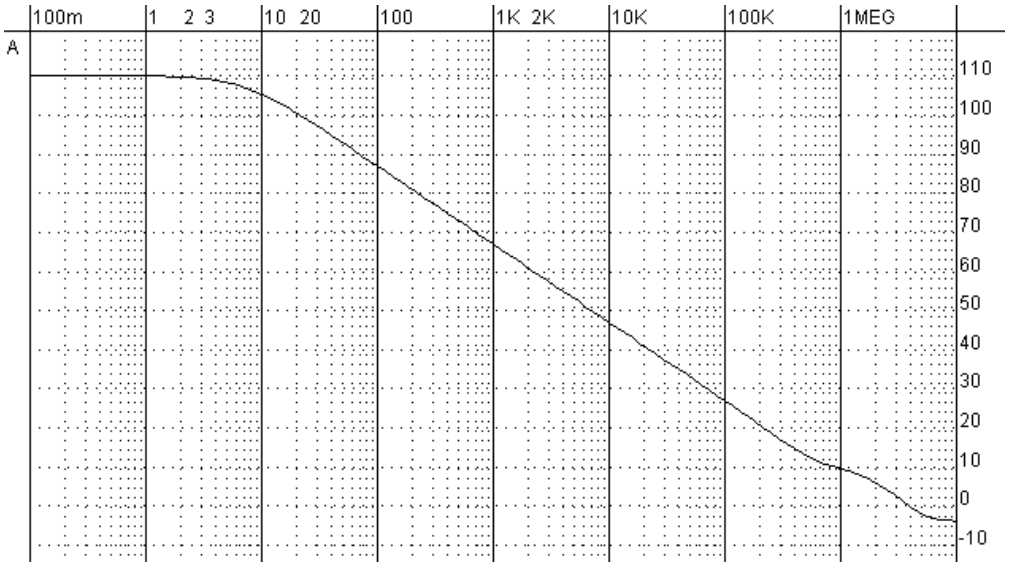


Figure 60: opamp PSRR for VDD supply.

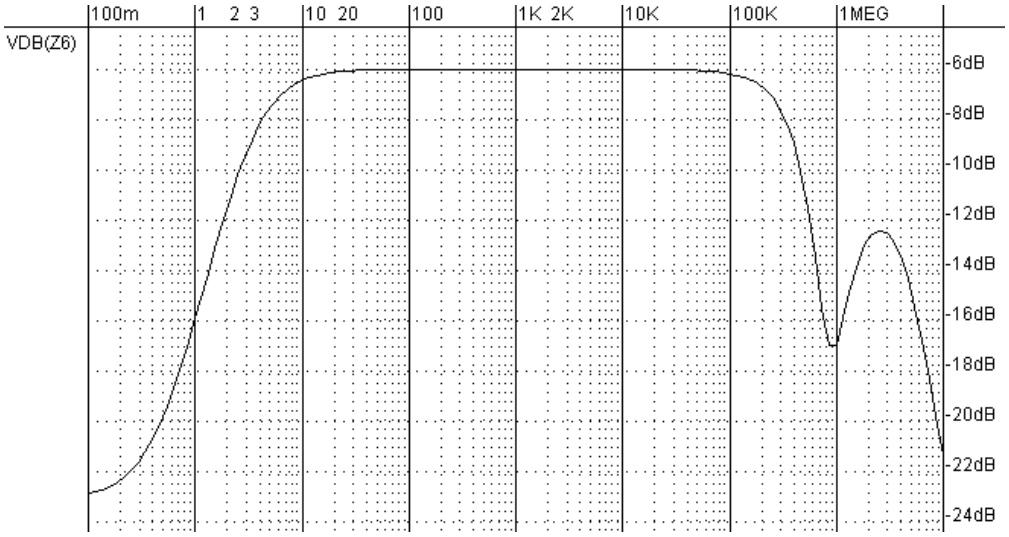


Figure 61: Open loop gain for to VSS supply.

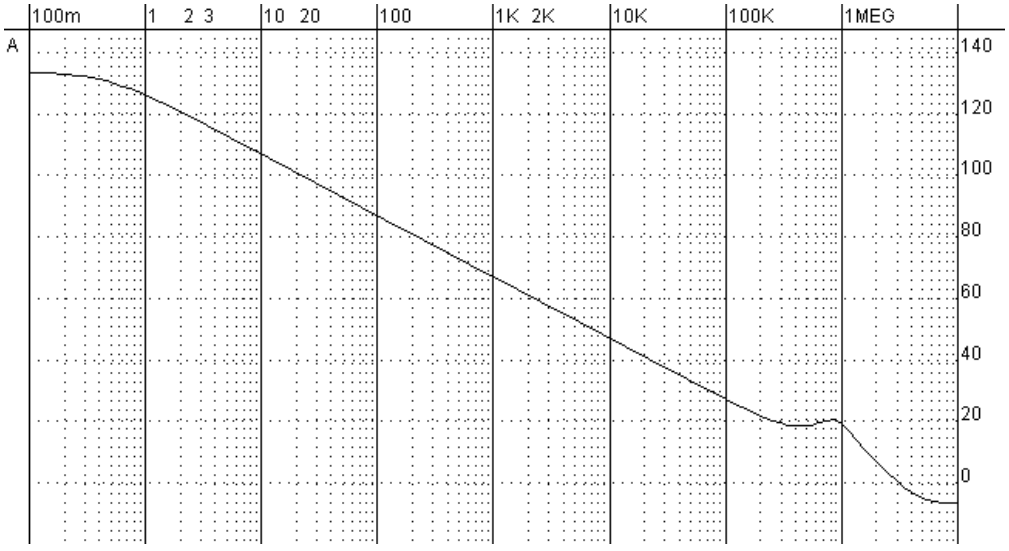


Figure 62: opamp PSRR for VSS supply.

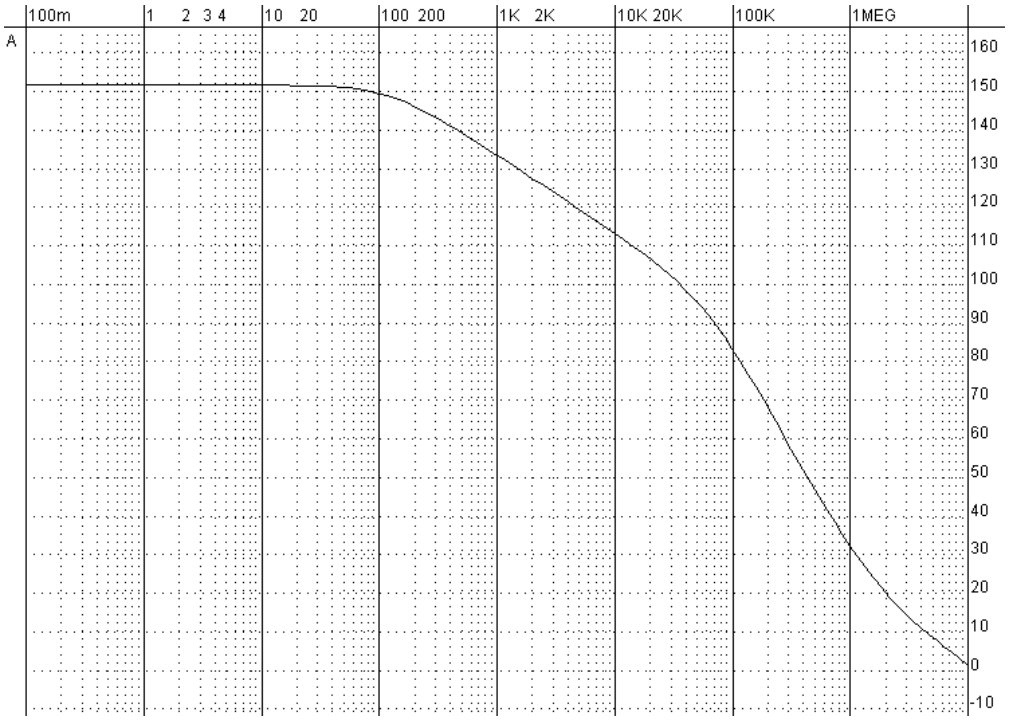


Figure 63: Simulation of the CMRR of class AB opamp.

voltage measured. The relationship of the applied current to the measured voltage provides the desired impedance.

By analyzing the operating point, the conductivity values of the output transistors are, g ds25 @ g ds26 @ 100nS. The inverse of the sum of these two conductances, in dB, provides the DC output impedance shown in Fig. 64. The admittance for the opamp was determined in section A3.2.2.

Figure 65 shows the output impedance of the circuit, where it can be observed that for 1kHz frequency the output impedance is approximately 70Ω.

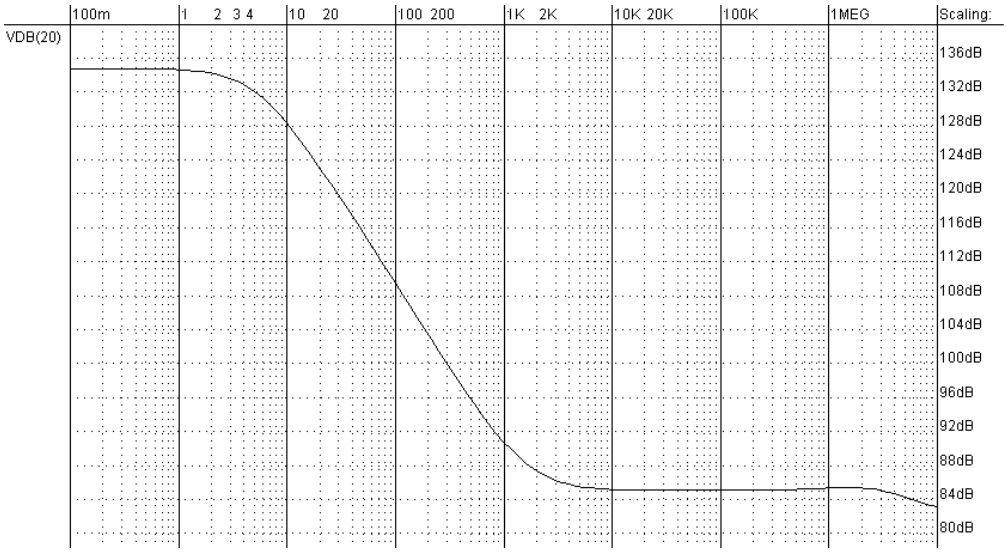


Figure 64: Open loop output impedance.

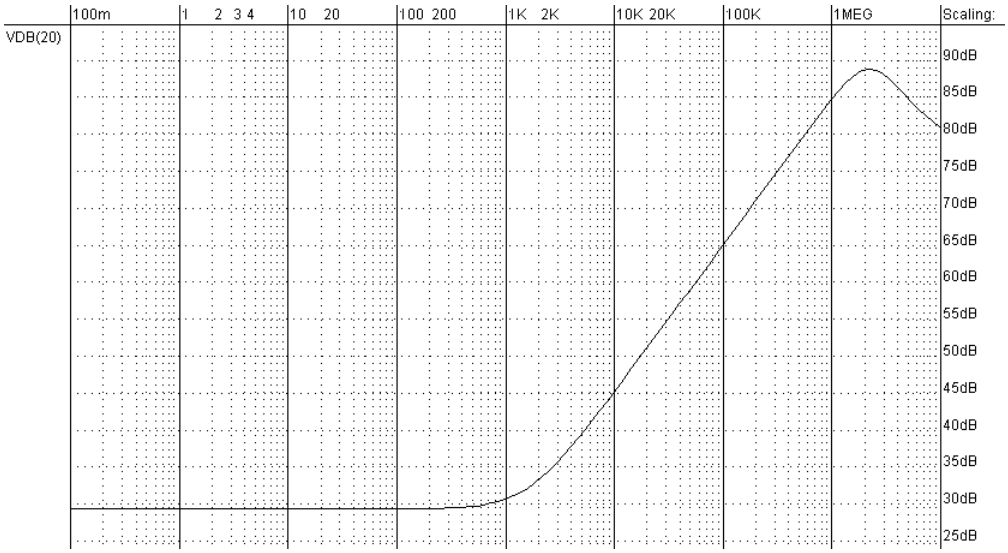


Figure 65: Closed loop output impedance.

4

CONCLUSION

4.1 CONCLUSIONS

Energy harvesters for low power electronics have been popular over the past few years. Researches in integrated, all-in-one, energy scavenging devices is at the forefront of cutting-edge technology. This research thesis may contribute to the advance of high efficiency integrated energy extraction circuits.

The present work presents two main substantial contributions. Firstly, the self-biased current reference, based on the multiple topologies. It has been verified to be very useful for applications requiring temperature variation compensation and power supply voltage independence. The high efficiency and low power current reference was designed, outputting a significantly constant current reference in the range of $9 - 12nA$. The circuits presented a high correlation between analytical and simulation results. During simulations, a sensitivity analysis was performed and a good robustness is demonstrated. The proposed design is suitable for the polarization of low or ultra-low power consumption CMOS circuits. The present current reference is also suitable for low voltage operation. Additionally, the integration of the reference to CMOS circuit designs should be straightforward, even with already existing designs.

Secondly, the AB class operational amplifier is proposed, including a translinear circuit for maintaining the minimum current of the output stage. The present operational amplifier is designed with efficient quiescent current control; the maintenance of minimum output

current is carried out via the minimum current selector circuit. The simulation results show that the design is suitable for the development of low power applications.

Extensive research was done in the circuit focusing on power consumption reduction and output stability. The final layout design is prepared for fabrication, which allows for further studies and improvements. The design has in mind an integrated energy harvesting extraction interface for wireless sensor networks devices. Also it has, likewise, applications for other scientific or personal mobile devices, which have low power requirements.

4.2 PROSPECT FOR FUTURE WORK

In the future, more circuit components necessary for the harvesting interface circuit will be developed. These components will follow the same baselines as the present ones, continuing the low power and high-efficiency methodology. Consequently, it is expected to fully produce a IC, including the full energy harvester extraction circuit. After being fabricated, the IC using the $0.35\mu m$ CMOS technology process will be tested in the real piezoelectric energy harvester. The test results will be compared with the simulation results.

The novel IC will allow for easy and cheap integration in existing devices, simplifying the assimilation of energy harvester transducers into current technology. According to the explored research, fully integrated energy harvesting devices are the step forward in the future technological portable world.

BIBLIOGRAPHY

Mohab Anis and Mohamed Elmasry. *Multi-Threshold CMOS Digital Circuits Managing Leakage Power*, volume 3. Springer, 2003.

Steven R Anton and Henry A Sodano. A review of power harvesting using piezoelectric materials (2003–2006). *Smart materials and Structures*, 16(3):R1, 2007.

Hironori Banba, Hitoshi Shiga, Akira Umezawa, Takeshi Miyaba, Toru Tanzawa, Shigeru Atsumi, and Koji Sakui. A cmos bandgap reference circuit with sub-1-v operation. *IEEE Journal of Solid-State Circuits*, 34(5):670–674, 1999.

Edgar Mauricio Camacho-Galeano, Carlos Galup-Montoro, and Márcio Cherem Schneider. A 2-nw 1.1-v self-biased current reference in cmos technology. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(2):61–65, 2005.

Patrik Cerwall, P Jonsson, R Möller, S Bävertoft, S Carson, and I Godor. Ericsson mobility report. *On the Pulse of the Networked Society. Hg. v. Ericsson*, 2015.

Anantha P Chandrakasan and Robert W Brodersen. Minimizing power consumption in digital cmos circuits. *Proceedings of the IEEE*, 83(4):498–523, 1995.

Anantha P Chandrakasan, Samuel Sheng, and Robert W Brodersen. Low-power cmos digital design. *IEICE Transactions on Electronics*, 75(4):371–382, 1992.

Jiwei Chen and Bingxue Shi. 1v cmos current reference with 50 ppm/° c temperature coefficient. *Electronics Letters*, 39(2):1, 2003.

Myungjoon Choi, Inhee Lee, Tae-Kwang Jang, David Blaauw, and Dennis Sylvester. A 23pw, 780ppm/° c resistor-less current reference using subthreshold mosfets. In *European Solid State Circuits Conference (ESSCIRC), ESSCIRC 2014-40th*, pages 119–122. IEEE, 2014.

Bijan Davari, Robert H Dennard, and Ghavam G Shahidi. Cmos scaling for high performance and low power-the next ten years. *Proceedings of the IEEE*, 83(4):595–606, 1995.

Giuseppe De Vita and Giuseppe Iannaccone. A 109 nw, 44 ppm/° c cmos current reference with low sensitivity to process variations. In *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pages 3804–3807. IEEE, 2007.

Francesco Dell'Anna, Tao Dong, Ping Li, Wen Yumei, Zhaochu Yang, Mario R Casu, Mehdi Azadmehr, and Yngvar Berg. State-of-the-art power management circuits for piezoelectric energy harvesters. *IEEE Circuits and Systems Magazine*, 18(3):27–48, 2018.

Quanzhen Duan and Jeongjin Roh. A 1.2-v 4.2-ppm c high-order curvature-compensated cmos bandgap reference. *IEEE Transactions on Circuits and Systems I: regular papers*, 62(3): 662–670, 2015.

Mohan V Dunga, C-H Lin, Xuemei Xi, Darsen D Lu, Ali M Niknejad, and Chenming Hu. Modeling advanced fet technology in a compact model. *IEEE Transactions on Electron Devices*, 53(9):1971–1978, 2006.

Christian C Enz and Eric A Vittoz. Cmos low-power analog circuit design. In *Emerging Technologies: Designing Low Power Digital Systems*, pages 79–133. IEEE, 1996.

Franco Fiori and Paolo Stefano Crovetti. A new compact temperature-compensated cmos current reference. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 52(11):724–728, 2005.

Carlos Galup-Montoro, Márcio Cherem Schneider, Ana Isabela Araújo Cunha, F Rangel de Sousa, Hamilton Klimach, and O Franca Siebel. The advanced compact mosfet (acm) model for circuit analysis and design. In *2007 IEEE Custom Integrated Circuits Conference*, pages 519–526. IEEE, 2007a.

Carlos Galup-Montoro et al. *MOSFET modeling for circuit analysis and design*. World scientific, 2007b.

Julius Georgiou and Christofer Toumazou. A resistorless low current reference circuit for implantable devices. In *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, volume 3, pages III–III. IEEE, 2002.

John B Goodenough and Kyu-Sung Park. The li-ion rechargeable battery: a perspective. *Journal of the American Chemical Society*, 135(4):1167–1176, 2013.

Fredrik S Gr, João CG Simóes, Helene Berntsen, Lars E Roseng, Tao Dong, et al. Low power consumption device for biological stability monitoring in drinking water. In *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*, pages 3841–3844. IEEE, 2018.

Tetsuya Hirose, Yuji Osaki, Nobutaka Kuroki, and Masahiro Numa. A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities. In *ESSCIRC, 2010 Proceedings of the*, pages 114–117. IEEE, 2010.

Hong-Wei Huang, Chun-Yu Hsieh, Ke-Horng Chen, and Sy-Yen Kuo. A 1v 16.9 ppm/° c 250na switched-capacitor cmos voltage reference. In *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*, pages 438–626. IEEE, 2008.

Kwok K Hung, Ping K Ko, Chenming Hu, and Yiu C Cheng. A unified model for the flicker noise in metal-oxide-semiconductor field-effect transistors. *IEEE Transactions on Electron Devices*, 37(3):654–665, 1990.

Paul Jespers. *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*. Springer Science & Business Media, 2009.

David A Johns and Ken Martin. *Analog integrated circuit design*. John Wiley & Sons, 2008.

Kanika Kaur and Arti Noor. Strategies & methodologies for low power vlsi designs: a review. *International Journal of Advances in Engineering & Technology*, 1(2):159, 2011.

C-H Lee and H-J Park. All-cmos temperature independent current reference. *Electronics Letters*, 32(14):1280–1281, 1996.

Jong Mi Lee, Youngwoo Ji, Seungnam Choi, Young-Chul Cho, Seong-Jin Jang, Joo Sun Choi, Byungsub Kim, Hong-June Park, and Jae-Yoon Sim. 5.7 a 29nw bandgap reference circuit. In *Solid-State Circuits Conference-(ISSCC), 2015 IEEE International*, pages 1–3. IEEE, 2015.

Ka Nang Leung and Philip KT Mok. A sub-1-v 15-ppm//spl deg/c cmos bandgap voltage reference without requiring low threshold voltage device. *IEEE Journal of Solid-State Circuits*, 37(4):526–530, 2002.

Ping Li, Yumei Wen, Chaobo Jia, and Xinshen Li. A magnetoelectric composite energy harvester and power management circuit. *IEEE Transactions on Industrial Electronics*, 58(7): 2944–2951, 2011.

Ping Li, Yumei Wen, Wenjian Yin, and Hanzhong Wu. An upconversion management circuit for low-frequency vibrating energy harvesting. *IEEE Transactions on Industrial Electronics*, 61(7):3349–3358, 2014.

Junjie Liu, Zhaoxin Geng, Zhiyuan Fan, Jian Liu, and Hongda Chen. Point-of-care testing based on smartphone: The current state-of-the-art (2017–2018). *Biosensors and Bioelectronics*, 132:17–37, 2019.

Jerome P Lynch and Kenneth J Loh. A summary review of wireless sensors and sensor networks for structural health monitoring. *Shock and Vibration Digest*, 38(2):91–130, 2006.

Lindsay M Miller, Einar Halvorsen, Tao Dong, and Paul K Wright. Modeling and experimental verification of low-frequency mems energy harvesting from ambient vibrations. *Journal of Micromechanics and Microengineering*, 21(4):045029, 2011.

Perry Miller and Doug Moore. Precision voltage references. *Analog Applications*, 1999.

Henri J Oguey and Daniel Aebischer. Cmos current reference without resistance. *IEEE Journal of Solid-State Circuits*, 32(7):1132–1135, 1997.

Arun Paidimarri, Danielle Griffith, Alice Wang, Anantha P Chandrakasan, and Gangadhar Burra. A 120nw 18.5 khz rc oscillator with comparator offset cancellation for$\pm$0.25%

temperature stability. In *2013 IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pages 184–185. IEEE, 2013.

J Paulo and PD Gaspar. Review and future trend of energy harvesting methods for portable medical devices. In *Proceedings of the world congress on engineering*, volume 2, pages 168–196, 2010.

Nikhil Raj, Ashutosh Kumar Singh, and Anil Kumar Gupta. Low power high output impedance high bandwidth qfgmos current mirror. *Microelectronics Journal*, 45(8):1132–1142, 2014.

Ariel Rosenman, Elena Markevich, Gregory Salitra, Doron Aurbach, Arnd Garsuch, and Frederick Francois Chesneau. Review on li-sulfur battery systems: An integral perspective. *Advanced Energy Materials*, 5(16):1500212, 2015.

Shad Roundy, Eli S Leland, Jessy Baker, Eric Carleton, Elizabeth Reilly, Elaine Lai, Brian Otis, Jan M Rabaey, Paul K Wright, and V Sundararajan. Improving power output for vibration-based energy scavengers. *IEEE Pervasive computing*, 4(1):28–36, 2005.

Kaushik Roy and Sharat C Prasad. *Low-power CMOS VLSI circuit design*. John Wiley & Sons, 2009.

Kaushik Roy, Saibal Mukhopadhyay, and Hamid Mahmoodi-Meimand. Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits. *Proceedings of the IEEE*, 91(2):305–327, 2003.

Leila Safari and Shahram Minaei. A simple low voltage, high output impedance resistor based current mirror with extremely low input and output voltage requirements. In *Telecommunications and Signal Processing (TSP), 2016 39th International Conference on*, pages 254–256. IEEE, 2016.

Samar K Saha. Modeling process variability in scaled cmos technology. *IEEE Design & Test of Computers*, 27(2):8–16, 2010.

Takayasu Sakurai and A Richard Newton. A simple mosfet model for circuit analysis. *IEEE transactions on Electron Devices*, 38(4):887–894, 1991.

Edgar Sánchez-Sinencio and Andreas G Andreou. A currentbased mosfet model for integrated circuit design.

Willy M Sansen, Frank Op't Eynde, and Michiel Steyaert. A cmos temperature-compensated current reference. *IEEE Journal of Solid-State Circuits*, 23(3):821–824, 1988.

AJ Scholten, GDJ Smit, M Durand, R Van Langevelde, CJJ Dachs, and DBM Klaassen. A new compact model for junctions in advanced cmos technologies. In *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.*, pages 4–pp. IEEE, 2005.

Adel S Sedra and Kenneth C Smith. Microelectronic circuits, 2014.

Francisco Serra-Graells and Jose Luis Huertas. Sub-1-v cmos proportional-to-absolute temperature references. *IEEE Journal of Solid-State Circuits*, 38(1):84–88, 2003.

Neha Singh and Harshit Kumar. Low voltage fgmos based current mirror. *Int J Sci Eng Technol Res*, 5:2840–2843, 2016.

Henry A Sodano, Daniel J Inman, and Gyuhae Park. A review of power harvesting from vibration using piezoelectric materials. *Shock and Vibration Digest*, 36(3):197–206, 2004.

Bang-Sup Song and P Gray. A precision curvature-compensated cmos bandgap reference. In *1983 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, volume 26, pages 240–241. IEEE, 1983.

Yuan Taur. The incredible shrinking transistor. *Ieee Spectrum*, 36(7):25–29, 1999.

J Teichmann, K Burger, W Hasche, J Herrfurth, and G Taschner. One time programming (otp) with zener diodes in cmos processes. In *ESSDERC'03. 33rd Conference on European Solid-State Device Research, 2003.*, pages 433–436. IEEE, 2003.

Scott E Thompson and Srivatsan Parthasarathy. Moore's law: the future of si microelectronics. *Materials today*, 9(6):20–25, 2006.

R Torrance, T Viswanathan, and JV Hanson. Cmos voltage to current transducers. *IEEE transactions on circuits and systems*, 32(11):1097–1104, 1985.

Yannis P Tsividis and Richard W Ulmer. A cmos voltage reference. *IEEE Journal of Solid-State Circuits*, 13(6):774–778, 1978.

Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya. A 300 nw, 15 ppm/ c, 20 ppm/v cmos voltage reference circuit consisting of subthreshold mosfets. *IEEE Journal of solid-state circuits*, 44(7):2047–2054, 2009.

Ken Ueno, Tetsuya Hirose, Tetsuya Asai, and Yoshihito Amemiya. A1-μw 600-ppm/°C current reference circuit consisting of subthreshold cmos circuits. *IEEE Transactions on Circuits and Systems II: Express Briefs*, 57(9):681–685, 2010.

Eric Vittoz and Jean Fellrath. Cmos analog integrated circuits based on weak inversion operations. *IEEE journal of solid-state circuits*, 12(3):224–231, 1977.

Zhenhua Wang. Current-mode cmos integrated circuits for analog computation and signal processing: a tutorial. *Analog Integrated Circuits and Signal Processing*, 1(4):287–295, 1991.

Kaiyu Wangaa, Zhenan Tang, Hualong Li, Yun Zhao, Xi Song, and Jiandong Su. Design and simulation of a cmos current source cell. *Procedia Environmental Sciences*, 10:1052–1058, 2011.

Chundong Wu, Wang Ling Goh, Chiang Liang Kok, Wanlan Yang, and Liter Siek. A low tc, supply independent and process compensated current reference. In *Custom Integrated Circuits Conference (CICC), 2015 IEEE*, pages 1–4. IEEE, 2015.

Zhaochu Yang, Einar Halvorsen, and Tao Dong. Electrostatic energy harvester employing conductive droplet and thin-film electret. *Journal of Microelectromechanical Systems*, 23(2): 315–323, 2014.

Faruk Yildiz. Potential ambient energy-harvesting sources and techniques. *Journal of technology Studies*, 35(1):40–48, 2009.

C Yoo and J Park. Cmos current reference with supply and temperature compensation. *Electronics Letters*, 43(25):1422–1424, 2007.

Zhao Zhe, Zhou Feng, and Huang Shengzhuan. All-cmos temperature compensated current reference. *Journal of Semiconductors*, 31(6):065016, 2010.

Tong Zhou, Tao Dong, Yan Su, and Yong He. A cmos readout with high-precision and low-temperature-coefficient background current skimming for infrared focal plane array. *IEEE Transactions on Circuits and Systems for Video Technology*, 25(8):1447–1455, 2015.

A

SUPPORT MATERIAL

A.1 TECHNOLOGY PARAMETERS

The technological parameters used in the simulations and extracted by MOSIS during the manufacture of the circuits are shown below. The parameters used were the BSIM3v3 and ACM models in the SPICE simulator. Initially, the ACM parameters were used in the simulations, which have fewer parameters and facilitate the analytical calculations. Subsequently, in other simulations, the BSIM3v3 parameters were used, which are more complete than the ACM model. The technologies used in simulations were AMS 0.35μm C35BC3.

A.1.1 *CMOS AMS 0.35 NMOS*

```
.MODEL MODN NMOS LEVEL=8
+MOBMOD =1.000e+00 CAPMOD =2.000e+00 NOIMOD =3.000e+00
+K1 =6.044e-01
+K2 =2.945e-03 K3 =-1.715e+00 K3B =6.325e-01
+NCH =2.310e+17 VTH0 =5.655e-01
+VOFF =-5.719e-02 DVT0 =2.227e+01 DVT1 =1.051e+00
+DVT2 =3.393e-03 KETA =-6.207e-04
+PSCBE1 =2.756e+08 PSCBE2 =9.645e-06
+DVT0W =0.000e+00 DVT1W =0.000e+00 DVT2W =0.000e+00
```

```
+UA =1.000e-12 UB =1.723e-18 UC =5.756e-11
+U0 =4.035e+02
+DSUB =5.000e-01 ETA0 =3.085e-02 ETAB =-3.947e-02
+NFACTOR=1.119e-01
+EM =4.100e+07 PCLM =6.831e-01
+PDIBLC1=1.076e-01 PDIBLC2=1.453e-03 DROUT =5.000e-01
+A0 =2.208e+00 A1 =0.000e+00 A2 =1.000e+00
+PVAG =0.000e+00 VSAT =1.178e+05 AGS =2.490e-01
+B0 =-1.765e-08 B1 =0.000e+00 DELTA =1.000e-02
+PDIBLCB=2.583e-01
+W0 =1.184e-07 DLC =3.000e-08
+DWB =0.000e+00 DWG =0.000e+00
+LL =0.000e+00 LW =0.000e+00 LWL =0.000e+00
+LLN =1.000e+00 LWN =1.000e+00 WL =0.000e+00
+WW =0.000e+00 WWL =0.000e+00 WLN =1.000e+00
+WWN =1.000e+00
+AT =3.300e+04 UTE =-1.800e+00
+KT1 =-3.302e-01 KT2 =2.200e-02 KT1L =0.000e+00
+UA1 =0.000e+00 UB1 =0.000e+00 UC1 =0.000e+00
+PRT =0.000e+00
+CGDO =1.300e-10 CGSO =1.300e-10 CGBO =1.100e-10
+CGDL =1.380e-10 CGSL =1.380e-10 CKAPPA =6.000e-01
+CF =0.000e+00 ELM =5.000e+00
+XPART =1.000e+00 CLC =1.000e-15 CLE =6.000e-01
+RDSW =6.043e+02
+CDSC =0.000e+00 CDSCB =0.000e+00 CDSCD =8.448e-05
+PRWB =0.000e+00 PRWG =0.000e+00 CIT =1.000e-03
+TOX =7.700e-09
+NLX =1.918e-07
+ALPHA0 =0.000e+00 BETA0 =3.000e+01
+AF =1.3600e+00 KF =5.1e-27 EF =1.000e+00
+NOIA =1.73e+19 NOIB =7.000e+04 NOIC =-5.64e-13
+LINT =8.285e-09 WINT =2.676e-08 XJ =3.000e-07
+RSH =8.200e+01 JS =2.000e-05
+CJ =9.300e-04 CJSW =2.800e-10
+MJ =3.100e-01 MJSW =1.900e-01
```

```
+PB =6.900e-01 PBSW =6.900e-01
* ---------------------------------------------------------------------
```

A.1.2 *CMOS AMS 0.35 NMOS*

```
.MODEL MODP PMOS LEVEL=8
+MOBMOD =1.000e+00 CAPMOD =2.000e+00 NOIMOD =3.000e+00
+K1 =5.675e-01
+K2 =-4.39e-02 K3 =4.540e+00 K3B =-8.518e-01
+NCH =1.032e+17 VTH0 =-6.171e-01
+VOFF =-1.128e-01 DVT0 =1.482e+00 DVT1 =3.884e-01
+DVT2 =-1.154e-02 KETA =-2.558e-02
+PSCBE1 =1.000e+09 PSCBE2 =1.000e-08
+DVT0W =0.000e+00 DVT1W =0.000e+00 DVT2W =0.000e+00
+UA =2.120e-10 UB =8.290e-19 UC =-5.284e-11
+U0 =1.296e+02
+DSUB =5.000e-01 ETA0 =2.293e-01 ETAB =-3.917e-03
+NFACTOR=8.237e-01
+EM =4.100e+07 PCLM =2.979e+00
+PDIBLC1=3.310e-02 PDIBLC2=1.000e-09 DROUT =5.000e-01
+A0 =1.423e+00 A1 =0.000e+00 A2 =1.000e+00
+PVAG =0.000e+00 VSAT =2.000e+05 AGS =3.482e-01
+B0 =2.719e-07 B1 =0.000e+00 DELTA =1.000e-02
+PDIBLCB=-1.777e-02
+W0 =4.894e-08 DLC =2.500e-08
+DWB =0.000e+00 DWG =0.000e+00
+LL =0.000e+00 LW =0.000e+00 LWL =0.000e+00
+LLN =1.000e+00 LWN =1.000e+00 WL =0.000e+00
+WW =0.000e+00 WWL =0.000e+00 WLN =1.000e+00
+WWN =1.000e+00
+AT =3.300e+04 UTE =-1.350e+00
+KT1 =-5.703e-01 KT2 =2.200e-02 KT1L =0.000e+00
```

```
+UA1   =0.000e+00 UB1   =0.000e+00 UC1   =0.000e+00
+PRT   =0.000e+00
+CGDO =1.100e-10 CGSO =1.100e-10 CGBO =1.100e-10
+CGDL =1.150e-10 CGSL =1.150e-10 CKAPPA =6.000e-01
+CF =0.000e+00 ELM   =5.000e+00
+XPART =1.000e+00 CLC =1.000e-15 CLE   =6.000e-01
+RDSW =1.853e+03
+CDSC =6.994e-04 CDSCB =2.943e-04 CDSCD =1.970e-04
+PRWB =0.000e+00 PRWG =0.000e+00 CIT   =1.173e-04
+TOX   =7.700e-09
+NLX   =1.770e-07
+ALPHA0 =0.000e+00 BETA0 =3.000e+01
+AF =1.48e+00 KF   =8.5e-27 EF =1.000e+00
+NOIA =1.52e+18 NOIB   =7.75e+03 NOIC   =5.0e-13
+LINT =-5.64e-08 WINT =3.845e-08 XJ =3.000e-07
+RSH   =1.560e+02 JS =2.000e-05
+CJ =1.420e-03 CJSW =3.800e-10
+MJ =5.500e-01 MJSW =3.900e-01
+PB =1.020e+00 PBSW =1.020e+00
* ----------------------------------------------------------------------
```

A.1.3 *Fabrication parameters extracted*

```
.MODEL CMOSN NMOS (          LEVEL =49
+VERSION = 3.1      TNOM   =27     TOX =7.7E-9
+XJ = 1E-7      NCH =2.2E17     VTH0   =0.479871
+K1 = 0.5955345     K2   =4.870054E-3      K3   =31.0560237
+K3B   = -10     W0   =1.927877E-5      NLX =2.315339E-7
+DVT0W   = 0     DVT1W =0      DVT2W =0
+DVT0 = 3.7277856     DVT1   =0.7127523      DVT2   =-0.1341752
+U0 = 370.5621715     UA   =-6.20728E-10     UB   =2.12351E-18
+UC = 3.946931E-11      VSAT   =1.578372E5     A0   =1.3160965
```

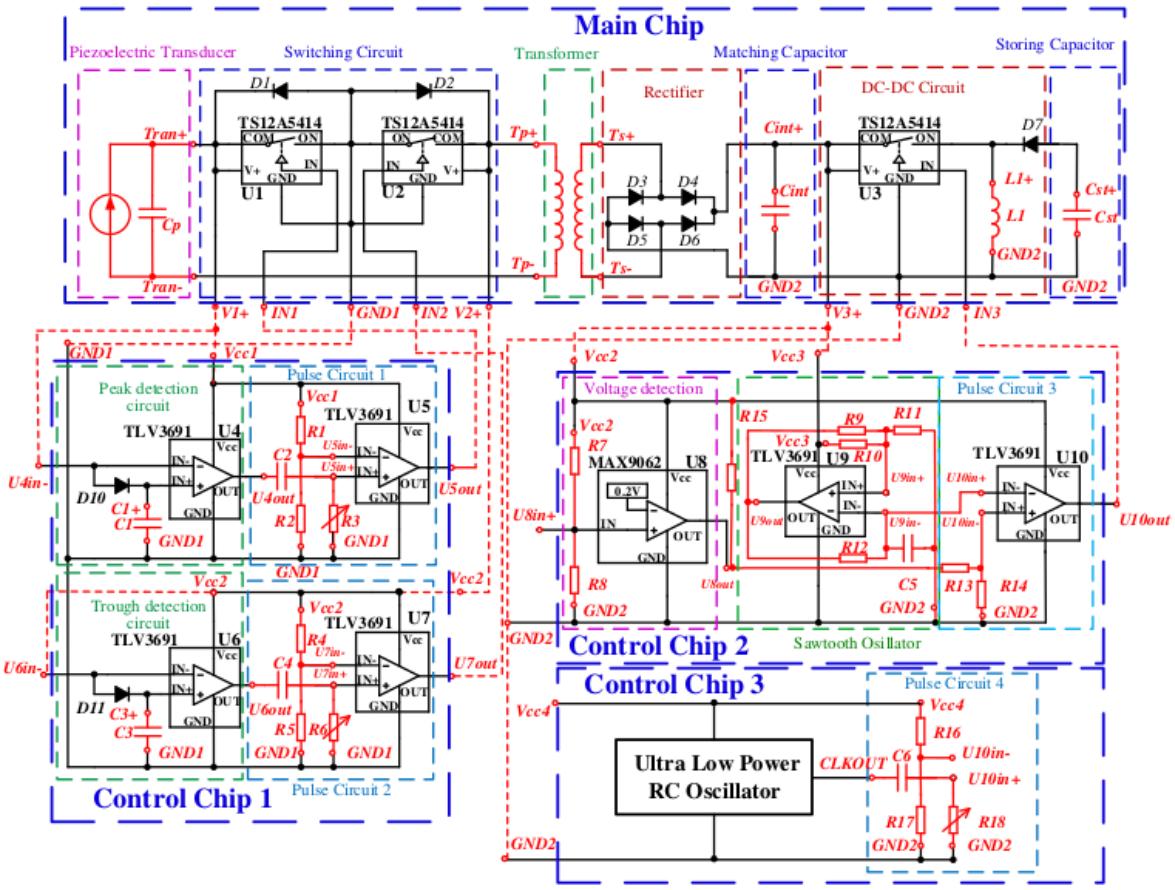
```
+AGS = 0.2035805 B0 =8.684055E-7 B1 =5E-6
+KETA = 1.195258E-3 A1 =5.01445E-4 A2 =0.4367848
+RDSW = 930.3632681 PRWG =-0.0662495 PRWB =-0.1020032
+WR = 1 WINT =1.543877E-7 LINT =2.502774E-10
+XL = -5E-8 XW =1.5E-7 DWG =-5.601953E-9
+DWB = 4.116379E-9 VOFF =-0.077016 NFACTOR =1.4098046
+CIT = 0 CDSC =2.4E-4 CDSCD =0
+CDSCB = 0 ETA0 =1 ETAB =9.332354E-3
+DSUB = 0.8313448 PCLM =1.6100703 PDIBLC1 =1.908382E-3
+PDIBLC2 = 2.883754E-6 PDIBLCB =-1E-3 DROUT =0
+PSCBE1 = 7.38739E8 PSCBE2 =9.669555E-4 PVAG =0
+DELTA = 0.01 RSH =80.7 MOBMOD =1
+PRT = 0 UTE =-1.5 KT1 =-0.11
+KT1L = 0 KT2 =0.022 UA1 =4.31E-9
+UB1 = -7.61E-18 UC1 =-5.6E-11 AT =3.3E4
+WL = 0 WLN =1 WW =0
+WWN = 1 WWL =0 LL =0
+LLN = 1 LW =0 LWN =1
+LWL = 0 CAPMOD =2 XPART =0.5
+CGDO = 2.85E-10 CGSO =2.85E-10 CGBO =1E-12
+CJ = 9.055464E-4 PB =0.8 MJ =0.3471175
+CJSW = 3.480887E-10 PBSW =0.8 MJSW =0.1340635
+CJSWG = 1.82E-10 PBSWG =0.8 MJSWG =0.1340635
+CF = 0 PVTH0 =-0.0186275 PRDSW =-101.4287928
+PK2 = 3.100094E-3 WKETA =-1.618383E-3 LKETA =4.928755E-4
)
* ---------------------------------------------------------------------
```

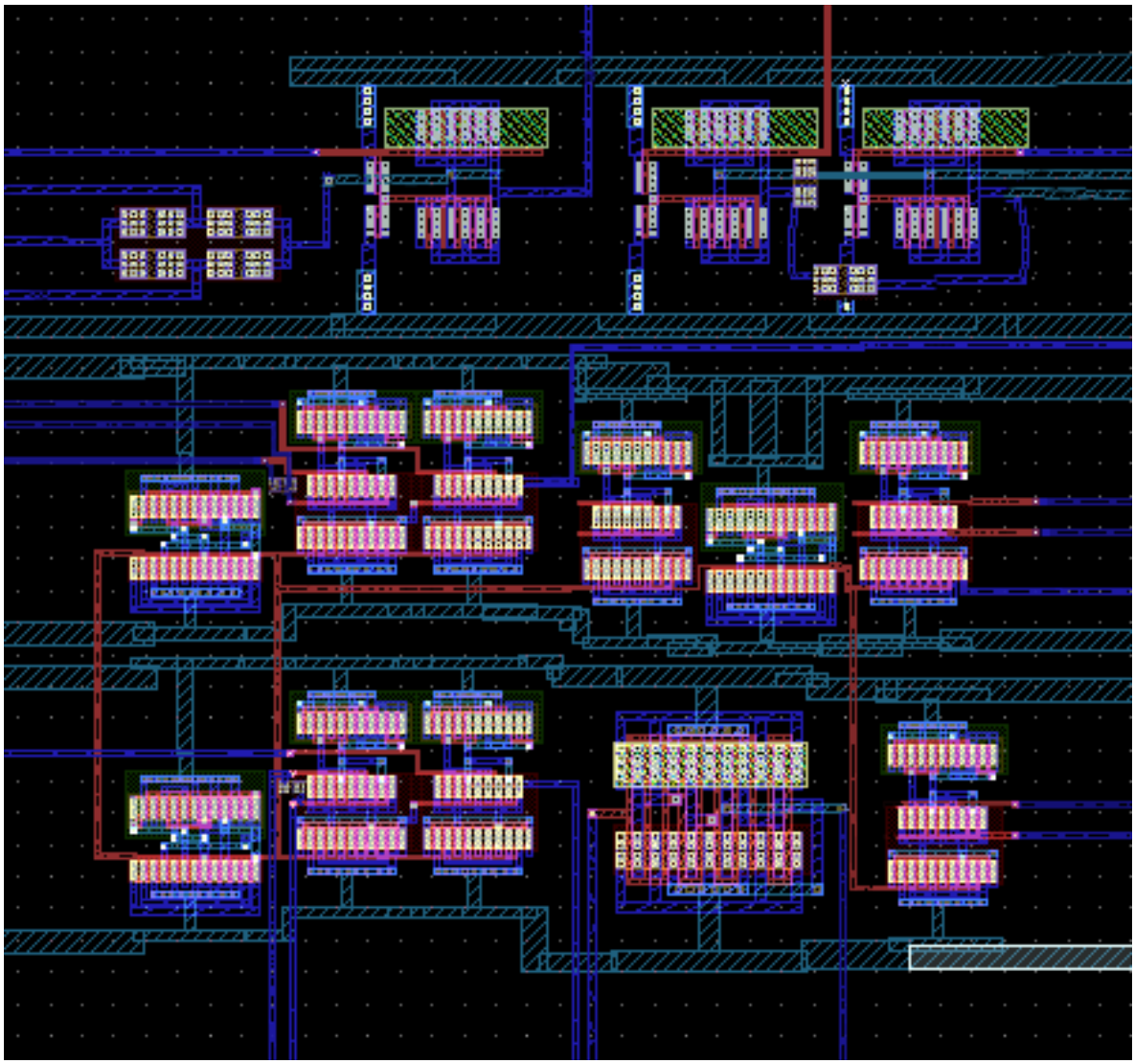
```
.MODEL CMOSP PMOS (
+VERSION = 3.1 TNOM = 27 TOX = 7.7E-9
+XJ = 1E-7 NCH = 8.52E16 VTH0 = -0.7350925
+K1 = 0.4288598 K2 = -0.0114832 K3 = 47.2991619
+K3B = -5 W0 = 4.171945E-6 NLX = 2.858711E-7
```

```
+DVT0W = 0 DVT1W = 0 DVT2W = 0
+DVT0 = 1.3953697 DVT1 = 0.5738767 DVT2 = -0.017946
+U0 = 148.7534168 UA = 1.311082E-10 UB = 1.681499E-18
+UC = -2.16371E-11 VSAT = 1.063971E5 A0 = 1.1377393
+AGS = 0.3718935 B0 = 2.707795E-6 B1 = 5E-6
+KETA = -5.402566E-3 A1 = 0 A2 = 0.5708398
+RDSW = 4E3 PRWG = -0.1143203 PRWB = 0.2137738
+WR = 1 WINT = 1.455594E-7 LINT = 0
+XL = -5E-8 XW = 1.5E-7 DWG = -1.395886E-8
+DWB = 8.356249E-9 VOFF = -0.1357486 NFACTOR = 2
+CIT = 0 CDSC = 2.4E-4 CDSCD = 0
+CDSCB = 0 ETA0 = 0.0584765 ETAB = 0.1338624
+DSUB = 0.6168241 PCLM = 3.9466493 PDIBLC1 = 6.201752E-3
+PDIBLC2 = 2.719856E-3 PDIBLCB = 4.291327E-3 DROUT = 0.0605352
+PSCBE1 = 8E10 PSCBE2 = 5E-10 PVAG = 1.0085966
+DELTA = 0.01 RSH = 156.9 MOBMOD = 1
+PRT = 0 UTE = -1.5 KT1 = -0.11
+KT1L = 0 KT2 = 0.022 UA1 = 4.31E-9
+UB1 = -7.61E-18 UC1 = -5.6E-11 AT = 3.3E4
+WL = 0 WLN = 1 WW = 0
+WWN = 1 WWL = 0 LL = 0
+LLN = 1 LW = 0 LWN = 1
+LWL = 0 CAPMOD = 2 XPART = 0.5
+CGDO = 3.31E-10 CGSO = 3.31E-10 CGBO = 1E-12
+CJ = 1.424439E-3 PB = 0.99 MJ = 0.546665
+CJSW = 3.914772E-10 PBSW = 0.99 MJSW = 0.3050481
+CJSWG = 4.42E-11 PBSWG = 0.99 MJSWG = 0.3050481
+CF = 0 PVTH0 = 6.780387E-3 PRDSW = -7.3589179
+PK2 = 1.444567E-3 WKETA = -1.356105E-3 LKETA = -5.850895E-3
)
* ---------------------------------------------------------------------
```

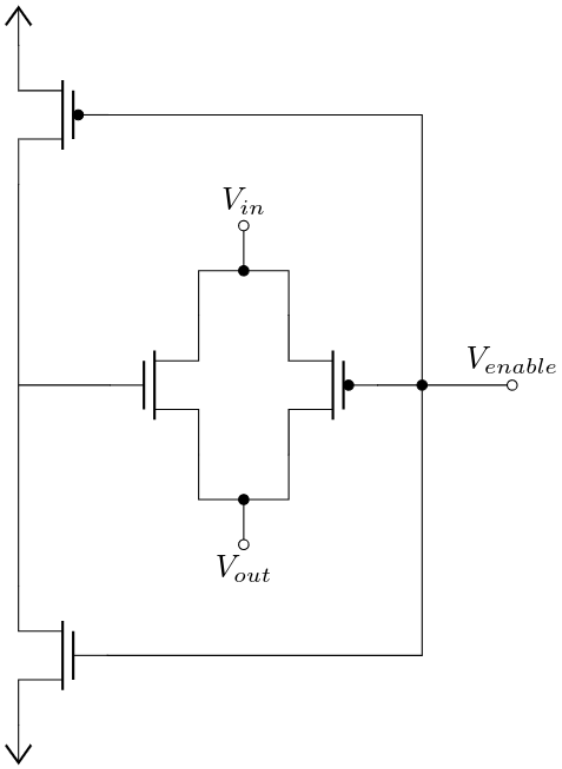
A.2 PHYSICAL LAYOUT

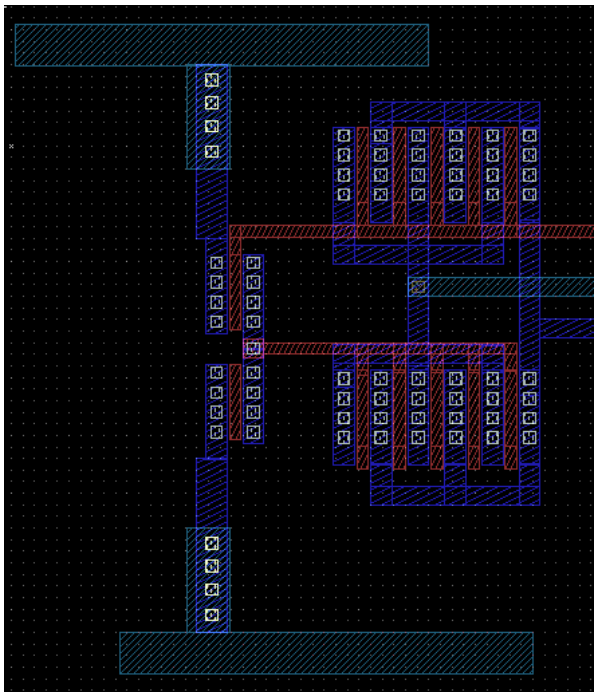
Complete Circuit



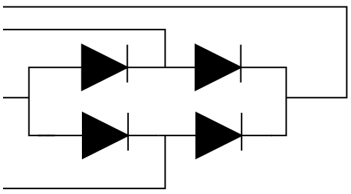


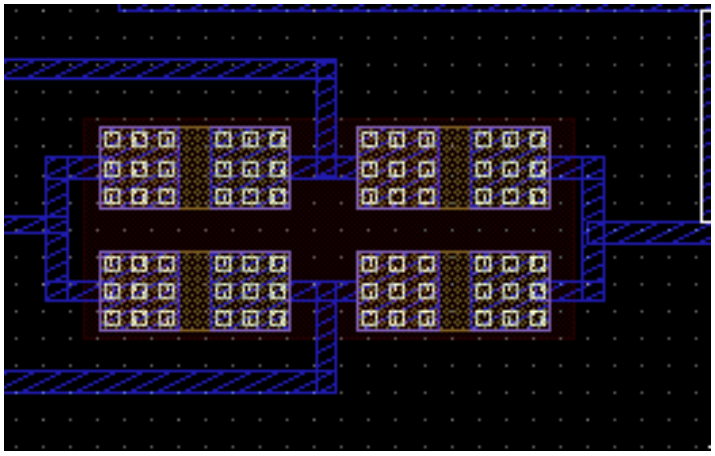
Analog Switch for switching circuit



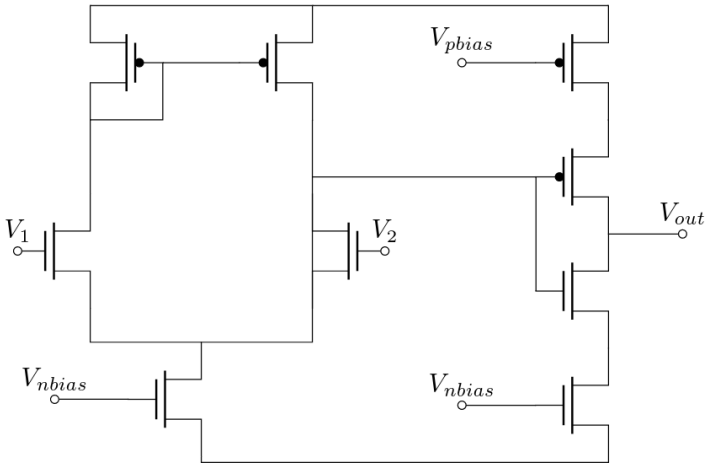


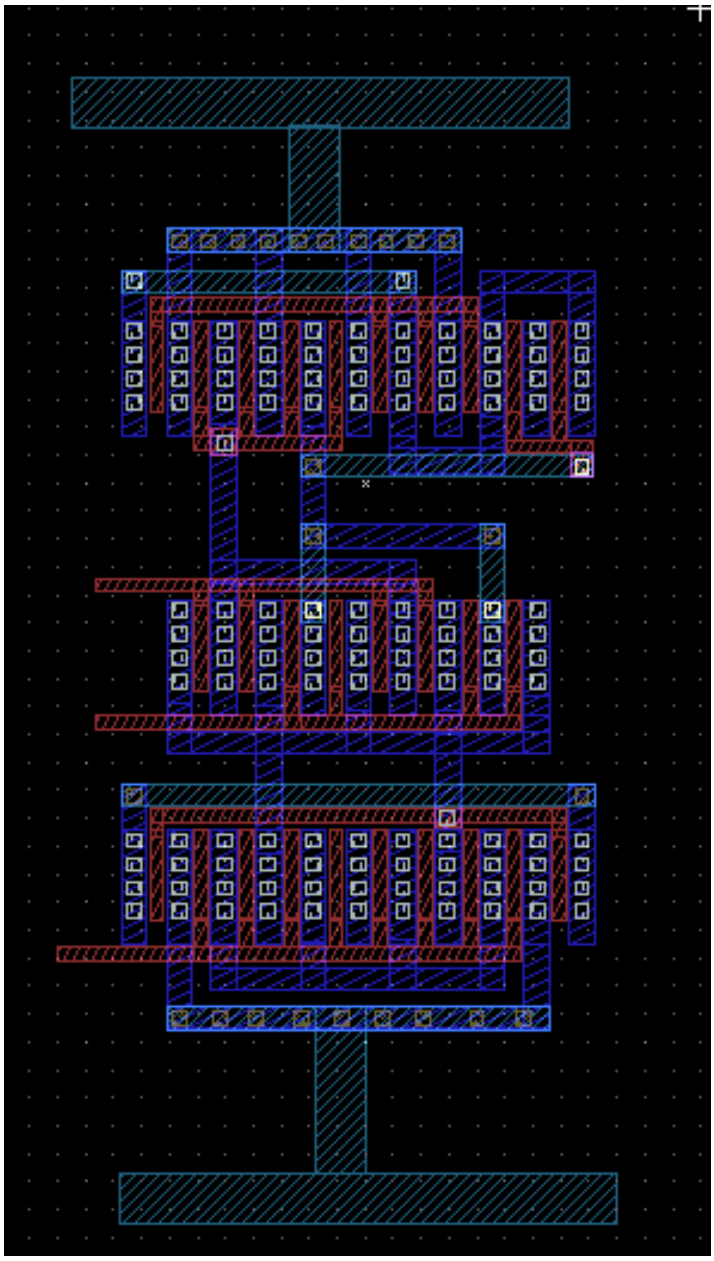
Rectifier using Schottky Diodes



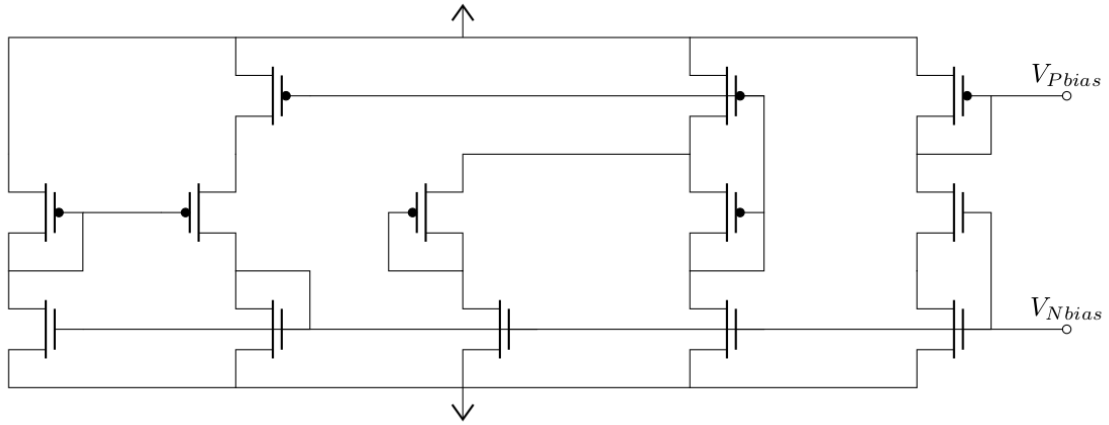


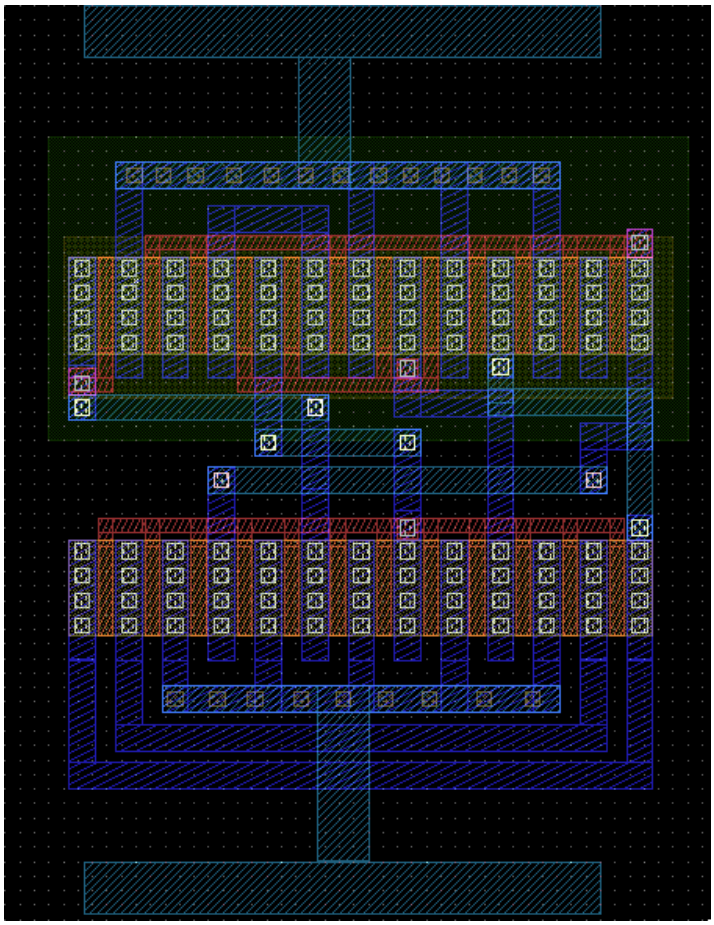
Comparator



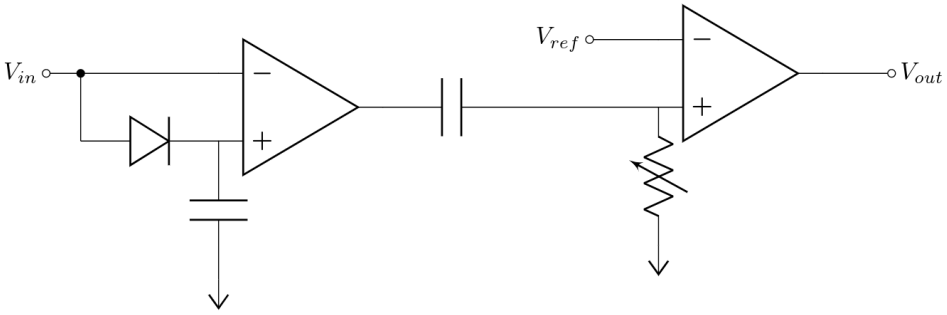


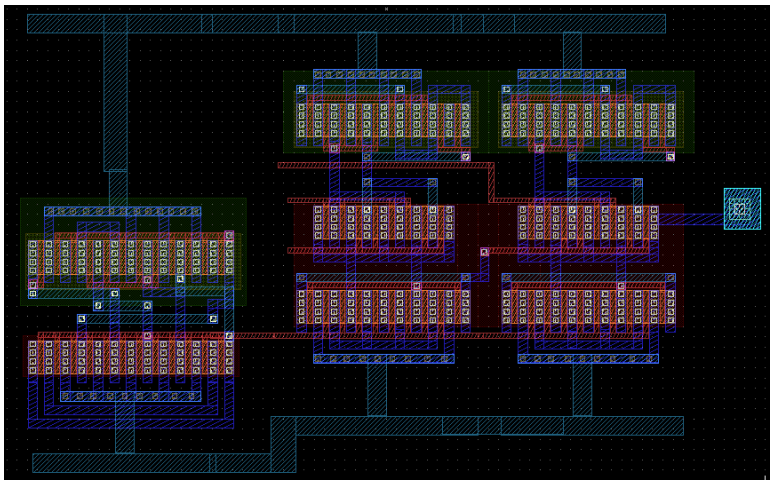
Current Reference



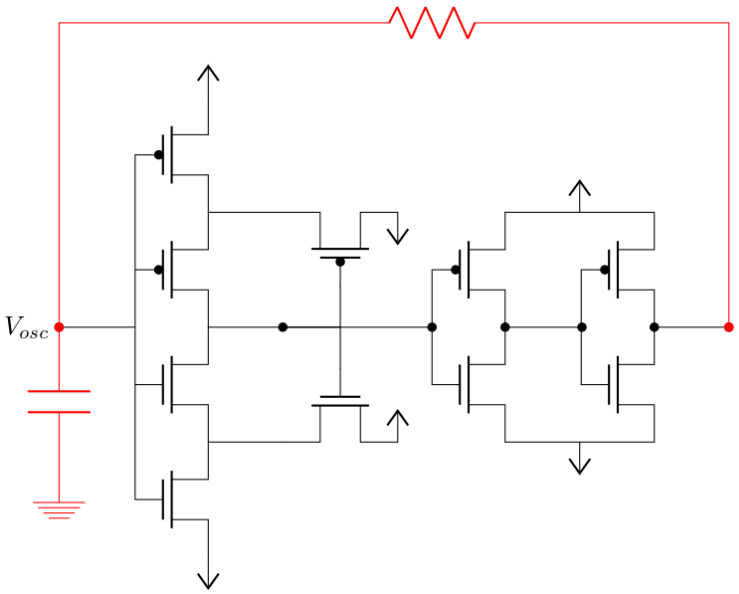


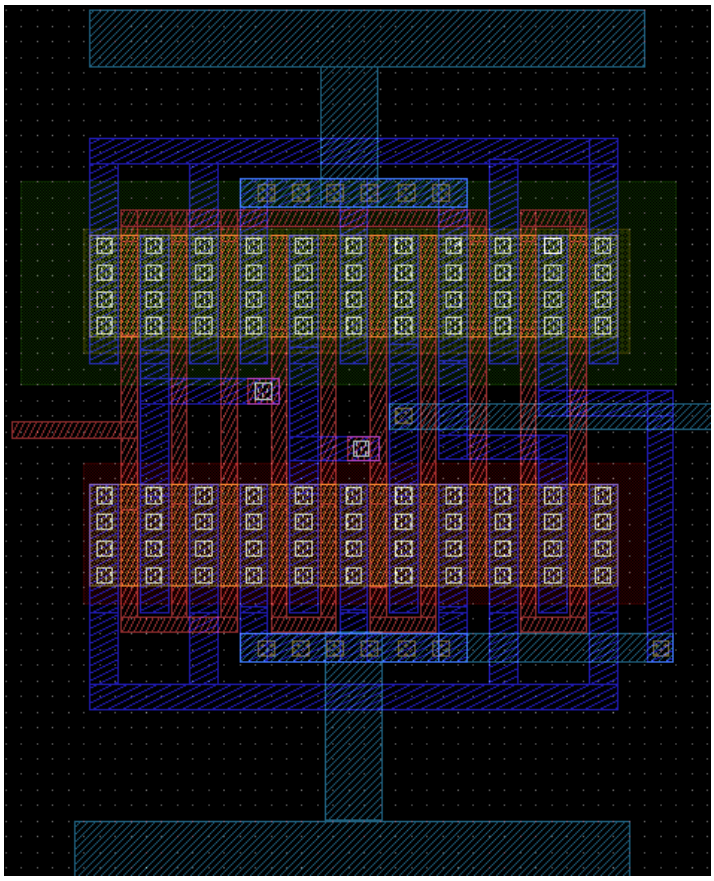
Peak Detector



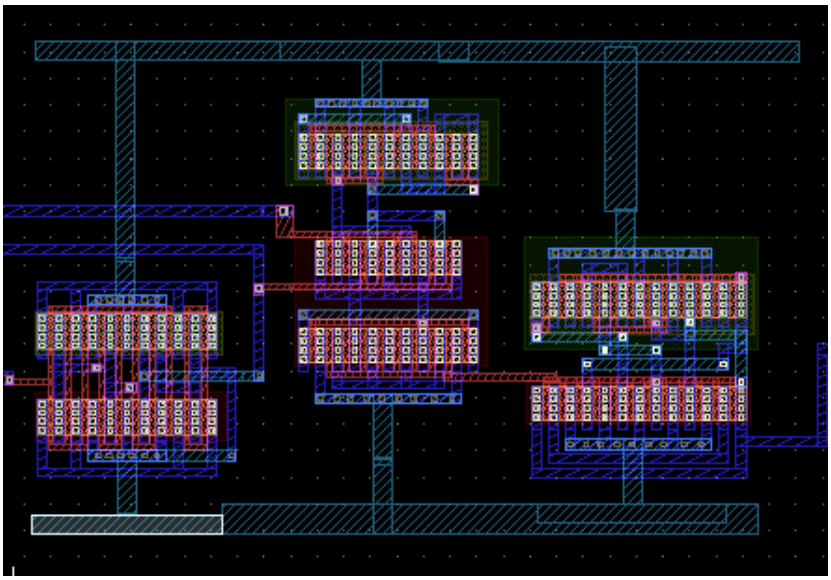


RC Oscillator





Control Chip #2



A.3 INTERNATIONAL JOURNAL ARTICLE

A.3.1 *A low-power CMOS current reference for piezoelectric energy harvester interface*

Submitted to

Transactions on Industrial Electronics

Manuscript ID

19-TIE-2038

Title

A low-power CMOS current reference for piezoelectric energy harvester interface

Authors

Rui Carvalho, Tao Dong, Zhaochu Yang, Ping Li, Yumei Wen

A low-power CMOS current reference for piezoelectric energy harvester interface

***Abstract*—This paper proposes a nanoscale CMOS current reference design for low power analog and digital devices. A self-biased circuit based on various simple design topologies is developed within the current reference. The current reference can compensate for temperature changes and fabrication discrepancies. Simulation results returned a low current around 12 nA. Excellent stability is achieved in a broad range of power supply voltages. In the interface with 0.35 μm fabrication process, a bias voltage is generated with currents in the nanoampere range. The present current reference is qualified to be used in digital-analog circuits, such as operational amplifiers or oscillators, and is designed to be suitable for energy harvesting interfaces, because of the high efficiency and low power consumption.**

***Index Terms*—low power, high efficiency, current reference, integrated circuit, power optimisation.**

I. Introduction

HARVESTING energy from the ambient environment to power portable electronics [1] wireless sensor networks (WSN) [2] has been popular during the last couple of decades. Piezoelectric energy harvesters emerges as an attractive solution for converting vibrational energy to electric energy. This type of energy production can be implemented in minimal size factors, which are beneficial for specific low power application, e.g. sensor nodes [3]. Circuits designed for this purpose should also have a very low power consumption to increase the energy scavenging efficiency. To efficiently extract power from the piezoelectric energy harvester, a power management circuit [4] comprising power rectification and storage is needed to attain a usable charge [2]. The extraction circuit is able to convert the signal give by the transducer, to a DC voltage. With consideration of the relatively low power scavenged from the ambient energy harvesters [5], the power management circuit is expected to have very low power consumption.

Integrated circuits (IC's) offer lower power consumption and smaller size compared to discrete packages, and therefore provide a solution to realize the power management circuit within the constraints. The technology Complementary Metal Oxide Semiconductor (CMOS) has been widely used in monolithic integrated circuit design [6], making it possible to create highly efficient circuits. Further improvements are feasible due to the scalability of the technology [7] when specific design rules are used. The rules are based on the resolution of the process, the λ parameter, defined by the minimum width of a polysilicon structure. Other improvements to power consumption and performance were conceived throughout the years [8]. Energy consumption reduction methods, such as decrease of leakage current [9] and dynamic power [10], chip capacitance minimization, technology scaling [11] and use of multiple thresholds [12], have been used leading to considerable performance improvement. Most of these techniques are well researched and used in several existing applications.

The transistors used in CMOS technology should be appropriately polarized by external voltage or current references. Ideally, the references are independent of power supply fluctuations, temperature variation and load resistance. For low power consumption purposes, current references are the most suitable way to polarize CMOS circuits. The current can be decreased to achieve the necessary power demands, without compromises to the supply voltage. The only limit to this reduction is the current leakages in the transistors.

This work studies general current reference topologies combined with state-of-the-art concepts, with a particular concern for power consumption. The performance of a voltage or current reference is defined by the power consumption and efficiency of one reference cell, along with temperature coefficient, fabrication process variation and supply sensitivity. Several issues are inherent in the development of precise integrated circuit cells. Variations in the circuit outputs as a result of temperature changes [13] or fabrication discrepancies [14] create several problems. Consequently, new approaches are found in order to negate or compensate for these variations. The sensitivity of the output current in a reference cell usually depends on supply voltage. In order to achieve independence from the supply voltage [15], the bias current [16] is determined by the output current itself. Supply voltage independence and state-of-the-art solutions were incorporated to improve the developed circuit topology to create a self-biased current reference. The circuit is designed to produce a compensated output current with very low sensitivity to temperature. The output current also does not depend on the physical properties of the technology and will therefore not be affected by unavoidable variation from fabrication processes.

This work aims to develop extremely low power current references, in the μW order of magnitude, to be used in energy harvesting management interfaces [17], [18], [19] and high-efficiency analog and digital circuits [20], [21]. Current reference design considerations are presented, and have been verified by circuit simulations. Comparison with results from literature indicates that the current reference proposed in this work is competitive in low power consumption, temperature stability, wide power supply range. The design can be readily implemented as a polarization circuit for analog and digital systems.

II. Design Considerations

A. Materials

This design is based on $0.35\mu m$ C35C4B3 process by ams AG, a mixed signal process with a standard cell library of

high density CMOS capable of 4-layer routing and a working temperature from -40 to 125$^{\circ}C$. The adoption of a standard CMOS technology allows the use of the the current reference as a module in a complete integrated circuit design, providing a current bias for other higher level circuit components.

This paper focuses on the output current value, stability and temperature coefficient with different simulation parameters, the simulation tool used is Cadence Virtuoso ADE. According to the model library files, we can get the following parameters that may be used for manual calculation in TABLE I.

TABLE I
CMOS C35C4B3 MODEL LIBRARY PARAMETERS

Device type	Thickness Gate Oxide (m)	Threshold voltage (V)	Mobility coefficient	Saturation Voltage (V)
NMOS	7.700e-09	5.655e-01	4.035e+02	1.178e+05
PMOS	7.700e-09	-6.171e-01	1.296e+02	2.000e+05

B. Methods

The current reference design takes into account temperature changes, fabrication process deviation and parasitic reductions. For this purpose multiple topologies are reviewed, gathering the benefits of particular designs, with the intent of integrating the advantageous aspects into one topology. Main advantages of topologies are discussed based on topological performances from simulations or the original work. The method for selecting transistor parameters for the circuit design is based on simple optimization through iterative analysis of results with design rule constraints, topology constraints (such as symmetry) and prior domain knowledge from literature, in order to improve stability and power consumption objectives.

1) Fundamentals:

Current references independent of the power source are commonly designed by the combination of a voltage reference and voltage to current converter.

As a standard current reference shown in Fig. 1, which is proposed in [22], [23], the output current is generated by a voltage drop across a resistor, which is usually created between the gate and drain of one or more metal-oxide-semiconductor field-effect transistor (MOSFET).

Working in strong inversion, the PMOS transistors create a current mirror, causing equal currents in the two circuit branches. Conversely, the NMOS transistor conducts in weak inversion. Regarding the relation to temperature variations, this circuit is identified as proportional to absolute temperature (PTAT)[24].

Consider a model for the MOSFET, expressed by equations [25] for each operation zone. The model covers essential properties of the transistors, performing correctly in strong or weak inversion regions [26], [27]. The electric field longitudinal element is smaller than the transversal part, making the concept of channel approximation a reasonable assumption.

$$I_S = \mu_n C'_{ox} \frac{V_t^2}{2} \frac{W}{L} \tag{1}$$

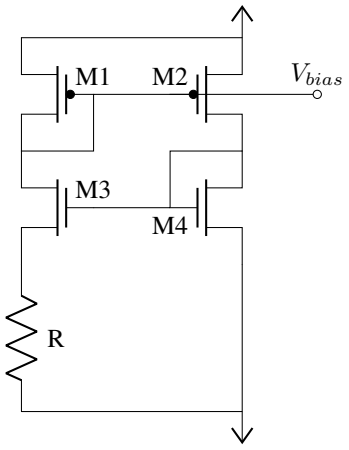


Fig. 1. Standard current reference.

Equation (1) calculates the passing current through the MOSFET in the saturation region. This region is the desired state for the majority of the devices; therefore, the expression is used as the core for further calculations and model computation. The parameters in the equation, μ is the mobility, C'_{ox} is the gate oxide capacitance per unit area, V_t the thermal voltage, and $\frac{W}{L}$ expresses the size relations of the transistor.

This model was derived from the inversion level approach to resolve the operation region [28], [29]. The drain current can be expressed by subtracting the reverse current from the forward current.

$$I_D = I_F - I_R = I_S(i_f - i_r) \tag{2}$$

In the saturation region the forward current is much greater than the reverse current, $I_F \gg I_R$, so the the drain current can be expressed solely by its direct current expressions, $I_D \approx I_F \approx I_S \cdot i_f$

Equation (3) describes I_D in strong inversion, when $I_D \gg \beta V_T^2$. Strong inversion is used to accomplish higher speed while maintaining low noise currents and offset voltages. The weak inversion region in equation (4), with $I_D \ll \beta V_T^2$, achieves the highest gain values.

$$I_D = \frac{\beta}{2n}(V_G - V_{T0} - nV_S)^2 \tag{3}$$

$$I_D = K\beta V_T^2 e^{\frac{V_G - V_{T0} - nVS}{nU_T}} \tag{4}$$

$$\beta = \mu_n C'ox \frac{W}{L} \tag{5}$$

The output current can be easily calculated, which is dependent on the resistor value, the current mirror ratio and the transistors drain currents.

$$I_o = \frac{V_t ln\left(\frac{\beta_3\beta_2}{\beta_1\beta_4}\right)}{R} \tag{6}$$

This topology is very inefficient when creating a current output equal to the current reference. The current consumption

of the reference circuit is twice the output current from being mirrored in the two branches, resulting in 33% calculated efficiency. This circuit may be suitable for low voltage cases, but not suitable for low currents.

To be able to generate small currents, using this topology, the resistor value would have to be extremely large. Implementation of a resistor with such size in the available CMOS technology would require a large area of the silicon wafe. Beyond this problem, the resistors fabricated in CMOS processes have variations of $10 - 30\%$ in their final value, creating a difference between devices, preventing the usability of a final system. Besides, the CMOS resistor does not have a well-defined temperature coefficient, which brings forth more challenges when trying to compensate temperature variations.

The present knowledge for reference circuits in CMOS technology based on intrinsic physical properties is still very limited, other topologies are typically based on the circuit in Fig. 1.

A simple variation to the standard current reference circuit is the replacement of the resistor. In this new design the voltage drop, previously over the resistance, is now created by transistors working in weak inversion.

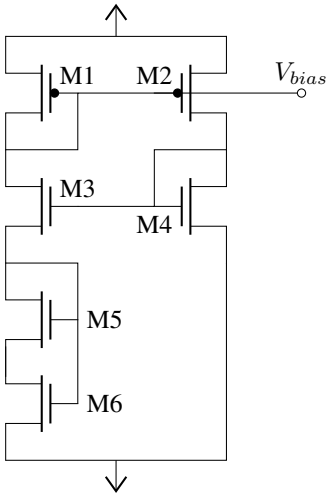


Fig. 2. Resistorless PTAT current reference.

The transistors act as voltage dividers, creating voltages on the order of mV. Whenever a higher voltage drop is needed, another cell of transistors can be added in parallel to the first cell.

$$V_c = V_t ln\left(1 + \frac{\beta_2}{\beta_1}\right) \tag{7}$$

2) Temperature compensated topologies:

One crucial aspect for a current reference design is to compensate for the temperature variation. Behaviour of integrated circuits can be affected by the temperature of the device, some of these changes are sub-optimal and should be prevented. This is quantified by the temperature coefficient (sensitivity) (8), the relative change of X_{ref} associated with a change in temperature, usually measured in $ppm/^{\circ}C$. In a CMOS circuit, components in a reference circuit tend to be dependent on temperature. Consequently, the temperature coefficient calculation is occasionally arduous and lengthy.

$$TC = \frac{\partial X_{ref}}{\partial T \cdot X_{ref}} \tag{8}$$

The temperature coefficient of a reference is possible to determine by an expression involving the partial derivation of its temperature dependent components. In equation (9) is the general function for the calculation of a circuit temperature coefficient.

$$TC = f\left(TC_{V_{DD}}, TC_{\beta_n}, TC_{\beta_p}, TC_{V_{tn}}, TC_{V_{tp}}\right) \tag{9}$$

An existing solution for temperature independence of current references, is the cancellation of temperature induced variations, using two different currents multiplied by a square-rooting CMOS interface.

The square-law [30], states that the output of a device is proportional to the squared input of that same device in the input range of its normal behaviour. A square-rooting circuit in Fig. 3 may be easily implemented by CMOS transistors exclusively in a symmetrical arrangement, the output current is then extracted by a current mirror. A square-rooting interface, along with multiplication, division, negation and squaring circuits, is commonly used as analog circuit building blocks for signal processing.

The currents to be multiplied by the square-rooting interface should cancel each other out [31] to generate a temperature independent voltage. To accomplish this cancellation, one of the currents should be proportional to the electron mobility, while the other is inversely proportional. Consistent with solid-state physics, the electron mobility is dependent on several factors [32], temperature being one of them. Using the inverse temperature relationship of two currents as mentioned earlier, to cancel each other out, which compensates the resulting output current for variation in temperature. The drafted circuit is in Fig. 3.

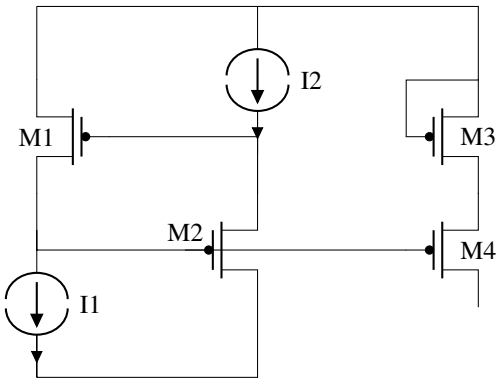


Fig. 3. Square-rooting interface.

A straightforward way to generate the output current, comes from designing symmetrical current sources, as shown in Fig. 4. I_1 is proportional to the electron mobility, whereas I_2 created by a resistor and the following transistors is inversely proportional.

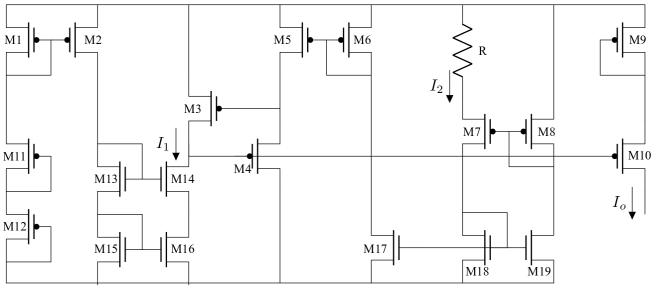


Fig. 4. Square-rooting based current reference.

The square-rooting cell is composed of 4 transistors operating in the weak inversion region, while the remaining MOSFETs operate in strong inversion. The equation (10) expresses the electron mobility based current generator which is mirrored to I_1.

$$I_1 = \frac{\beta_5 (V_{CC} - 3V_t)^2}{2(1 + 2\sqrt{\frac{\beta_5}{\beta_6}})^2} \tag{10}$$

The inversely proportional current, I_2, is mirrored from the current in the resistor.

$$I_2 = \frac{2(1 - \sqrt{\frac{\beta_{18}}{\beta_{16}}})^2}{R^2 \beta_{18}} \tag{11}$$

$$I_o = \sqrt{\frac{\beta_4 \beta_3}{\beta_2 \beta_1}} \sqrt{I_1} \sqrt{I_2} \tag{12}$$

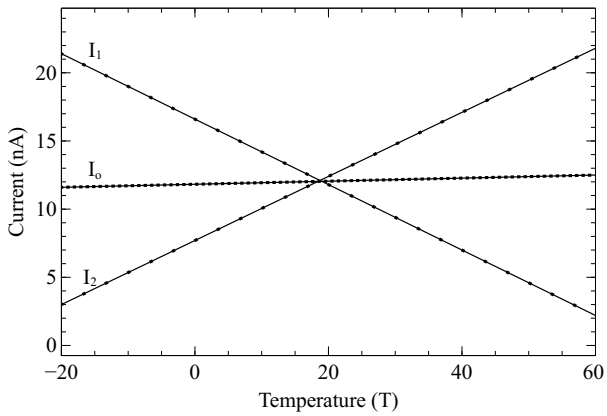


Fig. 5. Reversed temperature coefficient voltages compensating temperature variations

If all the MOSFETs are at the same temperature, it is assumed that the electron mobility affects the transistors correspondingly. Therefore, the mobility is cancelled according to equation (12), negating the temperature effects because of the temperature dependence of the threshold voltage and resistor value. The first current, I_1, uses the threshold voltage, incurring in a negative temperature coefficient, as V_t is typically affected in this way. Contrarily, CMOS resistors have a positive temperature coefficient, which is the reason for its application as the second current source.

Results show a temperature coefficient of 155 $ppm/^{\circ}C$ with a nominal current of 285 nA, in the current reference, over the temperature range of -15 to 75$^{\circ}C$.

3) Fabrication discrepancy independence concepts:

The previous reference designs, generate the output reference current based on intrinsic physical properties. This technique, although used in former literature, creates a new problem. Several properties vary according to deviations in fabrication. Although each integrated circuit works as expected, they may produce different results when compared, even among integrated circuits from the same batch. This is a problem in high definition analog circuits.

The switched capacitor method as reported by [14] and [33] presents a solution. This approach creates the expected current using an integrated CMOS capacitor, a voltage reference and a crystal oscillator. An equivalent resistance to the capacitor value and the switching frequency has to be created by a transistor cell. The generated current depends on the capacitor value and frequency, resulting in independence from the process technology. The integrated capacitor also brings another great trait, it is temperature independent, with a 20% maximum dispersion of the desired output.

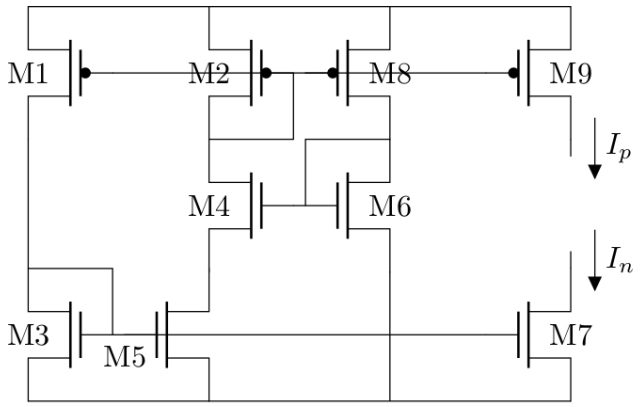


Fig. 6. Design following PTAT methodology

4) Low voltage and low power references:

There is a trend to reduce both area and power consumption of a device to achieve better miniaturization. The reduction of voltage from the power supply is not always possible; as sometimes, in CMOS circuitry, the use of several successive transistors between the positive and negative supply rails creates a high voltage difference between rails. As the minimum voltage necessary is established by the highest sum of voltage drops of the inline MOSFETs.

The circuit shown in Fig. 6, simplifies the design by using a succession of transistors to achieve a lower supply voltage. The circuit, based on a proportional to ambient temperature (PTAT) methodology, is resistorless, with an NMOS transistor in the triode region as a replacement. The circuit dependence on temperature is of T^5 while having a low supply voltage of $1.2V$. It is possible to achieve currents in the range of 1 to 100 nA.

5) Self Biased Current Source:

Self Biased Current Sources, designed for low voltages and very low power consumption purposes, are excellent solutions for the generation of polarizing current to be used in integrated circuits. Realizing the integrated circuit without external components allows for lower energy loss from parasitic elements and other unknown factors.

The current reference can be implemented by the voltage following current mirror topology and self cascoding MOSFETs. The design based in the Fig. 1 circuit, replaces the resistor with a self cascode MOSFET, in order to achieve the required low current and voltages.

In the circuit, a PTAT reference voltage is produced by an offset by the M8 and M9 devices, both in the low inversion region. This topology is fit for performance in devices where the efficiency is not the limiting factor.

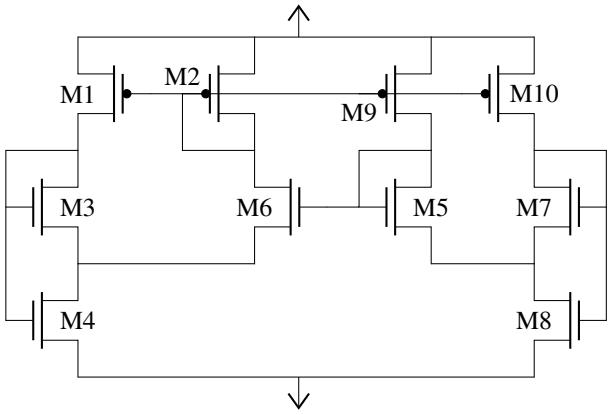


Fig. 7. Self bias proportional to temperature current reference.

Another implementation of the PTAT reference is using the self cascode MOSFETs M3 M4, making $V_{ref} = V_{s9}$. This topology is implemented with symmetry by equal transistors M8 M9.

Fig. 8 shows a nanoampere current reference proposed by [13], including temperature dependence control. In the article, both p and n-based, separate current references are designed. The subtraction of the symmetrical currents achieves temperature independence. The upcoming Figures presents the aforementioned, p and n-based, circuits separately.

Both of the circuits were simulated using the electronic design automation (EDA) tools with proprietary $0.35\mu m$ CMOS technology. The results shown in Fig. 9, with positive current sink to the NMOS and negative to the PMOS, using 1:1 current mirror connected to the corresponding biasing gate voltages.

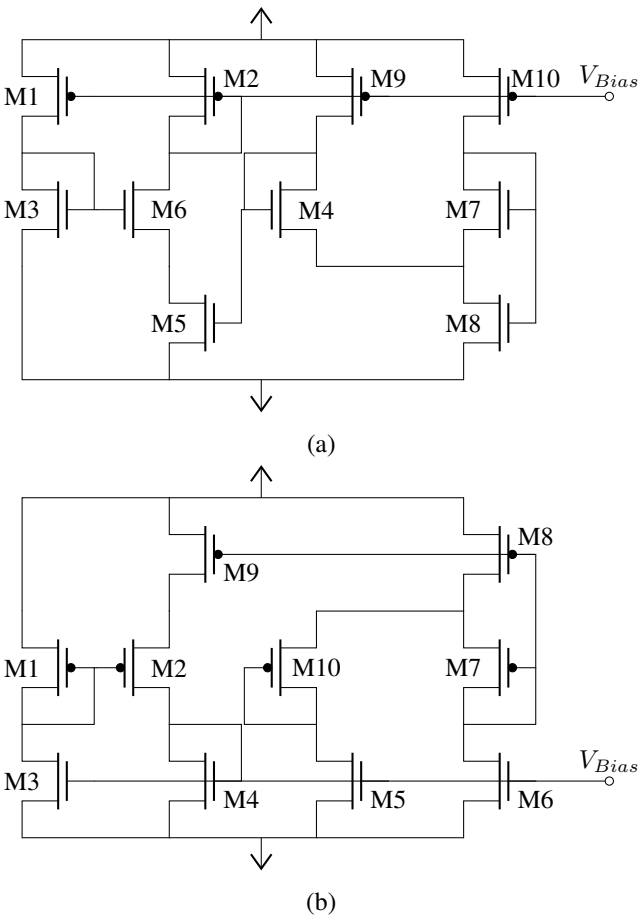


Fig. 8. Self bias current reference [13]. (a) p-type bias. (b) n-type bias.

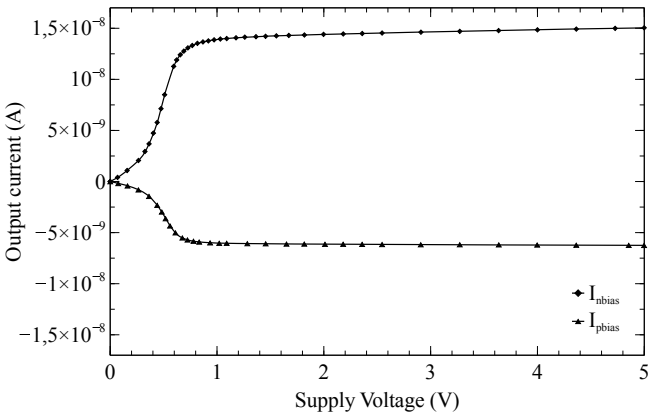


Fig. 9. Measured current reference of (8).

III. Prroposed Current Reference

A. Schematic Design

Taking into account the research and the results described in Section II an original design is developed, shown in Fig. 10, with parameters in TABLE II. The following circuit design is based on a combination of the features from the research. Several improvements were made, with the aim to increase the power efficiency, while keeping a decreased area footprint of the IC.

The current generation cell of the designed reference consists of p-type transistors, while the current mirroring is performed by the n-type transistors. The transistors perform, either in the weak or strong inversion, sub-threshold region.

The output current is predominantly dependent on the p-type MOSFET M_2, as a consequence of the voltage driven

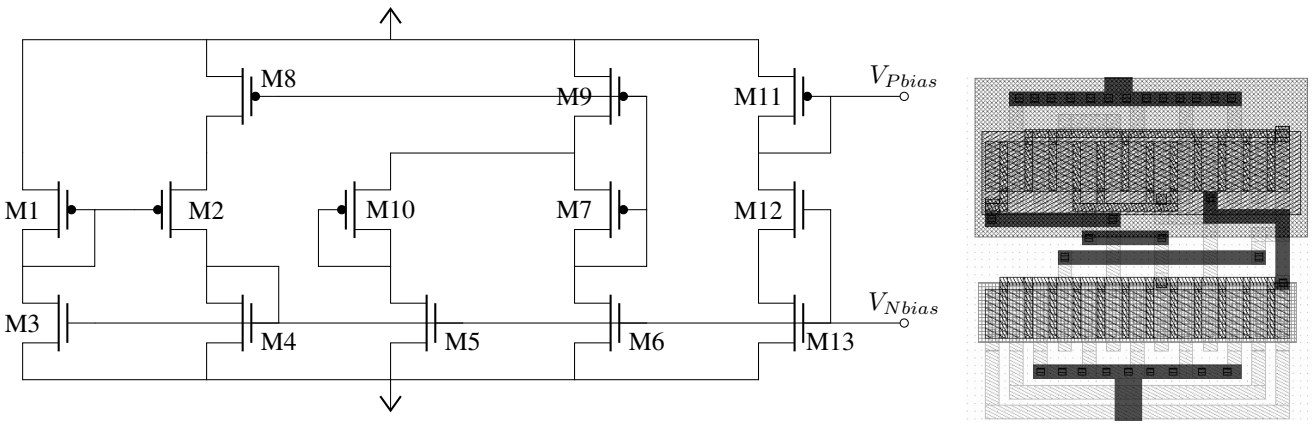


Fig. 10. Proposed nano scale self biased temperature and voltage independent low power current reference.

TABLE II
PROPOSED CIRCUIT TRANSISTOR SIZE

Transistor	Width (μm)	Length (μm)
M_1, M_9	60	3
M_2	300	3
M_{10}	252	3
M_3	6	3
M_12	250	3
M_4, M_5, M_6, M_{13}	6	3
M_7, M_{11}	6	3
M_8	4	150

to its gate, incoming from the voltage divider cell. Assuming M_2 is in the strong inversion region, the output current can be expressed by (13) and (14).

$$I = \beta V_{DS2}(V_{GS2} - V_t) \tag{13}$$

With
$V_{GS2} = V_{GS} + \eta V_t ln\left(\frac{K_4}{K_3}\right)$, and
$V_{DS2} = \eta V_t ln\left(\frac{K_5}{K_1}\right)$

$$I = \beta\eta V_t ln\left(\frac{K_5}{K_1}\right)\left(V_{GS1} + \eta V_t ln\left(\frac{K_4}{K_3}\right) - V_t\right) \tag{14}$$

B. Simulation Results

Simulation tools were used to verify the performance of the proposed circuit, as described in Section II.A Materials.

Simulation results (see Fig. 11), show that I_P, the current reference sourced from the p-type transistors, can keep a constant current as long the power source is superior to 1.6V. In reflection, I_N generates a very similar current, indicating this current reference circuit as moderately suitable for analog/digital design.

In addition to the first simulations, more specific verifications were conducted. With the ambient temperature (20°C) as a reference point, the current reference was simulated with temperature variations from -20 to 60°C. This temperature range is identified as extreme working condition of the system. The results are exhibited in Fig. 13, showing the accentuated disparities on I_N.

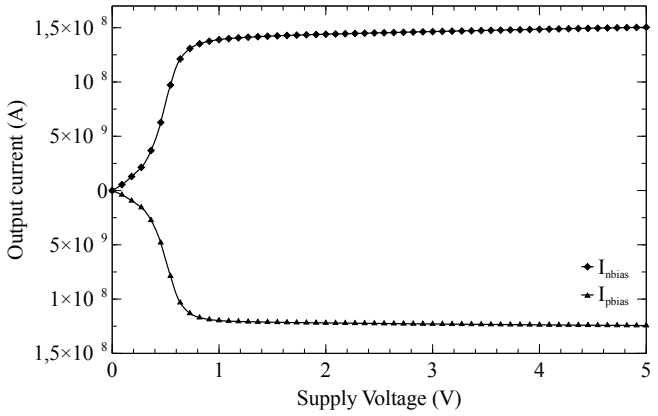


Fig. 11. Simulation results depending on source voltage at ambient temperature of circuit in Fig. 10.

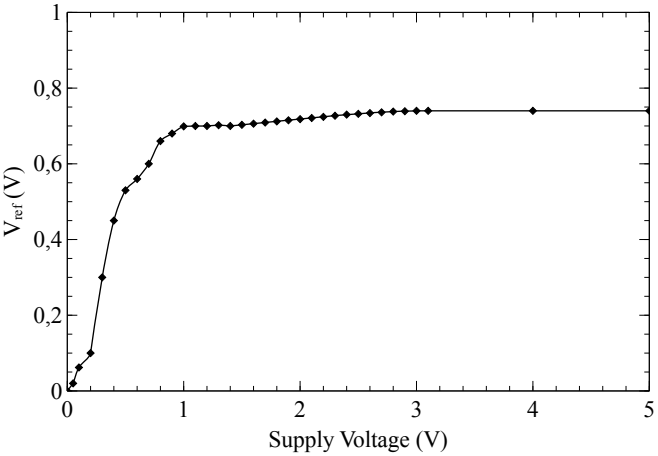


Fig. 12. Voltage reference results at ambient temperature.

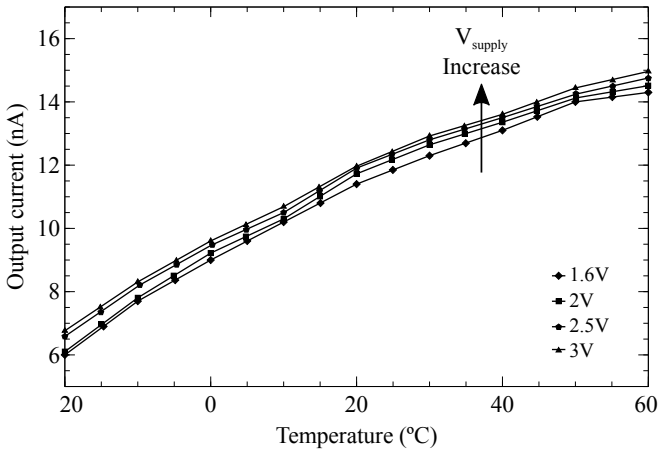


Fig. 13. Measured current with temperature variation.

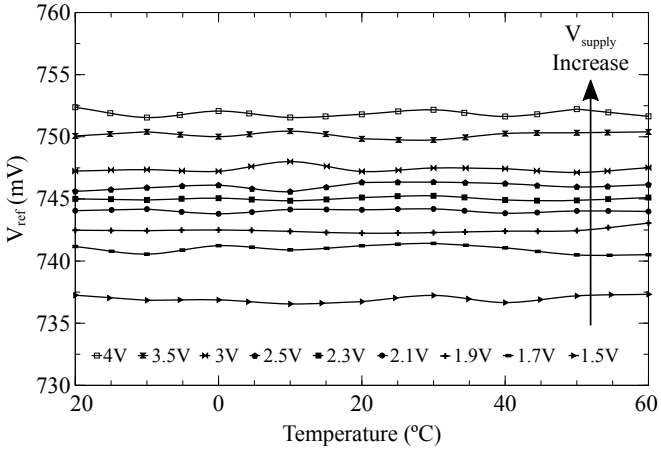


Fig. 14. Voltage reference measurements with temperature variation.

The power supply rejection ratio was simulated in Fig. 15, with a voltage supply of 3 V and a filtering capacitor, $C_f = 1pF$, the rejection ratio at 100Hz was checked to be around 45dB. The results show the power supply independence capability of the current reference.

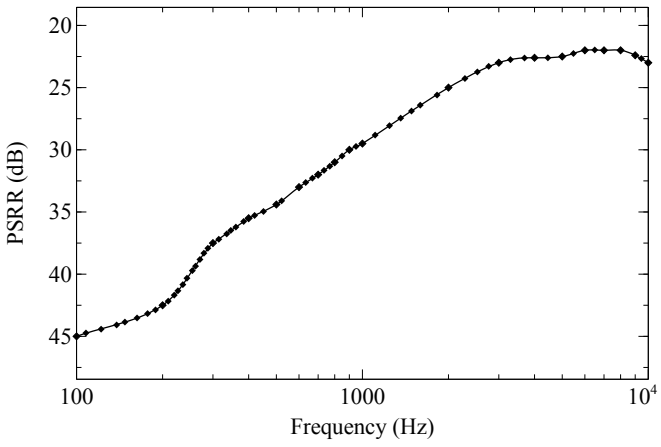


Fig. 15. Simulation results of the power supply rejection ratio depending on the frequency.

C. Layout design

The circuit layout (see Fig. 10) was designed according to rules imposed by the CMOS technology process guidelines. These rules are intrinsic to the device transistors, which can limit the performance of the applications, however, can also be useful when implementing references using the intrinsic, unchangeable values.

In order to ensure a further development of this design, scalable CMOS rules based on the λ parameter were used. Over time, CMOS processes incline to be outdated and be replaced by better processes, smaller in size and better performance with lower power consumption. The design used cannot guarantee full compatibility with the newer processes. Nevertheless, it allows for faster integration with small modifications to the original layout.

IV. Discussion

The proposed current reference is planned to be used in a piezoelectric energy harvester interface [2]. The current reference is an attempt at combining benefits from the research in Section II in a single design. A direct comparison is possible, between the original concepts and the presented final circuit.

One essential objective for the design is the temperature independence of the circuit. A square-rooting interface was incorporated in the design without challenges. The temperature stability is achieved by using two intrinsic voltages available with reversed temperature coefficients.

The temperature coefficient of the present design is calculated at 425 $ppm/°C$, a better outcome than the 1190 $ppm/°C$ result reported by [13]. Further temperature variation can be seen from the simulations results in Fig. 13. This graphical report shows a slight deviation for the current output upon simulated temperature changes.

Fabrication process discrepancies are also taken into account. Supplementary experimentation is necessary to confirm the deviations created by the fabrication. Although, the techniques and criteria used in the design should establish a reasonably stable device. The circuit is realized without resistors, a component in CMOS technology responsible for significant anomalies. The previously considered approach, switched capacitor method, was dismissed. The technique expanded the integrated circuit area considerately. Acknowledging the benefits, process stability, versus the disadvantages, expanded area and wasted power. It was deemed inappropriate for the application.

The main goal of creating a low power current reference, capable of achieving a nanoampere current output, was achieved. As shown in the results section, the circuit produces a nominal current of 12 nA when compared to researches as [13] and [34], the circuit attains a similar output performance. However, the proposed new circuit incorporates features which are not available in these similar circuits.

An overview comparison is available in TABLE III. The proposed circuit measured values are compared to similar circuits, acquired from cited literature.

TABLE III
RESEARCH COMPARISON

Parameters	Proposed Circuit	Hirose et. al [13]	De Vita et. al [34]	Sansen et. al [35]	Georgiou et. al [36]
CMOS Technology (μm)	0.35	0.35	0.35	3	0.8
Output Current (nA)	12	9.95	9.14	774	430
Minimum Supply Voltage (V)	1.6	1.3	1.5	3.5	2.5
Supply Current (nA)	54	68	37	2000	860
Current TC ($ppm/^{\circ}C$)	425	1190	44	375	600

V. CONCLUSION

A high efficiency and low power current reference was designed, outputting a stable current reference in the range of $9-12nA$. Compared to previous research, this circuit performs in the normal range, for its purpose, especially with the chosen technology.

The circuits presented a high correlation between analytical and simulation results. During simulations, a sensitivity analysis was performed and included, resulting in measured robustness. The proposed design is suitable for the polarization of low and ultra-low power consumption CMOS circuits. These are also suitable for low voltage operation. Additionally, the integration of the reference cell to CMOS circuit designs should be straightforward, even with already existing designs.

The circuit used CMOS technology, taking advantage of the sub-threshold region of CMOS transistors. The design was developed for application in energy harvesting interfaces and wireless sensor networks, although it has, likewise, applications for medical or personal mobile devices.

The Research work focused on power consumption reduction and output stability. The final layout design is ready for fabrication, continuing the use of the CMOS technology chosen for the simulations. The future work of this project involves production testing of an integrated circuit, using the $0.35\mu m$ CMOS technology process, to demonstrate the circuit functionality in real-world applications, and comparison with the obtained results from the performed simulations.

REFERENCES

[1] S. Chalasani and J. M. Conrad, "A survey of energy harvesting sources for embedded systems," in *IEEE SoutheastCon 2008*. IEEE, 2008, pp. 442–447.

[2] P. Li, Y. Wen, W. Yin, and H. Wu, "An upconversion management circuit for low-frequency vibrating energy harvesting," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 7, pp. 3349–3358, 2014.

[3] F. S. Gr, J. C. Simóes, H. Berntsen, L. E. Roseng, T. Dong *et al.*, "Low power consumption device for biological stability monitoring in drinking water," in *2018 40th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC)*. IEEE, 2018, pp. 3841–3844.

[4] F. Dell'Anna, T. Dong, P. Li, W. Yumei, Z. Yang, M. R. Casu, M. Azadmehr, and Y. Berg, "State-of-the-art power management circuits for piezoelectric energy harvesters," *IEEE Circuits and Systems Magazine*, vol. 18, no. 3, pp. 27–48, 2018.

[5] M. Penella and M. Gasulla, "A review of commercial energy harvesters for autonomous sensors," in *2007 IEEE instrumentation & measurement technology conference IMTC 2007*. IEEE, 2007, pp. 1–5.

[6] K. Roy and S. C. Prasad, *Low-power CMOS VLSI circuit design*. John Wiley & Sons, 2009.

[7] Y. Taur, "The incredible shrinking transistor," *Ieee Spectrum*, vol. 36, no. 7, pp. 25–29, 1999.

[8] K. Kaur and A. Noor, "Strategies & methodologies for low power vlsi designs: a review," *International Journal of Advances in Engineering & Technology*, vol. 1, no. 2, p. 159, 2011.

[9] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deep-submicrometer cmos circuits," *Proceedings of the IEEE*, vol. 91, no. 2, pp. 305–327, 2003.

[10] A. P. Chandrakasan and R. W. Brodersen, "Minimizing power consumption in digital cmos circuits," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 498–523, 1995.

[11] B. Davari, R. H. Dennard, and G. G. Shahidi, "Cmos scaling for high performance and low power-the next ten years," *Proceedings of the IEEE*, vol. 83, no. 4, pp. 595–606, 1995.

[12] M. Anis and M. Elmasry, *Multi-Threshold CMOS Digital Circuits Managing Leakage Power*. Springer, 2003, vol. 3.

[13] T. Hirose, Y. Osaki, N. Kuroki, and M. Numa, "A nano-ampere current reference circuit and its temperature dependence control by using temperature characteristics of carrier mobilities," in *ESSCIRC, 2010 Proceedings of the*. IEEE, 2010, pp. 114–117.

[14] B.-S. Song and P. Gray, "A precision curvature-compensated cmos bandgap reference," in *1983 IEEE International Solid-State Circuits Conference. Digest of Technical Papers*, vol. 26. IEEE, 1983, pp. 240–241.

[15] C. Yoo and J. Park, "Cmos current reference with supply and temperature compensation," *Electronics Letters*, vol. 43, no. 25, pp. 1422–1424, 2007.

[16] E. M. Camacho-Galeano, C. Galup-Montoro, and M. C. Schneider, "A 2-nw 1.1-v self-biased current reference in cmos technology," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 52, no. 2, pp. 61–65, 2005.

[17] P. Li, Y. Wen, C. Jia, and X. Li, "A magnetoelectric composite energy harvester and power management circuit," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2944–2951, 2011.

[18] Z. Yang, E. Halvorsen, and T. Dong, "Electrostatic energy harvester employing conductive droplet and thin-film electret," *Journal of Microelectromechanical Systems*, vol. 23, no. 2, pp. 315–323, 2014.

[19] ——, "Power generation from conductive droplet sliding on electret film," *Applied Physics Letters*, vol. 100, no. 21, p. 213905, 2012.

[20] T. Zhou, T. Dong, Y. Su, and Y. He, "A cmos readout with high-precision and low-temperature-coefficient background current skimming for infrared focal plane array," *IEEE Transactions on Circuits and Systems for Video Technology*, vol. 25, no. 8, pp. 1447–1455, 2015.

[21] T. Dong and N. M. M. Pires, "Immunodetection of salivary biomarkers by an optical microfluidic biosensor with polyethylenimine-modified polythiophene-c70 organic photodetectors," *Biosensors and Bioelectronics*, vol. 94, pp. 321–327, 2017.

[22] Y. P. Tsividis and R. W. Ulmer, "A cmos voltage reference," *IEEE Journal of Solid-State Circuits*, vol. 13, no. 6, pp. 774–778, 1978.

[23] E. Vittoz and J. Fellrath, "Cmos analog integrated circuits based on weak inversion operations," *IEEE journal of solid-state circuits*, vol. 12, no. 3, pp. 224–231, 1977.

[24] H. J. Oguey and D. Aebischer, "Cmos current reference without resistance," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 7, pp. 1132–1135, 1997.

[25] T. Sakurai and A. R. Newton, "A simple mosfet model for circuit analysis," *IEEE transactions on Electron Devices*, vol. 38, no. 4, pp. 887–894, 1991.

[26] S. K. Saha, "Modeling process variability in scaled cmos technology," *IEEE Design & Test of Computers*, vol. 27, no. 2, pp. 8–16, 2010.

[27] P. Jespers, *The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches*. Springer Science & Business Media, 2009.

[28] M. V. Dunga, C.-H. Lin, X. Xi, D. D. Lu, A. M. Niknejad, and C. Hu, "Modeling advanced fet technology in a compact model," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 1971–1978, 2006.

[29] A. Scholten, G. Smit, M. Durand, R. Van Langevelde, C. Dachs, and D. Klaassen, "A new compact model for junctions in advanced cmos technologies," in *IEEE InternationalElectron Devices Meeting, 2005. IEDM Technical Digest.* IEEE, 2005, pp. 4–pp.

[30] K. Bult and H. Wallinga, "A class of analog cmos circuits based on the square-law characteristic of an mos transistor in saturation," *IEEE Journal of solid-state circuits*, vol. 22, no. 3, pp. 357–365, 1987.

[31] E. Seevinck and R. F. Wassenaar, "A versatile cmos linear transconductor/square-law function," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 3, pp. 366–377, 1987.

[32] S. Takagi, T. Tezuka, T. Irisawa, S. Nakaharai, T. Numata, K. Usuda, N. Sugiyama, M. Shichijo, R. Nakane, and S. Sugahara, "Device structures and carrier transport properties of advanced cmos using high mobility channels," *Solid-State Electronics*, vol. 51, no. 4, pp. 526–536, 2007.

[33] H.-W. Huang, C.-Y. Hsieh, K.-H. Chen, and S.-Y. Kuo, "A 1v 16.9 ppm/ c 250na switched-capacitor cmos voltage reference," in *2008 IEEE International Solid-State Circuits Conference-Digest of Technical Papers*. IEEE, 2008, pp. 438–626.

[34] G. De Vita and G. Iannaccone, "A 109 nw, 44 ppm/ c cmos current reference with low sensitivity to process variations," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*. IEEE, 2007, pp. 3804–3807.

[35] W. M. Sansen, F. Op't Eynde, and M. Steyaert, "A cmos temperature-compensated current reference," *IEEE Journal of Solid-State Circuits*, vol. 23, no. 3, pp. 821–824, 1988.

[36] J. Georgiou and C. Toumazou, "A resistorless low current reference circuit for implantable devices," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, vol. 3. IEEE, 2002, pp. III–III.