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Single Phase NPC Inverter Controller with Integrated MPPT for PV Grid Connection

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***Abstract*— This paper presents a single-stage three-level Neutral Point Clamped (NPC) inverter for connection to the electrical power grid, with integrated Maximum Power Point Tracking (MPPT) algorithm to extract the maximum power available from solar photovoltaic (PV) panels. This single-stage topology is more compact than the traditional topology, it was chosen because with the proper control strategy. It is suitable to connect the PV panels to the power grid. The paper describes the design of a 5 kW NPC inverter for the interface of PV panels with the power grid, presenting the circuit parameters and the description of the control algorithms. A phase locked loop control is used to connect the inverter into the grid. Then, a proposed DC Link voltage control to regulate the input voltage of the inverter. Although an MPPT algorithm was used to optimize the energy extraction and the system efficiency. Inverter Output Current control to produce an output current (current injected in the power grid) with low Total Harmonic Distortion (THD) implemented in a DSP. Simulation and experimental results verify the correct operation of the proposed system, even with fluctuations in the solar radiation.**

***Keywords*—Photovoltaic System; Maximum Power Point Tracking (MPPT); Neutral Point Clamped (NPC) Inverter; Phase-Locked Loop (PLL).**

I. Introduction

As the population in the world increases, the renewable energy sources acquire growing importance due to the global energy demand. In the last years, global warming and energy policies have become a hot topic on the international agenda as countries are making an effort to reduce the greenhouse gas emissions.

Solar and wind energy sources have become very popular as result of the increasing research on new technologies, namely photovoltaic (PV) power generation technologies that are being widely studied. Despite the achieved developments in solar technologies further improvements can be done in order to lower their price, increase efficiency and maximize the energy extraction. In most cases, grid connected PV systems consist in the PV panels array and a power converter. Several topologies of converter can be adopted.

Transformerless solutions are the most commonly adopted because of the high performance in terms of efficiency, higher reliability, smaller size and weight, and lower price [1,2]. It exist different commercial inverters topologies used in PV systems [3]. For the H5 inverter which is commercialized by SMA. It is a classical H-bridge with an extra fifth switch in the positive bus of the DC-link. Moreover, the HERIC (Highly efficient and Reliable Inverter Concept) inverter is currently commercialized by Sunways. It is also derived from the classical H-bridge by adding a bypass leg in the AC side using two back-to-back IGBTs. Furthermore, the REFU inverter from Refusol also derived from H-bridge. It uses a half bridge within the AC side bypass and bypassable DC-DC converter [3]. All these inverters convert the two levels H-bridge inverter into a three level one for less output voltage stress. Somewhere else, the neutral point camped (NPC) inverter achieve the lower switch stress and can be used in both single phase and three phase inverters. In addition, NPC inverters topologies are of interest due to their lower output current total harmonic distortion (THD), the use of semiconductors in less stressing conditions and the lower switching frequencies [4].

The aim of this paper is to present the design and implementation of the proposed single-stage three-level Neutral Point Clamped (NPC) inverter system that is used to interface a PV system with the electrical grid. The topology of the inverter is analyzed and the proposed control techniques are explained.

II. Neutral Point Clamped Inverter

The multilevel inverters can be divided in three main topologies: flying capacitor, cascaded H-bridge and diode clamped multilevel inverters [5]. Neutral Point Clamped (NPC) inverter topology is used in this paper as shown in Fig.1. This type of multilevel inverter has the advantages of being simpler and cheaper when compared with other topologies. Besides this, the voltage on the switching power semiconductors, is half of the DC-link voltage and the output voltage and current have reduced THD [6,7], with smaller passive filter requirements [7].

Due to the diodes connected to the neutral point N, the voltage across the switching power semiconductors is $V_{DC}/2$,

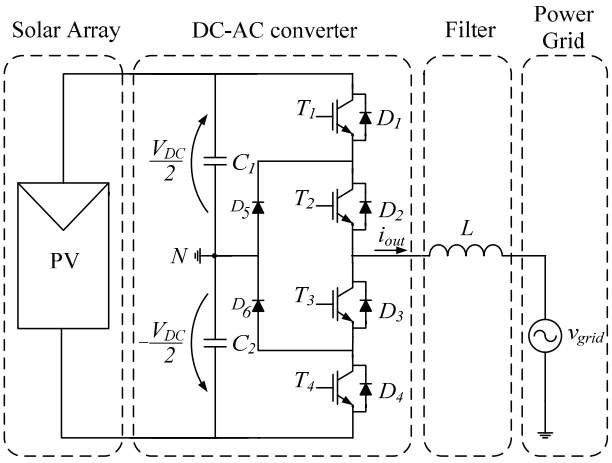

Figure 1. Implemented NPC converter for photovoltaic system.

and consequently the output voltage levels achievable in this topology are: $-V_{DC}/2$, 0 and $V_{DC}/2$.

The switching states of the single-phase three levels NPC inverter are shown in table I. The switches T_1 and T_3, and T_2 and T_4, are switched complementary. The control of this inverter can be done using a PWM technique. To implement the PWM are used two superposed triangular carriers. Each carrier is connected to one of two groups of switches controlled complementarily. The positive part of the carrier fixes the switching state of T_1 and T_3 whereas the negative part controls T_2 and T_4.

For a good operation of the NPC inverter, the DC-link capacitors must have an equal voltage. Furthermore, when the ripple of the DC-link is high, the output current can be difficult to control. The ripple happens due to the charging and discharging of the DC-link capacitors. This paper used a single-stage topology without a DC-DC power converter between the panels and the NPC inverter, therefore the inverter control integrates the current control and the Maximum Power Point Tracking algorithm.

III. The Proposed NPC Inverter Control System

The control system of the proposed topology is composed by four main blocks:

-Phase-locked Loop (PLL) to synchronize the output voltage with the electrical power grid voltage;

-DC-link voltage regulation;

-Maximum Power Point Tracking (MPPT) control to impose the reference current to be injected in the grid;

TABLE I. Switching States of a Single Phase Three Level NPC Inverter

Output voltage	Switches on	Output current	Current path
$V_{DC}/2$	T_1 and T_2	$i_{out}>0$	T_1, T_2
		$i_{out}<0$	D_1, D_2
0	T_2 and T_3	$i_{out}>0$	D_5, T_2
		$i_{out}<0$	D_6, T_3
$-V_{DC}/2$	T_3 and T_4	$i_{out}>0$	D_4, D_3
		$i_{out}<0$	T_4, T_3

-Inverter output current controller.

The block diagram of the implemented control system is shown in Fig.2.

The MPPT algorithm imposes the reference current to the current controller. This reference is added to the output of the DC-link voltage control. The resultant reference signal is multiplied by the unitary sinusoidal value from the PLL. The current control imposes the modulator reference waveform for the PWM block.

A. Phase-Locked Loop

To ensure the proper injection of current into the power grid is necessary to have a grid synchronization mechanism, i.e., to have information about the phase and frequency of the power grid voltage.

Different types of PLL have been developed and presented in literature [8,9]. In the proposed system an enhanced Phase-locked loop (E-PLL) was adapted to extract the fundamental components (phase angle and frequency) of the power grid voltage [10]. The E-PLL is less sensitive to power grid voltage distortion and is adapted to be used in practical applications with noisy conditions [11]. A block diagram of the E-PLL is shown in Fig.3.

The output signal of the E-PLL can be described as:

$$v_{PLL} = V_{PLL}\sin(\varphi_{PLL}) \tag{1}$$

This signal is in phase with the power grid voltage fundamental given by:

$$v_{grid} = V_{grid}\sin(\varphi_{grid}) \tag{2}$$

Where, V_{grid} is the peak value of the power grid voltage, and φ_{PLL} is the phase angle. The error between the power grid voltage and the output PLL signal can be expressed as:

$$\varepsilon_1 = V_{grid}\sin(\varphi_{grid}) - V_{PLL}\sin(\varphi_{PLL}) \tag{3}$$

The output signal of the phase detector is:

$$\varepsilon_2 = \varepsilon_1\cos(\varphi_{PLL}) \tag{4}$$

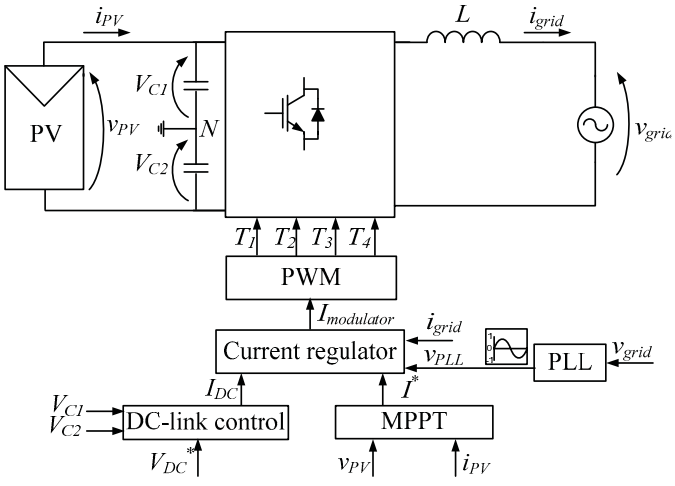

Figure 2. Block diagram of the NPC converter control system.

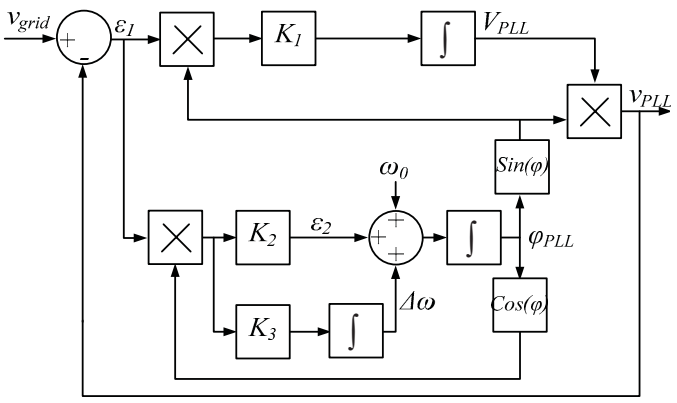

Figure 3. Block diagram of the E-PLL.

In steady state, $\varphi_{PLL} = \varphi_{grid}$, and so:

$$\varepsilon_1 = v_{grid} - v_{PLL} = 0 \tag{5}$$

The phase φ_{PLL} that is estimated by the PLL will be the phase angle of the reference output current injected into the grid which is:

$$i_{ref}^{*} = i_f^{*} \times \sin(\varphi_{PLL}) \tag{6}$$

Where i_f^* is the amplitude of the fundamental component of the reference current which is equal to:

$$i_f^{*} = I^{*} + I_{DC} \tag{7}$$

Where I^* is the PV current reference given by the MPPT algorithm and I_{DC} is the current reference given by the DC-link regulation.

The constant K_1 adjusts the amplitude convergence of the grid while K_2 and K_3 adjust the frequency and phase convergence.

B. Maximum Power Point Tracking MPPT

The maximum power supplied by the photovoltaic panels is not stable in the same operating point, whereas it varies with the weather conditions, such as solar irradiation and temperature. To extract the maximum power is necessary to implement a MPPT algorithm that dynamically adjusts the extraction of the power. Several MPPT algorithms have been studied by different authors, namely: Perturb and Observe (P&O), Fuzzy Logic, Neural Networks, Genetic Algorithm and Lagrange Multiplier [12-15]. In the proposed system was applied the Incremental Conductance algorithm in order to track the Maximum Power Point (MPP). The advantages of using this method are the higher efficiency and fast tracking of the MPP in comparison with other algorithms [16].

The incremental conductance method is based on the principle that the slope of the PV array power curve is zero at the MPP, so that $\Delta P/\Delta V = 0$, with $P = V I$.

Considering that:

$$\begin{cases} \Delta I/\Delta V = -I/V & \text{if} \quad P = \text{MPP} \\ \Delta I/\Delta V > -I/V & \text{if} \quad P < \text{MPP} \\ \Delta I/\Delta V < -I/V & \text{if} \quad P > \text{MPP} \end{cases} \tag{8}$$

The MPP can be tracked by comparing the instantaneous conductance I/V with the incremental conductance $\Delta I/\Delta V$.

The algorithm increments or decrements the reference until the condition $\Delta I/\Delta V = -I/V$ is achieved. Once the maximum power is reached, the operation of the PV array is maintained at this point. It is an effective algorithm and requires high sampling rates and fast calculations of the power slope [16]. It offers different advantages which are good tracking efficiency and automatic adjustment of the module operating voltage with no oscillations. Also, the response is improved and the control for the extracted power is optimized [17]. The implementation of this algorithm in the control unit was difficult and expensive, but with recent developments in microcontrollers it became more cost effective [18]. It lends itself well to DSP control, which can easily keep track of previous values of voltage and current [19].

C. DC-link Voltage Control

In order to ensure that the system does not become unusable, an optimized DC-link voltage equalization control, shown in Fig.2 is proposed. The controller imposes an increment or a decrement value added to the current reference, so that the voltage of the capacitors is approximately equal. To control the DC-link voltages, is used a PI controller for each capacitor voltage regulation and a digital filter to V_{C1} and V_{C2}. The reference voltage is given by:

$$V_{DC}^{*} = V_{C1} + V_{C2} \tag{9}$$

The error is then calculated according to the polarity of the PLL reference (10). This proposed method ensures that the regulation of the DC-link voltage does not affect the output current waveform. The minimum DC-link capacitance leads to larger voltage ripples. Nevertheless, such ripples were found to be within acceptable limits to run the inverter and the output current distortion has an acceptable level given in interconnection standards (IEC, IEEE, etc…).

$$e_V(t) = \begin{cases} \dfrac{V_{DC}^{*}}{2} - V_{C1avg} & \text{if} \quad v_{PLL} > 0 \\ \dfrac{V_{DC}^{*}}{2} - V_{C2avg} & \text{if} \quad v_{PLL} < 0 \end{cases} \tag{10}$$

The PI algorithm can be expressed in the continuous time domain as:

$$u_V(t) = K_p e_V(t) + K_i \int_{\tau=0}^{t} e_V(\tau) d\tau \tag{11}$$

The control is implemented in a DSP, therefore the PI controller must be implemented in discrete time. Considering the integration method of Forward Euler the PI can be expressed as:

$$u_V(k) = K_p e_V(k) + K_i T_s [e_V(k) + e_V(k-1)] \tag{12}$$

Where $T_s = 1/f_s$, with switching frequency f_s = 32 kHz.

D. Current Control

To connect the inverter into the power grid, is necessary to control the output current so that the power can flow from the

inverter to the power grid. The performance of the inverters connected to the grid in terms of THD current (Total Harmonic Distortion) depends largely on the control strategy applied. thus, it exists in the literature different types of control such as predictive, hysteresis, periodic sampling, resonant controller and PI current control [20,21]. This paper presents the PI current controller because it is the most common and widely used type of controller, and because of its simplicity. It consists in comparing the output current of the inverter with the reference current that is imposed by the other parts of the control system.

The reference current is given by:

$$i_{ref}^{*} = u_V(t) + I^{*} \tag{13}$$

The error can be expressed as:

$$e_I(t) = i_{ref}^{*} - i_{grid} \tag{14}$$

The PI algorithm can be expressed in the continuous time domain as:

$$u_I(t) = K_p e_I(t) + K_i \int_{\tau=0}^{t} e_I(\tau) d\tau \tag{15}$$

Considering the backward Euler integration method the PI control can be expressed as:

$$u_I(k) = K_p e_I(k) + K_i T_s [e_I(k) + e_I(k-1)] \tag{16}$$

Where $T_s = 1/f_s$ with $f_s = 32$ kHz.

IV. Simulations Results

In order to obtain a good characterization of the proposed topology, simulations were performed using PSIM software. The system was simulated under different operating conditions, in steady state and during transient state caused by solar radiation variations. All of aforementioned control loops (PLL, MPPT, DC-link and current control) were implemented using the programming language C. This approach gives to the simulations a behavior that is similar to the practical application since the algorithms implementations are almost the same. The simulated algorithms can be easily directly exported to a DSP.

The inverter was designed to have a nominal power of 5.7 kW. All the circuit parameters are presented in table II.

TABLE II. Circuit Parameters

Parameters	Value	Units
Number of panels in series	23	--
Series resistance	0.0065	Ω
Shunt resistance	1000	Ω
Short circuit current	7.74	A
Open circuit voltage	991.3	V
Maximum power	5750	W
Capacitors (C_1 and C_2)	470	µF
Inductance (L)	5	mH
Power grid voltage (rms)	230	V
Power grid frequency	50	Hz
Power grid inductance	100	µH
Power grid resistance	0.03	Ω

The L filter was designed to reduce the current distortion caused by the high switching frequencies of the IGBTs which is equal to 16 KHz. A sinusoidal pulse-width modulation SPWM was used to control the power semiconductors switching.

Fig.4 shows the synchronization of the PLL with the power grid voltage. When the system reaches the permanent state, the PI control output will be zero and the output of the integrator will vary between 0 and 2π.

In Fig.5 are presented the output current, voltage and

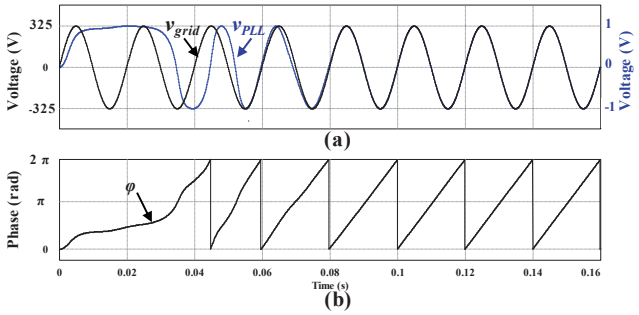

Figure 4. Block diagram of the E-PLL.

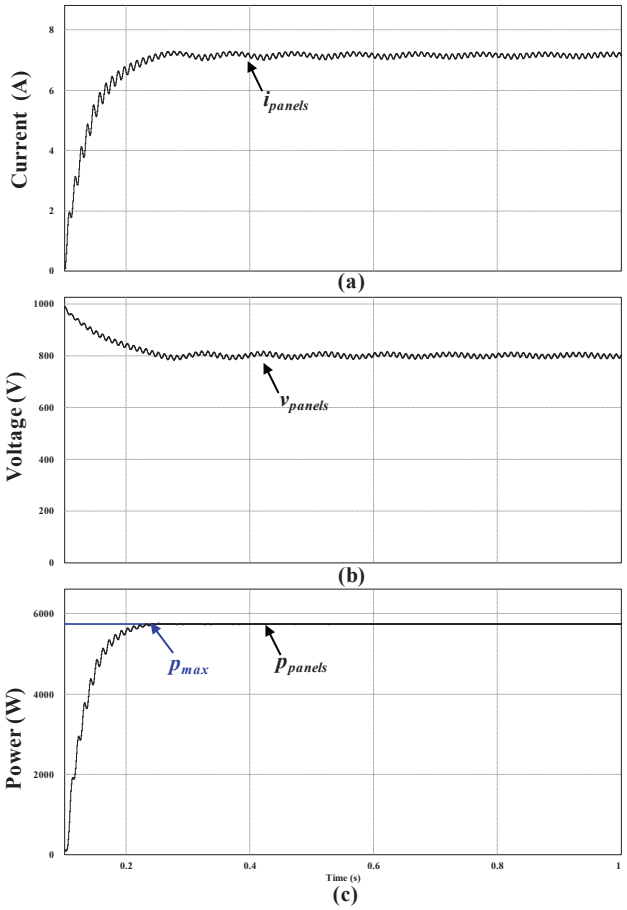

Figure 5. Startup of the proposed system with maximum solar radiation: (a) PV current (i_{panels}); (b) PV panels voltage (v_{panels}); (c) PV panels power (p_{panels}).

power of the solar panels array during the startup of the proposed system, with a maximum solar radiation of 1000 W/m². It can be seen that the power of the solar panels grows steadily without a significant ripple.

The current from the panels also increases in a controlled way. The system output power grows from zero to the maximum power in 0.25 s. The voltage in the solar panels array decreases until reaching the point of maximum power. The current extracted from the panels is stable with a ripple of 7%. The extracted power follows the maximum theoretical power of the system and has an average value of 5746 W.

It was intended to test the behavior of the system when a fluctuation in the solar radiation occurs. For that it was made a simulation in which it was imposed a fluctuation by levels on the solar radiation from the maximum power of 1000 W/m² to 600 W/m², passing through a value of 800 W/m², as shown in Fig.6. It can be seen that the extracted power follows the maximum available power, this way validating the MPPT algorithm.

The peak value of the current injected into the power grid is 35 A. Fig.7 shows the waveform of the inverter output current (i_{out}) following the reference (i_{ref}^*). It can also be seen in Fig.8 that the power factor is unitary.

Fig.9 shows the regulated voltages at the DC-link capacitors,

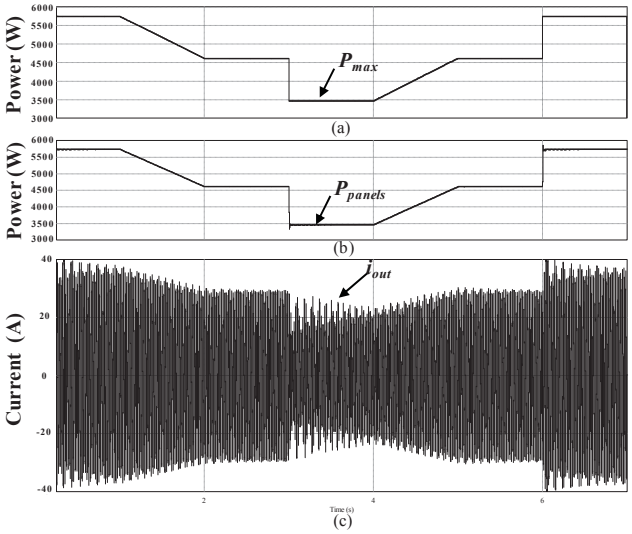

Figure 6. Operation with fluctuations in the solar radiation, from1000 W/m² to 800 W/m² and to 600 W/m: (a) Maximum theoretical power (p_{max}); (b) Extracted power PV panels (p_{panels}); (c) Inverter output current (i_{out}).

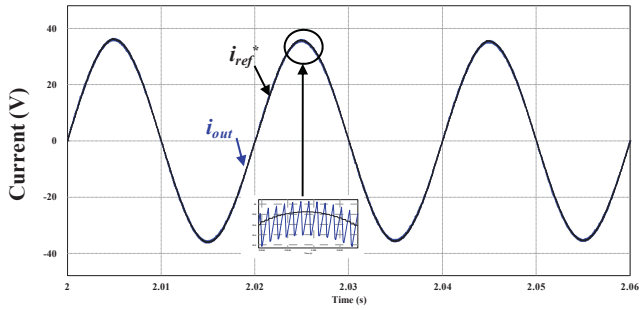

Figure 7. Reference current (i_{ref}^*) and current injected into the power grid (i_{out}).

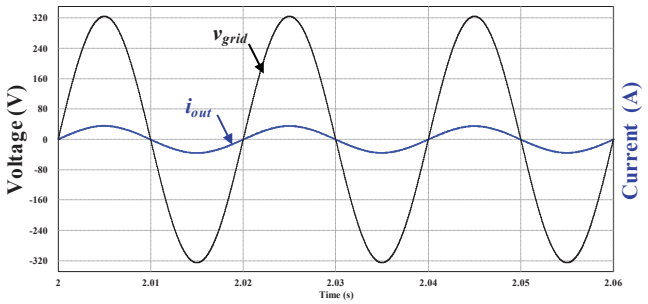

Figure 8. Power grid voltage (v_{grid}) and inverter output current (i_{out}).

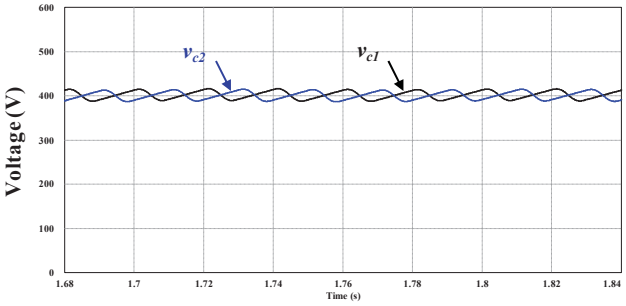

Figure 9. Voltages in the two capacitors of the DC-link (v_{c1}, v_{c2}).

with a ripple of 15%.

V. Experimental Results

The control strategy previously discussed in this paper has been implemented and tested experimentally on a single phase NPC grid connected inverter. The inverter parameters are equal to the parameters of the simulation. The IGBTs used were the *SKM50GB063D* from *SEMIKRON*. In the implementation of the digital control was used a floating-point 32 bits DSP (*TMS320F28335* from *Texas Instruments*). Fig.10 shows the NPC inverter hardware set-up. Simulation results are presented at nominal voltage of 800V DC and experimental results provided at a nominal voltage of 61.95V dc as shown in the table III, built in the laboratory.

All the experimental results that will be presented were measured using a Yokogawa DL708E oscilloscope. We first considered the implementation of the (PLL). Then, the implementation of the NPC inverter output current control.

Using an oscilloscope probe with a scale factor of (1/100), it can be seen in Fig.11 the output signal generated by the

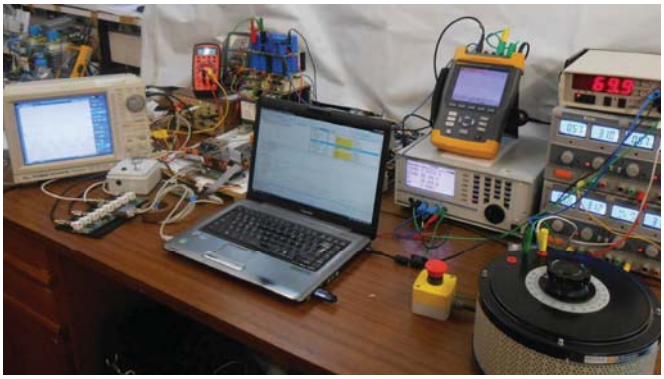

Figure 10. General view of the developed hardware setup.

TABLE III. MAXIMUM POWER EXTRACTED AND INVERTER OUTPUT CURRENT WITH MPPT IMPLEMENTATION

Voltage (V)	Resistance (Ω)	Maximum theoretical power(W)	Measured power (W)	Output measured current(A)
61.95	100	9.59	9.58	2.2
	80	11.99	12.00	2.6
	60	15.99	16.53	3
	40	23.98	22.27	3.67

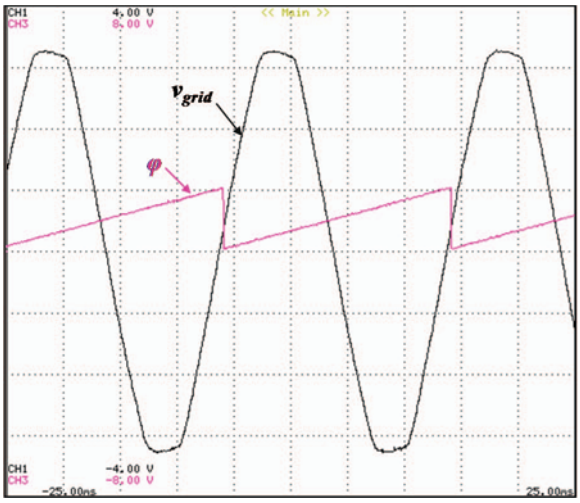

Figure 11. Power grid voltage (v_{grid}) (100 V/div) and phase generated by the PLL (φ) (6.28 V/div).

oscillator controller (φ), has the same phase and frequency of the power grid voltage (v_{grid}), assuming values between 0 and 2π.

In Fig.12 is shown the output signal of the PLL (v_{PLL}) devided by the amplitude V_{grid} which is synchronized with the input signal (v_{grid}).

After the validation of the PLL algorithm the output current

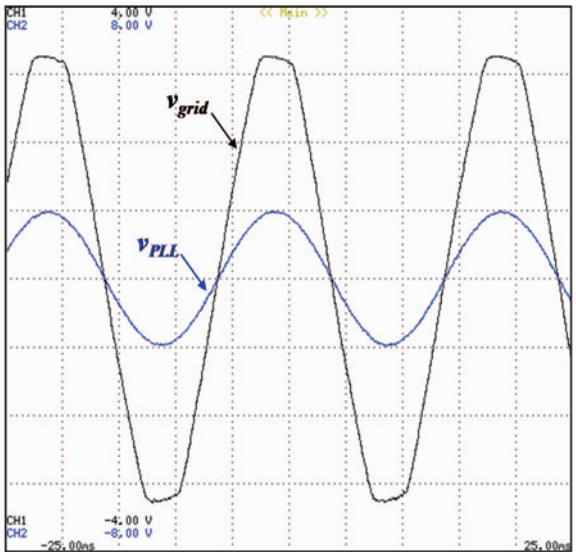

Figure 12. Power grid voltage (v_{grid}) (100 V/div) and PLL output signal (v_{PLL}) (1 V/div).

and DC-link controls were validated. The voltages of the two DC-link capacitors are balanced as expected and the THD of the output current is equal to 2.2 % as it is shown in Fig.13.

To validate the proper operation of the MPPT control algorithm, an ideal DC voltage source was used in series with a variable resistor to simulate a non ideal voltage source in order to change the maximum power supplied. The maximum power point occurs when the equivalent resistance of the NPC inverter is equal to the rheostat resistance (this operation assume the matching power), or to supply the inverter is seen as an equivalent resistance.

Fig.14 shows the maximum power extracted for a given input voltage of 60 V and different value of rheostat resistance.

Table III shows the maximum power extracted which is measured by a digital power meter ISW8000 and the output current of the NPC inverter depending on the resistance value of the rheostat.

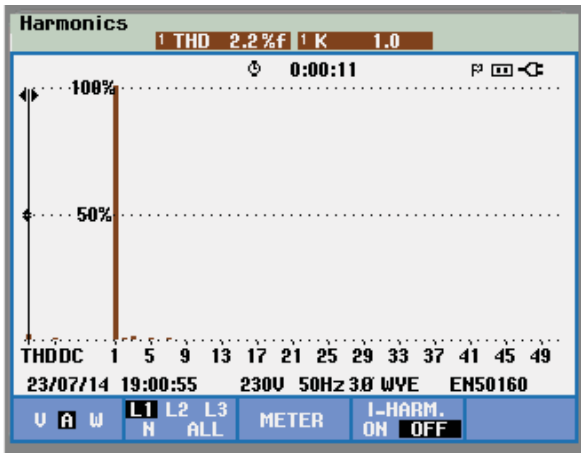

Figure 13.Total Harmonic Distorsion of the output current current

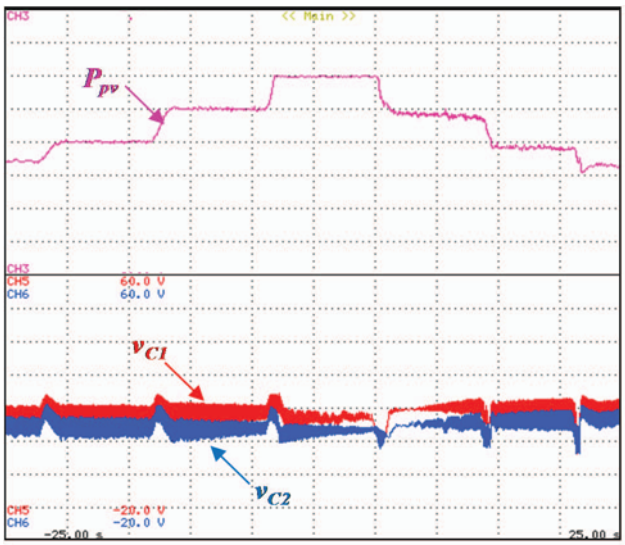

Figure 14. Maximum power extracted from the non ideal voltage source (P_{pv}) (3.8 W/div) and voltages in the two capacitors of the DC-link (v_{C1}, v_{C2}) (10 V/div).

From fig.15, fig.16, fig.17 and fig.18 we can remark that the output current follow exactly the reference current imposed by the control strategy.

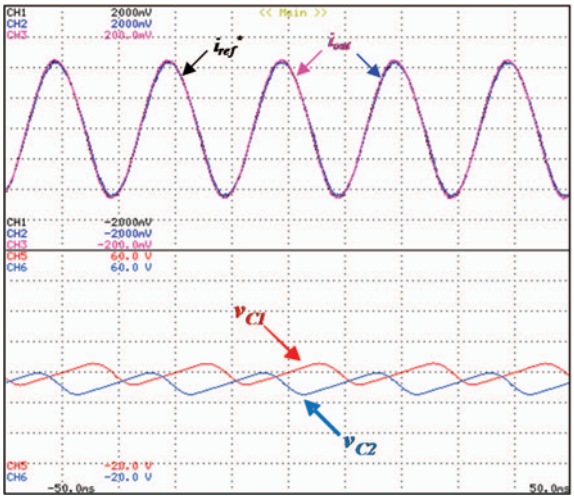

Figure 15. output current (i_{out}), reference curent (1 A /div) and voltages in the two capacitors of the DC-link (v_{C1}, v_{C2}) (10 V/div) for R=100 Ω.

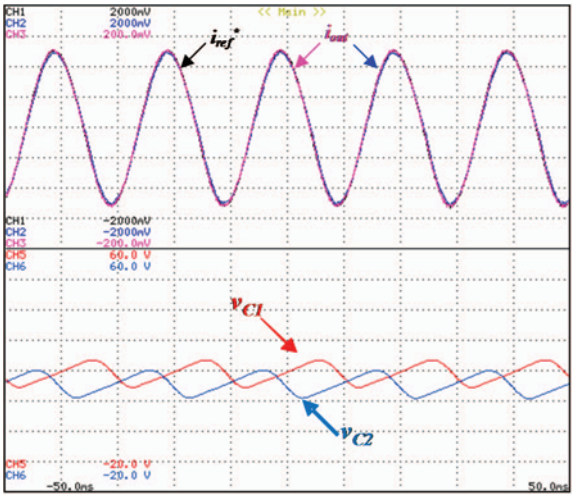

Figure 16. output current (i_{out}), reference current (1 A /div) and voltages in the two capacitors of the DC-link (v_{C1}, v_{C2}) (10 V/div) for R=80 Ω.

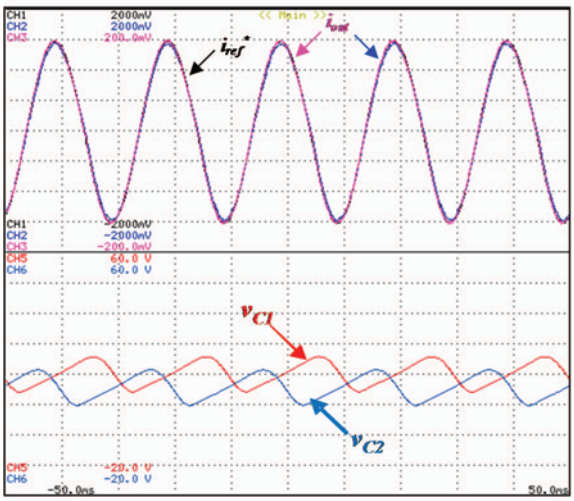

Figure 17. output current (i_{out}), reference current (1 A /div) and voltages in the two capacitors of the DC-link (v_{C1}, v_{C2}) (10 V/div) for R=60 Ω.

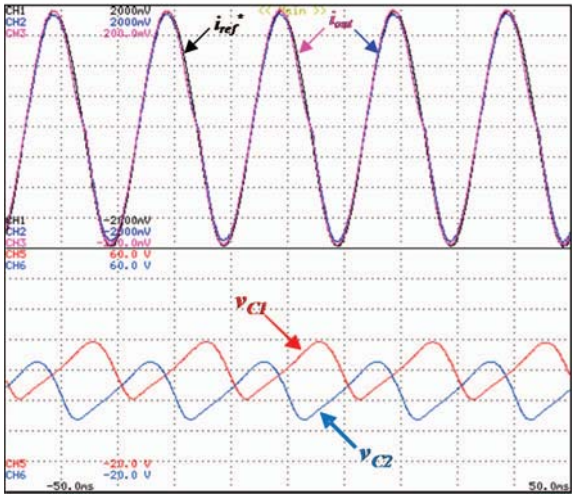

Figure 18. output current (i_{out}), reference current (1 A /div) and voltages in the two capacitors of the DC-link (v_{C1}, v_{C2}) (10 V/div) for R=40 Ω.

The inverter output current was obtained through a current probe connected to the oscilloscope with a transformation ratio of 10 mV / A. However, for a better resolution were given 5 turns on the wire around the current probe.

VI. Conclusion

This paper presents the design, simulation and experimental results of a 5 kW single-stage three-level Neutral Point Clamped (NPC) inverter for connection to the electrical power grid, with integrated Maximum Power Point Tracking (MPPT) algorithm to extract the maximum available power from solar photovoltaic (PV) panels. It also describes the design of the PLL controller, used to track the fundamental power grid voltage in order to synchronize the NPC inverter with the power grid, and to generate a reference for the inverter output current (which consists in the injected power grid current). All the controllers have been implemented using C code, validated by simulation in PSIM, and executed in a DSP. Experimental results indicate that the current injected in the power grid follows the reference, and that the voltages in the two DC-link capacitors are kept balanced. It is shown that the proposed system is able to always extract the maximum power available from the solar PV panels, even when there are solar radiation fluctuations.

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