Wafer-Level Packaging for RF Applications Using High-Resistivity Polycrystalline Silicon Substrate Technology

A. Polyakov[1], S. Sinaga[1], P.M. Mendes[1, 2], M. Bartek[1], J.H. Correia[2], and J.N. Burghartz[1]

[1]Delft University of Technology, HiTeC/DIMES, PO Box 5053, 2600 GB Delft, the Netherlands
Phone: +31-15-2789421, fax: +31-15-2623271, e-mail: a.polyakov@dimes.tudelft.nl
[2]University of Minho, Dept. of Industrial Electronics, 4800-058 Guimarães, Portugal

Abstract

High-resistivity polycrystalline silicon (HRPS) wafers are explored as a novel low-cost and low-loss substrate in Wafer-Level Chip-Size Packaging (WLCSP) for RF applications. The WLCSP solution we demonstrate is based on adhesive bonding of a HRPS wafer to a silicon wafer with active devices. After bonding, the IC wafer is thinned below 50 µm and selectively removed to expose its front-side contact pads. The HRPS wafer serves as a mechanical carrier, thermal spreader and vertical spacer in which vias are etched by DRIE to reach desired pads on the IC wafer. Then after a seed layer sputtering, a 5-10 µm Cu layer is plated on both wafer sides and patterned providing a back-side ground plane and large, front-side RF passives. Due to HRPS electrical properties, no dielectric isolation layer is required inside vias, simplifying the front-side processing. Solder bumping on the substrate back-side and singulation by dicing complete the processing. The presented concept enables integration of large RF passives with a spacing of >150 µm to the conductive silicon substrate containing the circuitry, while providing mechanical stability, reducing form factor and avoiding any additional RF loss. Antenna performance comparable to glass substrates and high quality factors for large spiral inductors (Q=11 at 1 GHz; 34 nH) are demonstrated. The HRPS substrates have high dielectric constant, low RF loss, high thermal conductivity, perfect thermal matching, and processing similar to the single-crystalline silicon.

Key words: Polycrystalline silicon, wafer-level packaging, high-resistivity silicon substrate, integrated passives, dielectric losses, substrate transfer.

Introduction

As the demand for ever-smaller electronic systems grows, manufacturers are seeking ways to increase IC integration levels and to reduce the size and weight of IC packages. The explosive expansion of mobile electronic terminals generates strong demand for high-performance, cost-effective and miniaturized RF modules providing desired functionality. Such RF ICs have set a challenge for packaging, especially at the low-end market segment where low-cost solutions are required. The chip size package (CSP) and wafer-level packaging (WLP) resulting from this effort, have been introduced into manufacturing at an unprecedented rate.

The driving force behind is not only the reduced size and weight, but primarily the fact that the wafer-level chip-size packaging (WLCSP) technology has potential of electrical performance improvement at a comparable manufacturing cost and thus providing an improved performance-to-price ratio. The same processing steps that are used to achieve the WLP technology basic packaging goal, can be adopted for implementation of additional components e.g. high-quality passives, antennas or isolation structures or protection of MEMS structures [1]. The emerging WLP technology and related integrated passive devices (IPDs) have proven to have capabilities of significant size reduction at a comparable cost and an improved electrical performance [2], [3].

Passive devices (PDs) like spiral inductors, transmission lines or antennas integrated on low to medium resistivity silicon substrates used in RF silicon processes suffer from high substrate losses degrading the achievable quality factor [4]. The substrate influence can partly be suppressed by increasing the substrate resistivity and/or increasing the device-to-substrate vertical separation. Spiral inductors integrated at the front side also consume significant part of the die area which is therefore not available for active circuitry. This makes an integrated RF PD a rather costly component.

Solution to the both above-mentioned problems can be found in using of an additional low-loss substrate serving as a spacer (thickness >100 μm) and positioning of the PDs above the active circuitry. Practically, this can be accomplished by wafer-to-wafer bonding and through-wafer electrical interconnect. Such additional fabrication steps can be economically justified if implemented as an integral part of wafer-level packaging (WLP) and balanced by the added value of PDs having increased quality factors and reduction of the total chip area.

As a candidate for low-loss material, glass substrates are often considered. Due to their low cost, availability in a wafer form, transparency and sealing properties, they are widely applied in wafer-level packaging [5]. However, limitied structuring capabilities (e.g. difficulty to make a through-substrate vias) and low thermal conductivity are the limiting factors for their application in high-performance RF ICs. High-resistivity (1-10 kΩ-cm) single crystalline float-zone silicon wafers may be used, but they are expensive and prone to surface channel effects [6].

In our previous work [7], we have shown that high-resistivity polycrystalline silicon (HRPS) is due to its comparably high dielectric constant and low dielectric losses a suitable substrate for integration of RF passive devices (e.g. transmission lines, inductors and antennas) and has potential for application in wafer-level packaging (WLP). In this work, we report our further progress in developments of an HRPS-based wafer-level chip-size package for RF applications. HRPS can be obtained from the early phase of float-zone wafer preparation (wafers from high-resistivity polysilicon rods) and is a cost-effective alternative to the high-resistivity single-crystalline silicon wafers and an 'easy-to-process' alternative to the glass wafers.

HRPS is proposed and characterized as a novel substrate in wafer-level packaging suitable for integration of RF passive devices. The WLP solution we introduce is based on adhesive bonding of a passive HRPS wafer to an active silicon IC wafer where the HRPS wafer serves as a mechanical carrier, thermal spreader and vertical spacer. It allows thinning and selective removal of the silicon IC substrate preserving mechanical integrity, at the same time suppressing RF substrate losses and vertical integration of high-quality passive components.

In the following section, the WLP concept based on HRPS substrate is introduced, the results on electrical and material characterization of HRPS are presented, and the fabrication sequence is discussed. In the section on RF applications, theoretical and experimental results obtained for via-connected spiral inductors, patch antennas and shielding structures are described.

Wafer-Level Packaging Using HRPS Substrate

Fig. 1 illustrates the proposed concept, where wafer-level chip-size packaging is used to stack HRPS substrate on top of a RF silicon IC process wafer and to integrate large, high-quality PDs on the package front side and a ground plane on the package back side. The IC wafer is thinned and selectively removed to expose its signal pads from the package back side and to provide shielding between different circuit partitions.

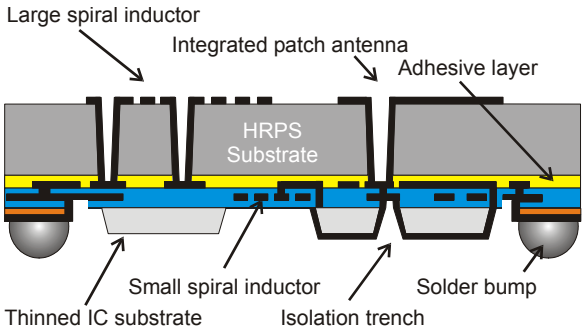


Fig. 1. Schematic view of the proposed wafer-level packaging concept based on a low-loss high-resistivity polycrystalline silicon substrate enabling implementation of RF features such as through-substrate isolation trenches for crosstalk suppression, vertically-spaced large spiral inductors, a back-side ground plane, area-array bumps with low parasitics, etc.

HRPS may also serve as a low-cost substrate for integration of passive networks. HRPS offers several advantages in comparison to glass, such as the higher and nearly frequency independent dielectric constant (11.7 vs. 4.8-6.2) [8] allowing for a 30%-35% more compact component integration, the >10-times higher thermal conductivity, the perfect matching of the thermal expansion coefficient to that of the integrated circuit (IC) wafer, and the full compatibility with silicon processing.

HRPS Substrate Electrical Characterization

HRPS wafers having diameter of 4 inch used in our experiments, were obtained from high-resistivity (~4kOhm-cm) polysilicon rods which are normally used for float-zone single-crystalline Si wafers. By avoiding the expensive float-zone crystallization step, the cost of HRPS wafers is significantly reduced, while the favorable material properties of single crystalline silicon (high thermal conductivity, comparably high dielectric constant, matched thermal expansion coefficient, easy processing) are still present. Moreover, the

polycrystalline structure of HRPS eliminates surface channel effects [6].

The substrate electrical properties were extracted from S-parameter measurements on coplanar waveguides (CPWs) and CPW T-resonators fabricated using a 2 µm Al metallization with and without 1 µm thick PECVD-oxide insulation layer. The CPW test structures were designed with different signal-ground spacings in order to achieve impedances close to 50 Ω in all cases and to allow for meaningful comparisons. CPW length of 0.5 mm, 1 mm, 3 mm, and 5 mm were used.

For comparison, the same CPW structures were also fabricated on a commercially available glass substrate AF-45 and high-resistivity monocrystalline silicon wafers with and without surface passivation [6].

The dielectric constant and the loss tangent were obtained from S-parameter measurements up to 30 GHz. Good agreement of the measured data and simulations in ADS-Momentum were obtained for all CPW structures and substrates shown in Fig. 2.

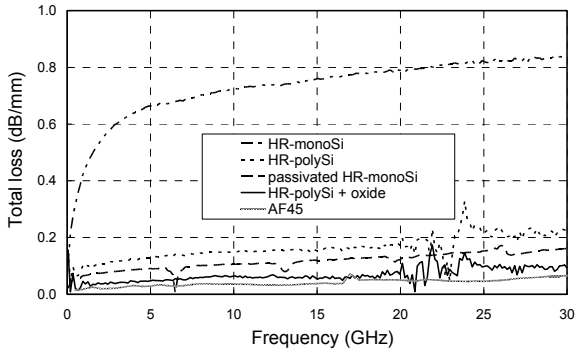


Fig. 2. Frequency dependence of the total loss of coplanar wave guides on high-resistivity polysilicon (HRPS) with and without 1 µm PECVD insulation oxide in comparison to high-resistivity mono-crystalline silicon (HRS) with and without surface passivation and to a Schott AF-45 glass substrate.

In comparison to the glass substrate Schott AF-45 (α=0.38 dB/cm), a comparably low loss figure was measured for HRPS with (α=0.44 dB/cm) and without (α=0.89 dB/cm) an insulation oxide layer at 6 GHz. The fact that a low loss tangent could be demonstrated for HRPS without an insulation oxide layer is significant, because metal vias through the HRPS substrate can therefore be built without any complicated dielectric liner formation (Fig. 1). In comparison to high-resistivity monocrystalline silicon, no additional surface passivation steps are required for HRPS. That is, because the material has an inherently high defect density (Fig. 3), suppressing any surface channel formation similarly to the surface amorphization to passivate the monocrystalline silicon [6]. Moreover, CPW T-resonators having quality factors $Q=f_0/f_{3\text{-dB}}>18$ demonstrated the low loss of HRPS, while eliminating any de-embedding error.

The crystallographic structure was analyzed using TEM. Fig. 3 shows as an example a bright-field TEM micrograph indicating presence and typical size of various crystallographic features.

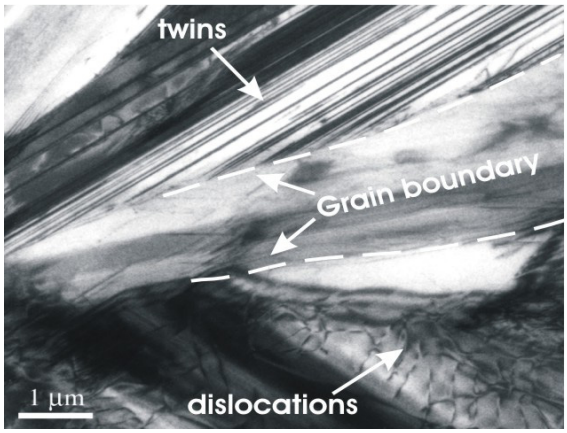


Fig. 3. A bright-field Transmission Electron Microscope (TEM) micrograph illustrating polycrystalline structure of HRPS substrates.

Fabrication sequence

The schematic fabrication sequence is shown in Fig. 4. The proposed WLCSP concept is based on silicon IC substrate transfer to a low-loss HRPS carrier using wafer-level adhesive bonding and 3-D metallization for realization of RF passives.

The bonding is done using <10µm-thick BCB layer as an adhesive [9]. First, the BCB layer is spun on the front side of a completed IC silicon wafer and then the wafer is brought into contact under vacuum conditions with HRPS substrate and bonded at pressure of 2 Bar. Next, BCB polymerization takes place at 300°C for several hours. The intermediate BCB layer poses lower demands on the wafer surface roughness than other bonding techniques, thus eliminating the need of additional planarization steps prior to bonding. The HRPS wafer has thickness of 200-500 µm and serves subsequently as a mechanical carrier. It should be noted that very thin HRPS wafers (<150 µm) are less suitable as due to the presence of an internal stress they might suffer from buckling along their periphery.

At this stage, the IC wafer with active circuitry is thinned below 50 µm and then selectively removed using wet or dry etching on places where

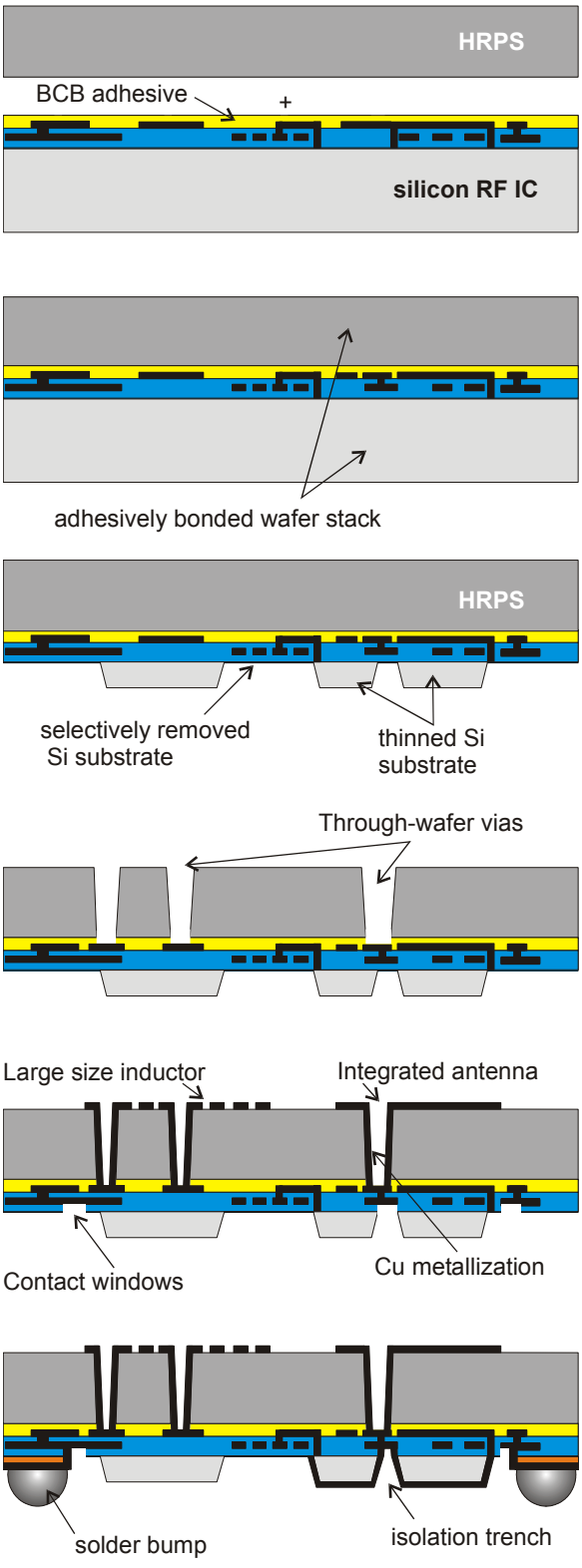


Fig. 4. Schematic HRPS-based WLP fabrication sequence enabling implementation of various RF enhancements. For explanation see text above.

front side signal pads have to be exposed and cross-talk suppression trenches are to be formed. Optionally, silicon is removed underneath the spiral inductors realized at the IC wafer front-side increasing their quality factor. An additional mask step is required to define contact windows in the dielectric layer and to expose the IC metallization from the back side.

Processing then continues on the front side where >50µm diameter vias are etched in the HRPS wafer and BCB layer using DRIE with silicon dioxide as a masking layer. In this step, the contact pads on the IC wafer are exposed from the front side. Since HRPS do not require any insulation layer, metal vias through the HRPS substrate can be built without any complicated dielectric liner formation directly onto the HRPS surface.

For front- and back-side metallization additive copper electroplated process is used. A Ti/TiN diffusion barrier and a Cu seed layer are first sputtered and ~5-10µm Cu is subsequently plated using electroplated photoresist as a mask. The exposed seed layer is then removed and processing is completed by forming of the solder bumps and singulation into individual dies.

Application for RF Silicon ICs

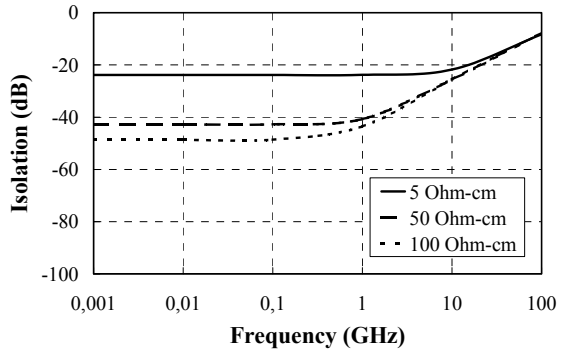
The same processing steps that are used to achieve the WLP technology basic packaging goal, can be adopted for implementation of an additional functionality at no or very limited additional cost. As shown in Fig. 1, the HRPS-based WLP concept presented allows packaging of RF silicon ICs with simultaneous integration of high-quality spiral inductors, antennas or cross-talk suppression structures. In following sections, all these features will be discussed in detail.

Substrate cross-talk suppression using trenching

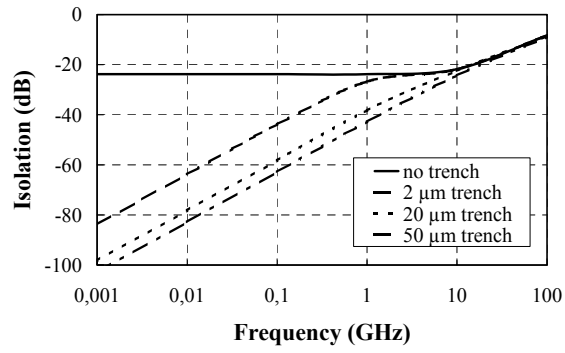
Substrate coupling draws a major concern in mixed-signal integrated circuit design. Noise generated by the noisy digital circuit can couple through the substrate into the analog/RF part (e.g. Low Noise Amplifier) and deteriorate its signal integrity. Furthermore, as the feature size decreases and clock frequency increases, the amount of substrate noise generated from digital switching activities increases dramatically, thus, making the substrate coupling become even more problematic. To overcome this problem, not merely new possibilities from the design perspective, but also the aspects of processing technology have to be considered.

The WLP concept employed in this work is based on the idea where silicon substrate is bonded to a supporting HRPS wafer, hence, mechanical

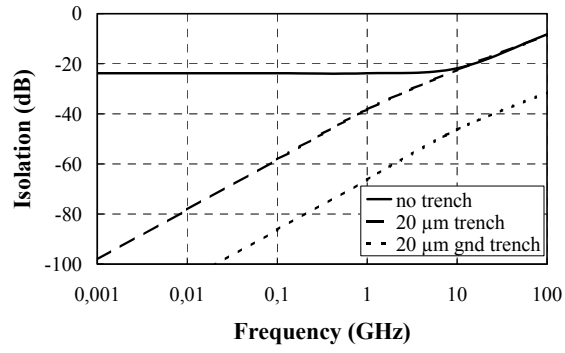
reliability is no longer an obstacle to implement isolation techniques which require substrate structuring such as thinning and trenching.



(a)



(b)



(c)

Fig. 5. Simulated isolation between two substrate contacts vs. frequency for: (a) different substrate resistivities; (b) different trench widths; and (c) an isolation trench with and without grounded backside metallization. If not mentioned otherwise a 50 µm-thick, 5Ω-cm substrate is considered.

Theoretical analysis of substrate coupling was performed by means of 2D device simulator (MEDICI) for a simplified structure consisting of a thinned silicon substrate bonded to a dielectric carrier. Optionally the silicon substrate is trenched and has back-side ground plane metallization. Fig. 5 shows the simulation results indicating influence of various factors (substrate resistivity, isolation trench width, presence of a back-side ground plane) on isolation between two single-ended substrate contacts as a function of frequency.

For experimental verification, test structures with and without through-substrate trenches were fabricated. The measurement results for samples without back-side ground plane are shown in Fig. 6.

The results achieved indicate that substrate trenching is a very effective method for cross-talk suppression at low and medium frequencies. At higher frequencies (>1GHz), trenches have to be lined by ground plane metallization to maintain their effectivness.

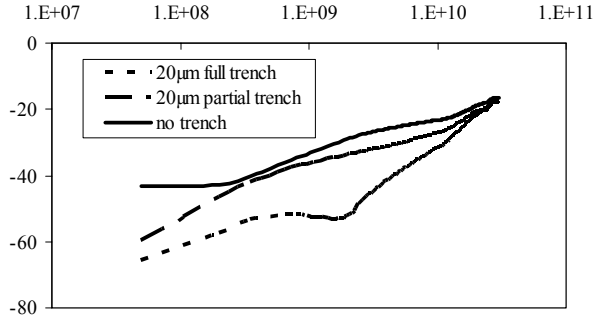


Fig. 6. Measured isolation vs. frequency between two substrate contacts showing influence of a partial and a full trench (contact separation is 100 µm).

Vertically spaced spiral inductors

RF passive components such as spiral inductors usually occupy a large fraction of the costly chip area. A solution to this problem can come from an integration of the passive components over or under the active circuitry [10]. This can be accomplished by using a spacer substrate, having low RF loss, a high permittivity, and good thermal conductivity as accomplished in the WLP concept proposed in this study.

Fig. 7 shows how quality factor of a particular spiral inductor depends on its separation from a metal ground plane and the resistivity of the carrier substrate.

To demonstrate this concept, large spiral inductors (up to 34 nH) were realized on a high-resistivity polysilicon with and without 1µm thick PECVD oxide isolation layer (Fig. 8). A quality factor Q>10 at 1 GHz was measured for a very large 34-nH coil (A=820x820 μm^2) as shown in Fig. 9. It was particularly remarkable that the inductors were also functional without any dielectric isolation layer (Q=7.5 for a 34 nH coil).

Very small spiral inductor occupying only a small die are does not need to be vertically spaced. A better option is to integrate them directly on the RF IC wafer and during the packaging process selectively remove the silicon substrate underneath to increase their quality factor (see Fig. 1).

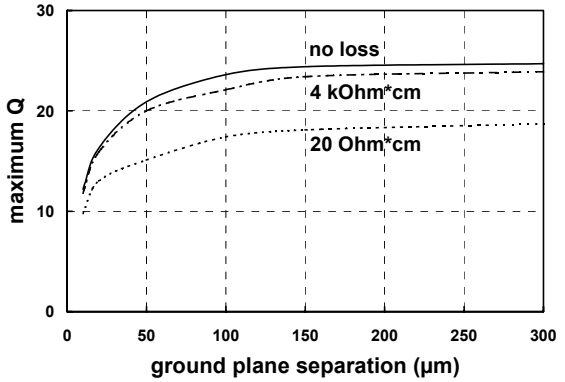
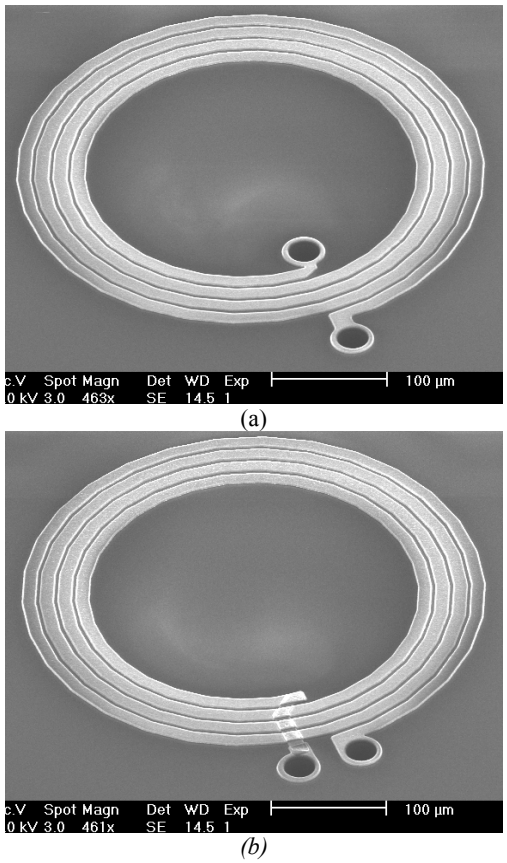


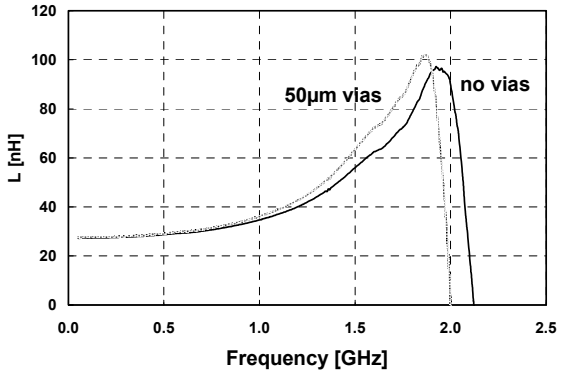
Fig. 7. Quality factor of a 17-nH spiral inductor (in 4-µm Al metallisation) vs. the separation of a metal ground plane for three different substrate resistivities.



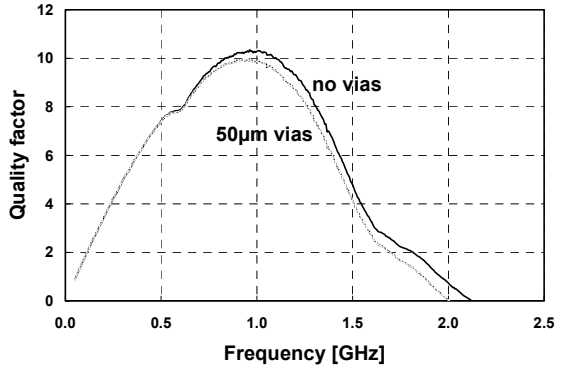
(a)

(b)

Fig. 8. SEM photographs of spiral inductors on high-resistivity polycrystalline silicon (HRPS) with via connections through the HPRS substrate without (a) and with (b) underpass.



(a)



(b)

Fig. 9. Inductance and quality factor (Q) of a 34 nH inductor on a HRPS substrate with and without through-substrate vias.

Integrated antennas

The possibility to integrate an on-chip antenna operating at a certain frequency range is highly dependent on the required device dimensions and efficiency. Reduction of dimensions and efficiency improvement can be obtained through proper device geometry. Substrates with higher dielectric constant are favorable as they enable significant size reduction of integrated antennas [11].

To demonstrate the suitability of HRPS substrate for on-chip antenna integration a simple patch antenna was built on top of an HRPS wafer. No insulating layer between the metal patch and the substrate was applied. The design was made with HFSS FEM tool. The antenna was designed to operate in the 5-6 GHz ISM band, which yields antenna dimensions of 7.7x7.6 mm^2. The patch metal

layer was made with 2 µm of sputtered aluminum and the feeding was realized through a microstrip line.

For a measurement purpose, the antenna die was placed on top of a PCB substrate and the feeding microstrip line was connected to a SMA connector. The fabricated antenna prototype is shown in Fig. 10.

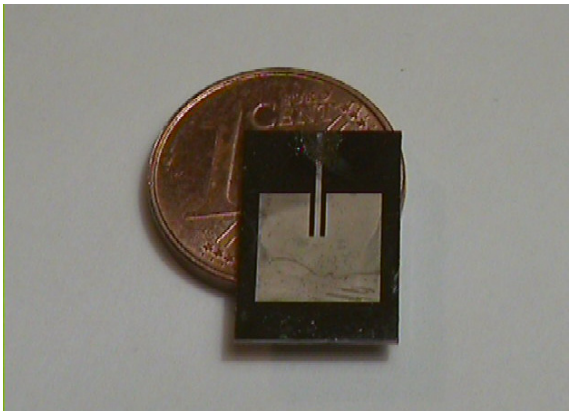


Fig. 10. Patch antenna prototype fabricated on a HRPS substrate.

All the measurements were performed using the HP 8510 vector network analyzer, which was previously calibrated with one-port calibration. The antenna efficiency was measured using the Wheeler cap method [12]. This method is based on the measurements of the antenna input return loss when it is radiating or not radiating. The last condition is usually met with a metallic cap enclosing the antenna under test. With those measurements the efficiency can be easily computed. The antenna efficiency was also obtained from simulations and compared with the measured values.

The measured values obtained in the Wheeler cap method are plotted in Fig. 11. Antenna efficiency of 18.6 % has been extracted, which is in good agreement with the value computed by HFSS (19.6 %). The measured antenna operating frequency of 6.25 GHz, with a –10 dB return loss bandwidth of ~200 MHz also fit the simulations.

Conclusions

In conclusion, HRPS is presented and demonstrated as a low-cost material for wafer-level packaging of silicon RF ICs. HRPS provides a low RF loss, a high dielectric constant, a high thermal conductivity, good mechanical properties, and a perfect match to the integrated circuit silicon substrate in thermal expansion coefficient. Last but not least, the fabrication technology know-how available for standard single-crystalline Si substrates is directly applicable to processing of HRPS. The HRPS-based WLP concept proposed in this study enables implementation of 3-D passive structures potentially enhancing package performance. This was demonstrated on vertically spaced spiral inductors, cross-talk suppression structures and integrated patch antennas.

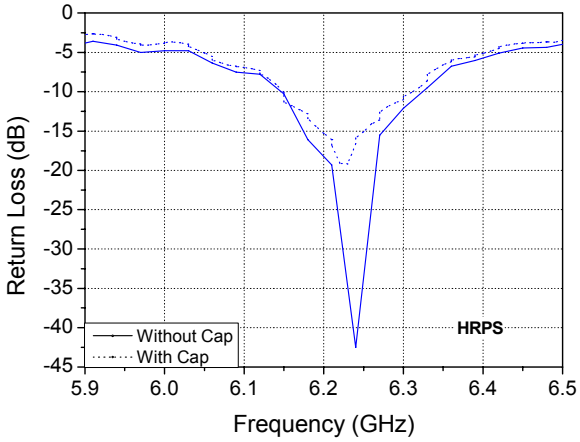


Fig. 11. Measured return loss versus frequency used to obtain the operating frequency, bandwidth and efficiency.

Acknowledgments

The authors wish to acknowledge the support by Philips Semiconductors and Philips Research in the context of the Philips Associate Centre at DIMES (PACD); the Portuguese Foundation for Science and Technology (SFRH/BD/4717/ 2001, POCTI / ESE / 38468 / 2001, FEDER), and the European Commission (project Blue Whale IST-2000-3006). Dr. Manfred Grundner and Wacker Siltronic are acknowledged for supplying polysilicon rod material. Bernd Lux from the Institute of Crystal Growth (IKZ), Berlin, Germany is acknowledged for arranging the wafer dicing and polishing.

References

[1] H. Reichl, V. Grosser, "Overview and Development Trends in the Field of MEMS Packaging", Proc. MEMS 2001, Interlaken, Switzerland, January 21 – 25. pp. 1-5, 2001.

[2] S.K. Pienimaa, N.I. Martin, "High density packaging for mobile terminals", Proc. 51st ECTC, Orlando, Florida, May 29 - June 1, pp. 1127 - 1134, 2001.

[3] L. Larson, D. Jessie, "Advances in RF packaging technologies for next-generation wireless communications applications", Proc. IEEE 2003 Custom Integrated Circuits Conference, San Jose, USA, September 21-24, pp. 323-330, 2003.

[4] J.N. Burghartz, B. Rejaei; "On the Design of RF Spiral Inductors on Silicon", IEEE Transactions

on Electron Devices, Vol. 50, No. 3, pp. 718-729, 2003.

[5] A. Badihi, "Ultrathin Wafer Level Chip Size Package," IEEE Trans. on Advanced Packaging, Vol. 23, No. 2, pp. 212-214, May 2000.

[6] B. Rong, J.N. Burghartz, L.K. Nanver, B. Rejaei, M. van der Zwan, "Surface-Passivated High-Resistivity Silicon Substrates for RF-IC's", IEEE Electron Device Letters, Vol. 25, No. 4, pp. 176-178, April 2004.

[7] P.M. Mendes et al., "Wafer-Level Integration of On-Chip Antennas and RF Passives Using High-Resistivity Polysilicon Substrate Technology", Proc. of 55th ECTC, Las Vegas, USA, June 1-4, pp. 1879 – 1884, 2004.

[8] A. Polyakov, P.M. Mendes, S.M. Sinaga, M. Bartek, B. Rejaei, J.H. Correia, J.N. Burghartz; Processability and Electrical Characteristics of Glass Substrates for RF Wafer-Level Chip-Scale Packages", Proc. 53rd Electronic Components and Technology Conference, New Orleans, USA, May 27-30, pp. 875-880, 2003.

[9] Hewlett Packard, "Basics of measuring the dielectric properties of materials", Application Note 1217-1.

[10] J. Hinojosa, "S-Parameter Broadband Measurements On-Coplanar and Fast Extraction of the Substrate Intrinsic Properties," IEEE Microwave and Wireless Comp. Letters, Vol. 11, No. 2, pp. 80-82, 2001.

[11] J. Hinojosa, K. Lmimouni, G. Dambrine, "Fast Electromagnetic Characterization Method of Thin Planar Materials Using Coplanar Line up to V-band", Electron. Lett., Vol. 38, No. 8, pp. 373-374, 2002.

[12] A. Polyakov, M. Bartek and J.N. Burghartz, "Area-Selective Adhesive Bonding Using Photosensitive BCB for WLCSP Applications", ASME Journal of Electronic Packaging, accepted for publication.

[13] N.P. Pham, P.M. Sarro, K.T. Ng, J.N. Burghartz, "IC-compatible two-level bulk micromachining process module for RF silicon technology", IEEE Trans. on Electron Devices, Vol. 48, No. 8, pp. 1756 -1764, August 2001.

[14] P.M. Mendes, A. Polyakov, M. Bartek, J. N. Burghartz, J.H. Correia, "Integrated 5.7 GHz Chip-Size Antenna for Wireless Sensor Networks", Transducers'03, Boston, USA, June 8-12, pp. 49-52, 2003.

[15] Edward H. Newman, Peter Bohley, C. H. Walter, "Two Methods for the Measurement of Antenna Efficiency", IEEE Trans. Ant. Prop., Vol. 23, No. 4, pp. 457-461, 1975.