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Filipe Manuel Serra Alves

Auto-calibrated, thermal-compensated MEMS for smart Inclinometers

Universidade do Minho
Escola de Engenharia

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Trabalho efetuado sob a orientação do
Professor Doutor Luis Alexandre Machado da Rocha
Professor Doutor Jorge Miguel Nunes dos Santos Cabral

Março de 2017

STATEMENT OF INTEGRITY

I hereby declare having conducted my thesis with integrity. I confirm that I have not used plagiarism or any form of falsification of results in the process of the thesis elaboration.

I further declare that I have fully acknowledged the Code of Ethical Conduct of the University of Minho.

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Full name: Filipe Manuel Serra Alves

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Filipe Alves

Guimarães, March 24th, 2017.

To my beloved Sister!

Para a minha querida Irmã!

Abstract

The electronic control of a mechanical structure with micro dimensions, offers unique opportunities to exploit the tight coupling between co-integrated micromechanical structures and ICs (=Micro Electro Mechanical Systems (MEMS)). This coupling allows the implementation of integrated data-acquisition systems, with overall functionality or specifications that cannot be met using individually designed structures and circuits.

This work focus on the development of a new class of MEMS-based inclinometers that includes electromechanical pre-processing of the mechanical signal in the mechanical domain and thermal compensation. The force-dependent pull-in voltage of a micromechanical structure, due to a sufficiently large electrostatic field, enables the realization of a high-resolution, low-bandwidth inclinometer. Pull-in is characterized by the sudden loss of stability in electrostatically actuated parallel-plate devices. Since pull-in voltage is stable and easy to measure, it enables an effective transduction mechanism that does not require complex readout electronics.

A switched capacitor based complementary metal-oxide-semiconductor (CMOS) integrated circuit is developed, fabricated and used to detect the large capacitance change in the MEMS sensing element, while controlling a high-resolution external actuation system.

Dedicated MEMS microstructures with extra proof mass show high sensitivity, $269mV/^{\circ}$ with a non-linearity better than $0.5\%FS$ (Full Scale of $\pm 23^{\circ}$). The measured noise is limited by the actuation system, rather than the mechanical-thermal white noise of the MEMS device, setting the sensor's resolution at $75\mu^{\circ}$, high above state-of-the-art MEMS devices. The characteristics of this dedicated MEMS inclinometer system enables an thermal compensation mechanism, which increases the sensor stability to values better than $0.004\%FS$.

Resumo

O controlo eletrónico de estruturas mecânicas de micro dimensões, oferece oportunidades únicas para a exploração do acoplamento integrado entre microestruturas mecânicas e circuitos integrados (=*Micro Electro Mechanical Systems* MEMS). Este tipo de acoplamento permite a implementação de sistemas de aquisição de dados integrados, com funcionalidades ou especificações que não poderiam ser atingidas por estruturas ou circuitos desenhados individualmente.

Este trabalho foca-se no desenvolvimento de um novo tipo de inclinómetros MEMS que inclui mecanismos de compensação térmica diretamente no domínio mecânico. A tensão de *pull-in* de uma microestrutura mecânica, possibilita a criação de inclinómetros de elevada resolução e baixa largura de banda. O fenómeno de *pull-in* é caracterizado pela súbita perda de estabilidade em estruturas de elétrodos-paralelos, quando electrostaticamente atuadas. Uma vez que a tensão de *pull-in* é estável e fácil de medir, é possível criar um método de transdução eficiente, sem ser necessário um *front-end* capacitivo de elevada complexidade.

Um circuito integrado, baseado num amplificador de condensadores comutados, é desenvolvido, fabricado e usado para detetar a variação de capacidade no elemento sensorial, ao mesmo tempo que controla o sistema de atuação externo de elevada resolução.

As microestruturas fabricadas com uma massa-inercial adicional, demonstraram elevada sensibilidade, $269mV/^{\circ}$ (não linearidade $< 0.5\%$, escala completa de $\pm 23^{\circ}$). O ruído medido não foi limitado pelo ruído termomecânico da estrutura, mas sim pelo sistema de atuação, colocando a resolução do sensor em $75\mu^{\circ}$, claramente acima do estado da arte em dispositivos MEMS. As características únicas deste inclinómetro, permitem a implementação de mecanismos de compensação térmica, podendo melhorar a estabilidade do sensor para valores superiores a $0.004\%FS$.

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Acronyms

AC - Alternating Current

ADC - Analog to Digital Converter

AM - Amplitude Modulation

ASIC - Application Specific Integrated Circuit

BS - Backside

CDC - Capacitance to Digital Converter

CM - Common Mode

CVC - Capacitance to Voltage Converter

CFC - Capacitance to Frequency Converter

CMFB - Common-mode Feedback

CMOS - Complementary Metal-Oxide-Semiconductor

COTS - Commercial Off-The-Shelf

CTE - Temperature Coefficient

CVD - Chemical Vapor Deposition

DAC - Digital to Analog Converter

DC - Direct Current

DM - Differential Mode

DOF - Degree-of-Freedom

DRIE - Deep Reactive Ion Etching

FFT - Fast Fourier Transform

FPGA - Field Programmable Gate Array

FS - Full Scale

FSM - Finite State Machine

GBW - Gain Bandwidth Product

HDL - Hardware Description Language

HF - Hydrofluoric Acid

IC - Integrated Circuit

I^2C - Inter-Integrated Circuit

INL - Iberian International Nanotechnology Laboratory

LSB - Least Significant Bit

MCU - Microcontroller Unit

MEMS - Microelectromechanical Systems

PCB - Printed Circuit Board

PECVD - Plasma-enhanced Chemical Vapor Deposition

PTAT - Proportional to Absolute Temperature

RF - Radio Frequency

RH - Relative Humidity

RIE - Reactive Ion Etching

RGT - Resonant Gate Transistor

RMS - Root Mean Square

SEM - Scanning Electron Microscope

S/H - Sample and Hold

SOI - Silicon-on-Insulator

SR - Slew Rate

SPI - Serial Peripheral Interface

SNR - Signal to Noise Ratio

TIA - Transimpedance Amplifier

T$_{pi}$**-**Pull-In Time

TC - Thermal Coefficient

TDC - Time to Digital Converter

V$_{pi}$**-**Pull-In Voltage

1
Introduction

In the past century, picturing the possibility of making *"small but movable machines"* was just the dream of some extraordinary people [1.1]. Over the years, the technology developments, pushed by human curiosity, turned that thought into a reality. This field of engineering, also known as **microengineering**, is where several physical domains meet each other at a micro-scale.

The origin of the technology that we now know as MicroElectroMechanical Systems (MEMS) can be traced back to the beginning of the 50's, when Smith, then at Bell Telephone Laboratories, published in *Physical Review* the first stress-sensitive effects in silicon and germanium, called piezoresistance [1.2]. Together with this discover, the invention of the transistor, in 1947 at the same laboratory [1.3], and latter the creation of the first integrated circuits (IC), at Texas Instruments [1.4] and at Farchild Semiconductor [1.5], both in 1958, triggered the investigation whether these revolutionary electronic fabrication techniques could be applied to sensors.

This new world of possibilities drove a new research field on micromachined silicon devices, studying the compatibility with IC technology, along with the properties of silicon as a mechanical material [1.6]. The evolution of IC technology also meant

that new batch fabrication techniques were available for the micromechanical components. During the early 60's, the first papers on silicon diaphragm pressure sensors and strain gauges were published by Bell Labs and Honeywell Research Centre [1.7, 1.8]. The interest in this silicon sensor technology started to increase and, by the late 60's, the first pressure sensors started to be commercialized by new American companies.

At the beginning of the 70's, huge developments in the manufacturing processes initiated a new era of superior performance sensors, **the first true MEMS sensors**. At this point, the automotive, medical and aerospace industries started to benefit from the smaller size, lower cost and higher reliability offered by silicon-based micro-devices when compared with the old macro-systems. This demand allowed the micro-sensors production volumes to increase, reaching the mass fabrication of silicon-based pressure sensors and accelerometers by the end of the 80's [1.9].

1.1 MEMS

What is exactly the meaning of MEMS? Is it purely the acronym for microelectromechanical systems, i.e. systems with 1μm to 1mm of length that combines both mechanical and electrical components? The answer is no. Not all the MEMS devices are "electromechanical" and few are "systems". In fact the term MEMS was not introduced until 1987 [1.10].

The term is now used to refer all kinds of miniaturised devices, generally 3D microstructures and mostly fabricated from silicon (bulk micromachining, surface micromachining or both), mainly using techniques employed in IC manufacture. Today, devices from silicon microsensors to "lab-on-a-chip" are all referred to as MEMS [1.11].

The need for the readout information of the mechanical devices and its further processing, as well as the demand for calibration and compensation schemes triggered the development of dedicated integrated interface circuits. The development of fully-integrated systems (mechanical element and dedicated electronics), was the breaking point for spreading the MEMS technology into new application areas. The impact of the electronic interface on the overall MEMS device performance is so large that, it has maintained the interest of related research for more than two

decades now.

This field of microengineering has witnessed an explosive growth, supported by new emerging applications, such as accelerometers, strain gauges, microphones, air mass flow sensors, pressure sensors and more recently gyroscopes, inkjet printer heads, digital microdisplays and yaw-rate sensors [1.12]. In particular, the inertial sensors market, namely accelerometers and gyroscopes, during the last decade, represented approximately one quarter of the whole MEMS market, largely dominated by the automotive industry. In the past few years, the consumer electronics market started paying a more important role in the inertial sensors market, overtaking the automotive as the most relevant industry [1.13].

1.1.1 Inertial Sensors

The fundamental concept of an inertial sensor can be understood with reference to the mechanical system represented in figure 1.1. A proof mass, m, is suspended by a mechanical spring, k, that is acted by an input force, F, representative of a quantity to be measured. This input force causes the displacement of the mass, x, that is proportional to the applied force.

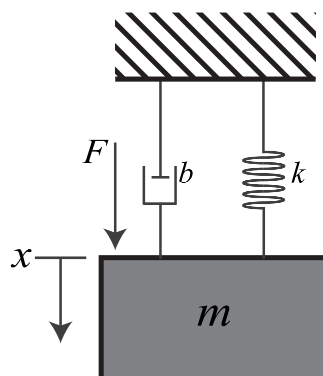


Figure 1.1: Simplified diagram of a MEMS inertial sensor.

The input force can result from the acceleration of the mass, in the case of an accelerometer [1.14–1.16] or inclinometer [1.17]. In the case of a vibratory gyroscope [1.18], this force is related to the Coriolis acceleration [1.19] (result of the angular rotation of the mass).

Different transduction mechanisms are used to transform the acceleration acting on the mass, into the device information of interest [1.20]. Usually, these sensors

are designed in a way that the parasitic forces on the mass are rejected, while achieving high transduction gains. Such unwanted forces might result from stress, packaging problems, thermal expansion or cross-axis sensitivity, leading to more complex spring and mass designs.

During the movement of the proof mass, a damping force proportional to the mass velocity is generated. The damping coefficient, b (figure 1.1), in inertial MEMS is typically dominated by air damping. The damping effect can be controlled by a proper packaging, allowing the device accurate operation under low pressure. Additional forces, such as electrostatic force might act on the device, depending on the operation mode.

1.1.2 MEMS Fabrication

Even though MEMS fabrication is based on the IC microfabrication batch processes, mastering the MEMS fabrication technology is not an easy task. The MEMS specific challenges include the packaging of mechanical structures, or the manufacture of thick mechanical layers. To face these challenges, numerous MEMS fabrication processes have been developed over the years. Traditionally, these processes have been divided into surface micromachining and bulk micromachining [1.12].

Surface micromachining is based on patterning thin films on top of the substract wafer [1.21]. In the typical fabrication process, depicted in figure 1.2, successive steps of thin film deposition, followed by selective etching are performed to achieve 3-D structures. The structures complexity can vary from two structural layers and one sacrificial layer, in the most simple examples, to five structural layers in the most complex moving devices [1.22]. The compatibility with IC processing is one of the main advantages of surface micromachining, allowing an easy integration of mechanical and electrical components in the same chip.

On the other side, bulk micromachining defines structures by selectively etching the substrate [1.23], allowing this way, the fabrication of thick structures. This possibility is specially important in the inertial sensors field that benefits from a large proof mass. Additionally, the opportunity of using single-crystal silicon to fabricate the device, due to its predictable and stable properties, reinforces the idea that bulk micromachining is suitable for mechanical devices. The bulk manufacturing was strongly simplified with the combination of deep reactive ion etching

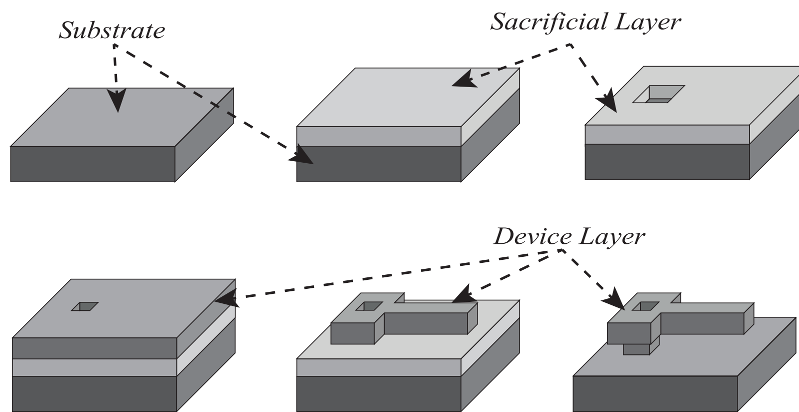


Figure 1.2: Typical surface micromachining process, involving layers depositions, optical lithography and etching.

(DRIE) and silicon on insulator (SOI) technology, which additionally enables the reduction of the devices' size [1.24, 1.25]. An example of a possible process, using SOI wafers and DRIE etching is shown in figure 1.3. This kind of processes are quite simple and result in structures with well defined features.

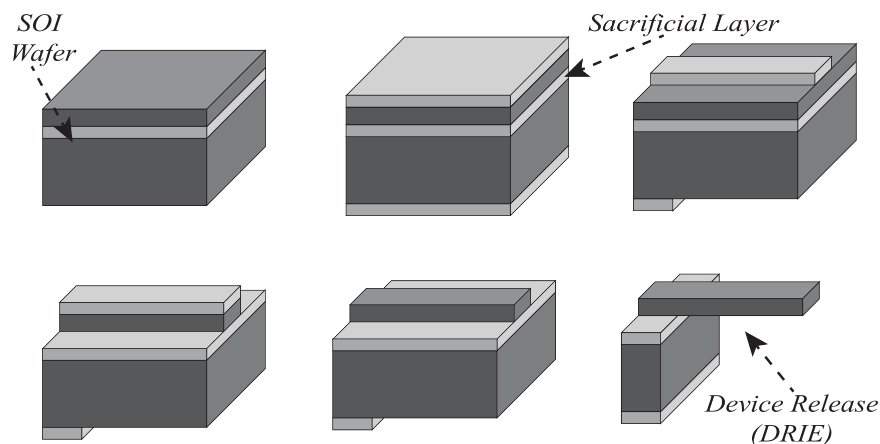


Figure 1.3: Typical bulk micromachining process in a SOI wafer.

1.1.3 Packaging and Integration

The act of bringing together the mechanical and electrical parts can be referred to as *integration*, while the *packaging* indicates the achievement of placing the diced chips into handleable modules that can be assembled into circuit boards.

Packaging a device implies dicing and assembling the die, as well as encapsulating and testing [1.26]. This task is specially important in MEMS devices [1.27, 1.28],

where the performance and reliability can be deeply affected. It often accounts for $30 - 90\%$ of the total cost.

According to the definition of MEMS, the circuits and the mechanical elements should be fabricated in the same silicon die, but in reality, there are many different integration options.

Board-level Integration

Integrating the system at the board level involves using different packages for the micromechanical and for the circuit part, connecting them at the circuit board level (figure 1.4). This scheme implies long wiring distances, large electronic noise and low potential for miniaturization.

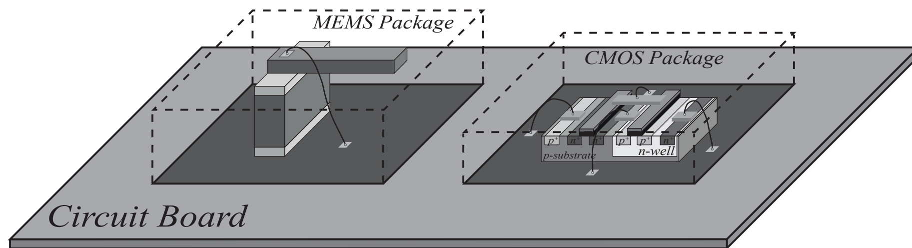


Figure 1.4: Circuit board level integration.

Chip-level Integration

This packaging scheme is represented in figure 1.5, where separate micromechanical and circuit dies are used. The dies are placed in the same package and connected between each other using bonding wires. The fact that multiple dies are used reduces processing issues, commonly registered in wafer-level integration approaches. On the other hand, the distance between the mechanical element and the circuit is not minimized.

Wafer-level Integration

The integration scheme that minimizes the distance between the circuits and the mechanical elements, reducing electromagnetic noise, is the wafer-level integration. This method also allows maximizing the miniaturization, producing small dimension packages.

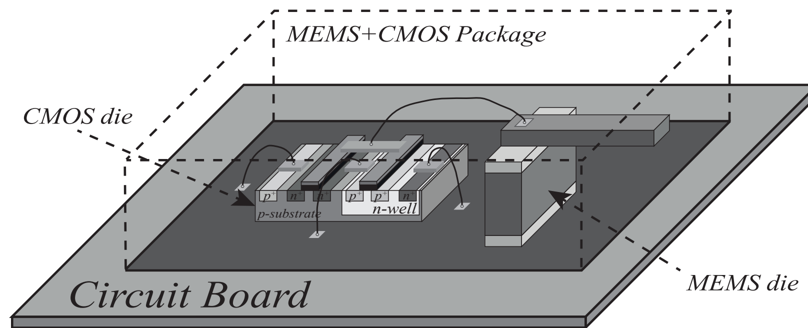


Figure 1.5: Chip level integration.

Wafer-level integration can be divided in two groups. The ones that both components (micromechanical components and integrated circuit) are fabricated in the same wafer (monolithic) and the ones integrated through die attachment (wafer-bonding figure 1.6).

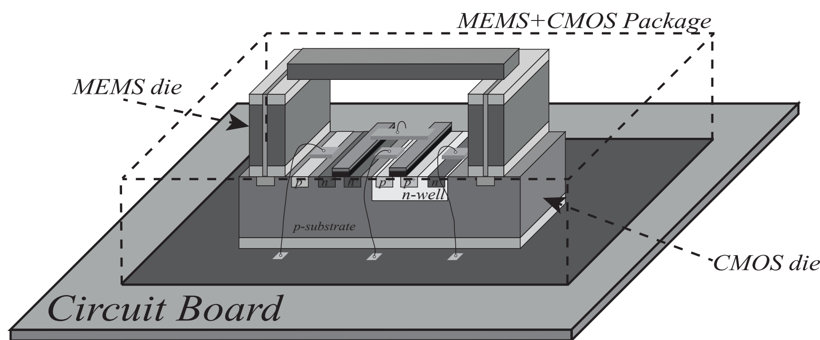


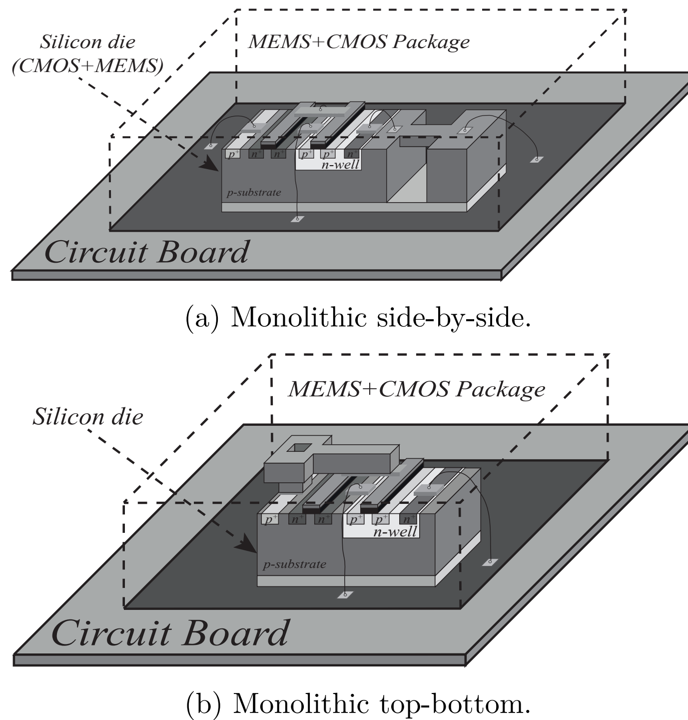
Figure 1.6: Wafer level integration - Wafer bonding.

In the monolithic integration, distinct variations can be found, where the electromechanical element and the circuitry are placed side-by-side (figure 1.7a), or place on top of each other (figure 1.7b).

These monolithic integration types can be achieved either by using:

- Post-processing fabrication technique, where the electromechanical element is processed on top of the semiconductor wafer with preexisting circuits.
- Pre-processing fabrication technique, where the electromechanical element is fabricated on a wafer first, followed by the circuit fabrication.
- Side-by-side-processing fabrication technique, where the electromechanical element and the electronic circuits are created simultaneously.

The integration approaches presented in this section are the main ones, but many



(a) Monolithic side-by-side.

(b) Monolithic top-bottom.

Figure 1.7: Wafer level integration. Monolithic integration

variations can be found in literature [1.29].

1.2 Inclinometers

An inclination or tilt sensor is a device that measures the tilt angle of an object, based on the measured component of the gravitational force. This kind of sensors is used in many areas of application, such as avionics, automotive, automation, civil engineering, robotics and consumer fields [1.30–1.34].

Typically, inclinometers are based on an existing high sensitivity accelerometer that is incorporated into a system as the sensing element [1.35, 1.36]. As a result, the characteristics of the selected accelerometer will define the inclinometer characteristics. Since size, cost and power are usually important application characteristics [1.37, 1.38], MEMS accelerometers [1.20] are commonly used rather than traditional accelerometers (though high performance, they are very expensive, power hungry and cumbersome).

Inclinometers are devices that do not require large bandwidths but they must have a good stability over time and good resolution. This is particularly important

for structural health monitoring, where autonomy, long term stability and auto-calibration capabilities are highly desirable [1.37, 1.38]. These characteristics call for dedicated solutions that can provide inclinometers with auto-calibration and autonomy.

1.2.1 Non-MEMS Approaches

In the most recent years, some new inclinometer approaches have been proposed using non-MEMS technology [1.39–1.42], with resolutions of a few milidegrees. Nevertheless, current state-of-the-art inclinometers, are dominated by other technologies, rather than MEMS. A range of servo inclinometers are available on the market, using detection mechanisms that have "virtually" infinite resolution. Usually, these inclinometers operate as a closed loop torque balance servo system (figure 1.8).

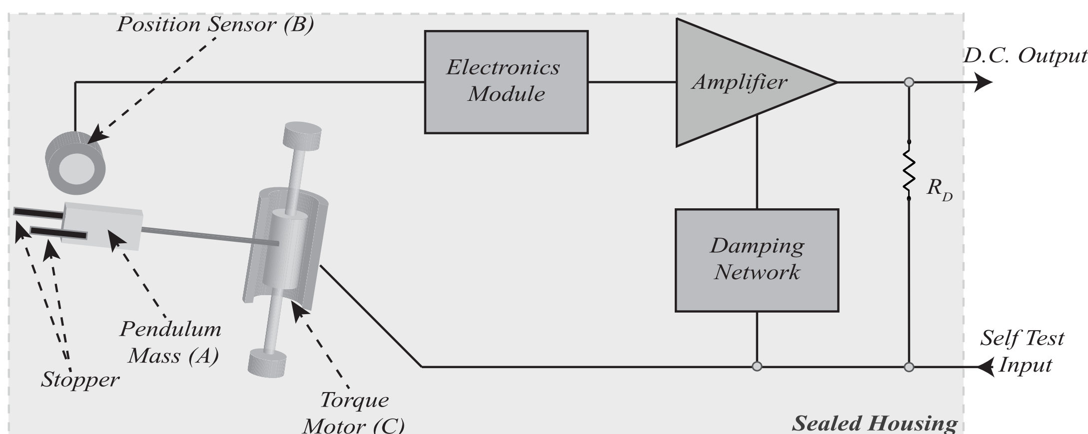


Figure 1.8: Closed loop torque balance servo system (Sherborne Sensors).

As the inclinometer is tilted, along its sensitive axis, the pendulum mass, A, moves in the direction of the tilt, as a result of the force from the gravitation acceleration component. This location change is detected by the position sensor, B, and the resultant error signal is fed to the amplifier that acts on the torque motor, C, through R_D. The current applied to the motor armature produces a force that opposes the gravitational force, moving the mass (A) towards its original position. The feedback current that flows through R_D generates a voltage across the resistor, which is proportional to the sine of the tilt angle.

This kind of devices, commonly used in structural health monitoring, can have resolutions as low as 28 $\mu°$ [1.43] but are expensive and therefore cannot be widely

applied. They have also been used to detect natural disasters such as earthquakes [1.44] or soil slope movements, adding the need for great autonomy [1.45]. Given these requirements, there are opportunities for the development of dedicated MEMS solutions for low-power, low-cost, high-performance inclinometers, both commercially and at the scientific level.

1.2.2 MEMS Approaches

In the past few years, several MEMS based accelerometers were used as inclinometers [1.46]. The precision and resolution of those devices depend on the technology and transduction mechanism used. The most common transduction mechanisms are capacitive [1.47, 1.48], piezoresistive [1.49], resonant [1.50], thermal [1.51] and, more recently, optical [1.52].

Piezoresistive accelerometers are usually characterized by a simple fabrication process and elementary sensor structures. Typically, this kind of accelerometers have simple measuring techniques (piezoresistors bridges are widely used) showing good linearity but low sensitivity [1.53]. Piezoresistive sensors, in general, offer the advantage of being suitable for applications where the sensor must operate remotely from the electronics. However, they are intrinsically sensitive to temperature, increasing the need for implementation of temperature compensation mechanisms [1.54].

Numerous thermal convection-based accelerometers have been presented over the last two decades [1.32, 1.55–1.57]. The key feature of this kind of devices is that no solid proof mass is required to measure acceleration since it relies on the free convection of an air bubble in a closed chamber. Thermal devices are compact, easy to fabricate and sensitive to small accelerations. Nevertheless, the heat transfer and fluid flow is quite slow, limiting the frequency response of the accelerometer and constraining the device applications [1.51].

The oscillation frequency at resonance of a mechanical structure changes while under the effect of an external force (i.e. external acceleration) [1.58–1.60]. This principle can be used in several sensors, and parameters other than frequency, such as oscillation amplitude, can be used as the transduction mechanism. Normally, frequency-output resonant sensors achieve high sensitivity and good resolution allied with good stability. Resonant sensors can be developed based on several different operating methods with input and output signals of electrical nature,

allowing the detection and tracking of the resonant frequency using closed-loop read-out circuits [1.50].

Regarding the pros and cons of the listed transduction mechanisms, the capacitive devices arise as a good alternative. Micromachined capacitive accelerometers can achieve high sensitivity and good resolution but typically yield low signal levels, which requires high sensitivity interface circuitry carefully designed to reduce parasitic capacitances [1.48, 1.61].

The MEMS-based solutions proposed in literature, are still far from reaching the resolution levels required for the main applications of tilt sensors. Piezoresistive based approaches can reach resolutions around 0.1° [1.53], while thermal type devices reported resolutions of $3m°$ [1.32]. In [1.61], a capacitive inclinometer was proposed, aiming to have small size, high sensitive and good resolution, but a resolution of 0.25° was retrieved in a high operating range (±90°). Recently, a 2-axis inclinometer based on three quartz vibrating MEMS beam was proposed, announcing a resolution of $0.3m°$ [1.46].

1.2.3 Commercial Devices

Despite the youth of electronic inclinometers, there is an expressive amount of devices on the market with very good characteristics. Those devices were designed to be used in many different areas of applications, such as aviation and marine [1.43, 1.62], platforms leveling [1.63], large machinery installation [1.62], structural monitoring or laser leveling [1.43, 1.62–1.67]. There are also some devices to be used in robotics field [1.63, 1.64] and in power electronics, to control the tilt of solar panels [1.64]. The continuous human interest in exploring the space or just the need for transmitting data over long distances, requires precise control of the antennas alignment [1.63, 1.64].

Some MEMS approaches have been developed at a commercial level in the past few years, starting to come close to the conventional inclinometers characteristics. A synopsis of some of the best commercial devices specifications is presented in table 1.1, and can work as a guide towards the proposed sensor desired specifications.

Table 1.1: State-of-art devices Specifications

	MEMS Inclinometers			Not MEMS technology/Conventional inclinometers	
Specification	MEMSIC AXTLA01/02 [1.68]	RST Digital Tilt Logger [1.65]	Murata SCA103T D05 [1.66]	Jewell LSOC/LSOP [1.67]	Sherbone Sensors LSOC/LSOP [1.43]
Resolution ($\mu°$)	30000	600	1300	280	28
Sensitivity (mV/°)	100±10	NA	140	3183	5000
Operation Range (°)	±20	±15	±30	±1	±1
Bandwidth (Hz)	6	0.1	28	0.5	10
Non-Linearity (%FS)	<0.4	0.0125	0.11	0.03	0.05
Thermal Drift (%/°C)	0.01	NA	0.013	0.04	0.05
Stability/Repeatability (%FS)	NA	±0.0125	0.028	NA	0.04
Output Signal	Analog Voltage	Digital	Digital	Analog Voltage	Analog Voltage
Technology	MEMS	MEMS	MEMS	Closed-Loop (Servo)	Closed-Loop (Servo)

NA - Not Available

1.3 Motivation and Goals

The possibility of developing a smart inclinometer that goes beyond the current stat-of-the-art, including all the challenges that arises when working in a multidisciplinary field is the main motivation for this work.

Besides that, the proposed approach for the realization of the inclinometer, that uses the pull-in voltage as the transduction mechanism [1.69], is a novel approach that can open the doors to a new level of sensors where the nonlinearities of the electromechanical coupling can be used to create novel sensors with more relaxed electronics. In fact, since the pull-in voltage mainly depends on the material properties and dimensions, it is believed that, a scheme to achieve an auto-calibrated and thermally compensated inclinometer can be implemented [1.70, 1.71].

The main goal of this work is the realization of a smart inclinometer that goes beyond current state-of-the-art:

- Resolutions better than current state-of-the-art commercial devices ($< 0.6m°$);
- Auto-calibrated inclinometer;
- Thermal-compensated inclinometer;
- Small form factor;

In order to achieve the envisioned smart inclinometer, intermediate goals must be achieved:

1. Design and fabrication of the MEMS structure taking into consideration the mechanical-thermal noise that can ultimately define the device resolution. Commercial available multi-project wafer and in-house processes (Iberian International Nanotechnology Laboratory - INL) are used for the fabrication of the device.

2. Implementation of the readout, control and actuation circuits. Initially, required electronic circuits are implemented at the PCB (printed circuit board) level using COTS (Commercial Off-The-Shelf) while a FPGA (Field Programmable Gate Array) is used to implement the requested digital functionalities. This approach has the advantage of enabling the implementation and testing of several control alternatives and digital interfaces. Later, an integrated circuit is designed and fabricated, including the readout electronic circuit and the digital electronics.

3. Test and characterization of the novel smart inclinometer.

1.4 Organization of the Thesis

Following the introduction and state-of-the-art review, where the current trends and challenges in inclination sensors design were analyzed, this document is organized as follows (figure 1.9):

Chapter 2 provides the theoretical background on the pull-in phenomenon (static analysis), which is mandatory to understand the sensor working principle. A brief stability analysis over the transduction method is presented, in order to drive the implementation closer to the best solution.

An overview on the existing readout circuit approaches for capacitive MEMS structures is presented in chapter 3, with special focus on the higher frequency modulation techniques, either in the continuous-time or discrete-time domain. The conclusions of this chapter define the guidelines for the integrated circuit implementation.

The complete system implementation is described in chapter 4, including the MEMS sensing element design and fabrication, as well as the mixed-signal integrated circuit. The MEMS and IC integration process is also addressed in this chapter.

The main results of the developed system are shown in chapter 5, mainly in terms of the overall system performance. Some particular results of the application specific integrated circuit (ASIC) are presented as a readout characterization.

Chapter 6 concludes this work and provides recommendations for future improvements on the current device, either in terms of sensitivity and resolution, or in terms of fully integration (supported with some simulation results).

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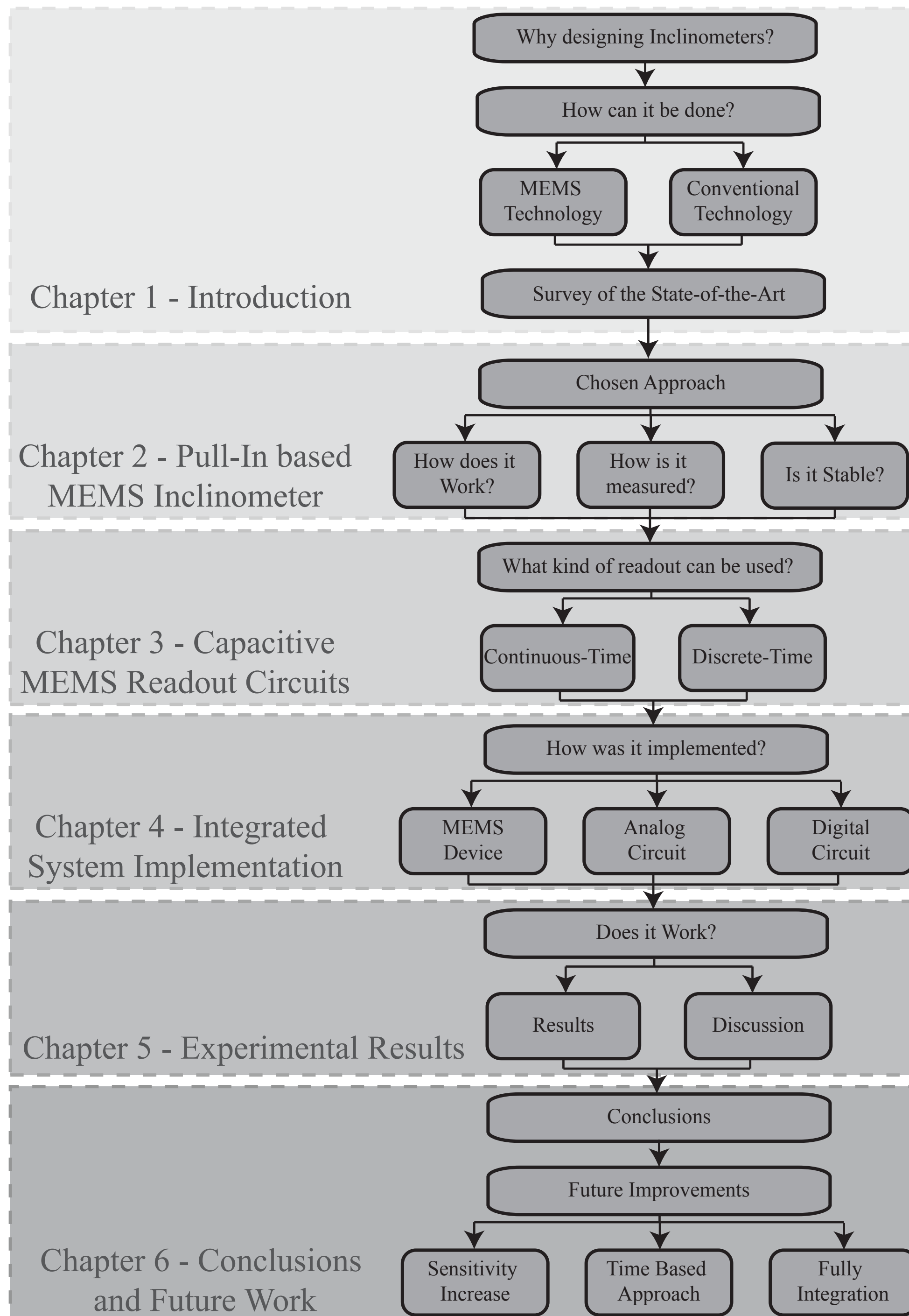

Figure 1.9: Organization chart of the thesis.

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2

Pull-In based MEMS Inclinometer

MEMS devices, due to its micro-dimensions, have unique characteristics when compared to macro-scale devices. This suggests that our propositions, based on our experience at the macro-level, are no longer valid. Some *"macro-world"* effects can be negligible in the micro-domain, while others become crucial. It is a matter of the effect to be analysed [2.1].

The coupling across various domains, even thought not exclusive, is a typical feature in MEMS. Taking into account the Paschen's effect, unlike macro devices, the electrical and mechanical coupling in the μ-domain is not limited by the electrostatic breakdown, caused by a high actuation voltage, but rather by the *pull-in* phenomenon [2.2, 2.3]. This strong coupling in small size devices leads to several new emerging phenomena, like the nonlinear pull-in. Matter of study since 1967, when the Resonant Gate Transistor (RGT) was firstly introduced [2.4], the pull-in instability is one of the most important phenomena when designing/analysing electrically actuated parallel-plate microsystems [2.5]. Considering a parallel-plate MEMS actuator, composed by a fixed and a movable electrode (anchored by a mechanical spring), when an electrical voltage is applied, an electrostatic force between the two electrodes is generated (inversely proportional to the square of

the deflection). This attraction force is countered by the restoring elastic force of the spring (linear with deflection), culminating in an unstable system for deflections, x, beyond a critical value, x_{pi}. The voltage that is needed to reach the critical deflection is named as the *pull-in voltage, V_{pi}*. A graphical representation of the pull-in phenomenon is depicted in figure 2.1, showing the stable motion of the device, for actuation voltages smaller than V_{pi}, and the instability at the critical point that originates the electrodes to snap together. This non-linearity has been studied from different perspectives [2.5–2.12]. In the application context, some novel pull-in based sensors have been proposed during the past few years [2.6, 2.8, 2.11, 2.12], while others focused on studding the dynamics and nonlinearities behind it [2.5, 2.7, 2.9, 2.10].

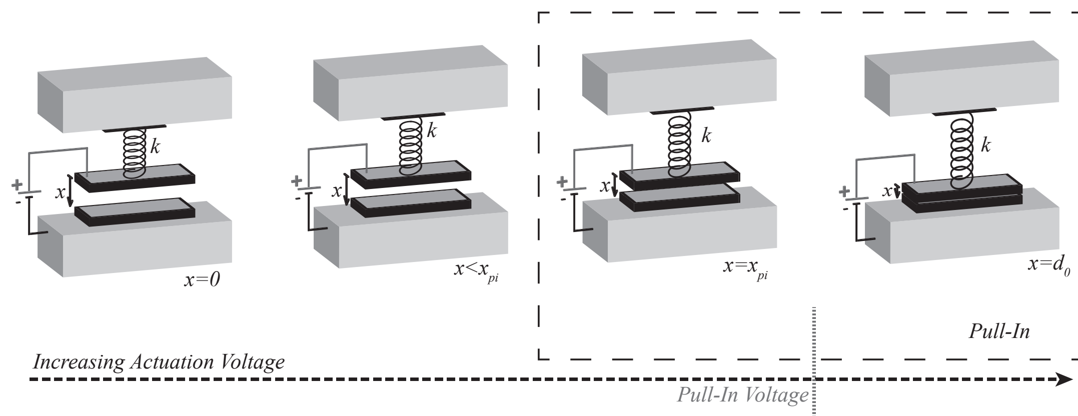

Figure 2.1: Representation of the Pull-In phenomenon in an electrostatically actuated parallel-plate MEMS device.

In this chapter, the emphasis is on understanding the nonlinear behavior in the electromechanical coupling of electrostatically actuated parallel-plate MEMS devices, and how it can be used as a way to develop stable transduction mechanisms for novel sensors. Before explaining the basic working principles of the pull-in based inclinometer, a mathematical description of the pull-in phenomenon is presented, focusing on the evolution of the equilibrium points towards instability. The leading sources of errors in the proposed transduction mechanism are also identified and studied in order to theoretically understand its effects.

2.1 Pull-In Phenomenon - Theoretical Support

The device studied during this analysis, is the simplified model of an electromechanical parallel-plate micro-actuator, depicted in figure 2.2. The gap-varying capacitor has one movable plate with 1-Degree-of-freedom (DOF) and two fixed electrodes, allowing bidirectional motion. This characteristic enables the possibility of using two different modes of operation, namely the *symmetric* and the *asymmetric* modes. The first one corresponds to the case where simultaneously two actuation voltages are applied to the actuator (between the movable plate and the two fixed ones). The second mode, and most widely used, lies on an asynchronous actuation, i.e. an actuation voltage is applied within the movable plate and one of the fixed electrodes at a time. For the purpose of this study, mainly because it enables differential measurements, the asymmetric mode is the one to be analysed.

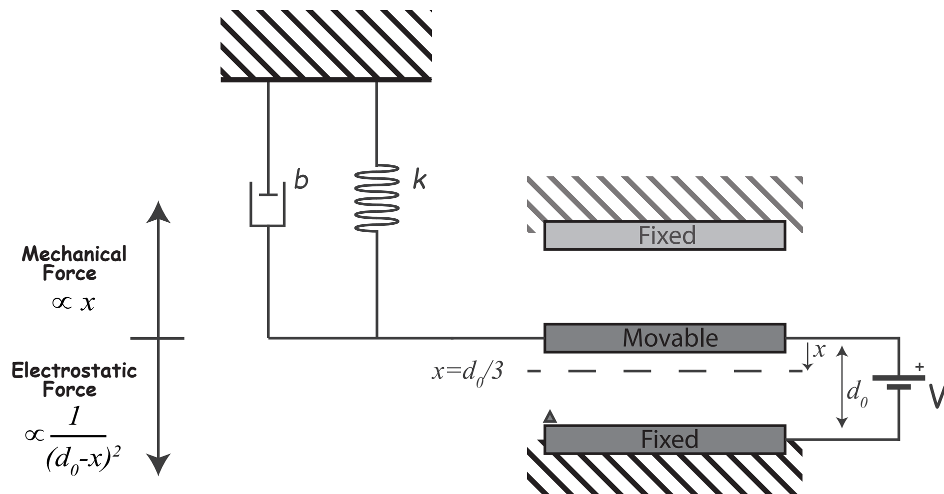

Figure 2.2: Force model of a simplified one-degree-of-freedom electrostatic micro-actuator.

Assuming the asymmetric operation mode, the analysis can be simplified to a simple parallel-plate case. Two electrodes separated by an initial gap and a linear elastic restoring force. Considering the proposed parallel-plate device at the rest position (equilibrium between all the forces), the capacitance is given by [2.13]:

$$C_0 = \varepsilon \frac{A}{d_0}, \tag{2.1}$$

where d_0 is the initial gap (distance between the plates), A is the electrodes overlapping area and ε is the dielectric constant of the material between the plates. When a voltage is applied across the parallel-plates, the 1-DOF movable electrode moves towards the fixed plate, decreasing the interplate distance. Considering a movement of x and an initial capacitance, C_0, calculated using equation (2.1), the new capacitance becomes:

$$C_x = \varepsilon \frac{A}{d_0 - x} = C_0 \frac{d_0}{d_0 - x}. \tag{2.2}$$

The movement of the device is stable until the pull-in point, where the stability of the equilibrium position is lost. The device is governed by the dynamic equilibrium of forces:

$$F_{electrostatic} + F_{elastic} + F_{damping} + F_{inertia} + F_{external} = 0. \tag{2.3}$$

The electrostatic force, $F_{electrostatic}$, generated by the applied voltage, V, attracts the movable plate towards the fixed one. For a structure with a distance between plates much smaller than the size of the plates, it is possible to assume that the electric field across the electrodes is homogeneous and has the same intensity and direction everywhere. Starting from there and relying on Coulomb's law, the electrostatic force in a given capacitor, C_0, can be expressed as [2.14]:

$$F_{electrostatic} = \frac{1}{2} V^2 \varepsilon \frac{A}{{d_0}^2} = \frac{1}{2} V^2 \frac{C_0}{d_0}. \tag{2.4}$$

As a consequence of the attraction caused by the electrostatic force, the capacitor's gap decreases, increasing the capacitance (equation (2.2)) and consequently the electrostatic force as:

$$F_{electrostatic} = \frac{1}{2} V^2 \frac{C_x}{(d_0 - x)^2} = \frac{1}{2} V^2 \frac{C_0\, d_0}{(d_0 - x)^2}. \tag{2.5}$$

With a stiffness of k, the elastic restoring force that the spring exercises on the movable plate, in opposition to the movement, is equal to $F_{elastic} = -kx$.

During the movement of the plate, the flow resistance of the fluid that fills the gap between electrodes, usually air, generates a damping force contrary to the

movement. In similarity with the electrostatic force analysis, the structure dimensions (small gap in comparison to the electrode width and length) allows the establishment of a damping mechanism called squeeze-film damping [2.15]. This force, $F_{damping}$, is proportional to the velocity as well as the damping coefficient, b, $F_{damping} = -b\frac{dx}{dt}$. The damping coefficient is defined by the physical dimensions of the structure along with the fluid properties. Another dynamic effect caused by the plate's movement is the inertia, generating a force proportional to the mass, m, $F_{inertia} = -m\frac{d^2x}{dt^2}$.

In addition, the movable plate can be acted by external forces, like acceleration, $a_{external}$, creating an additional force, $F_{external} = ma_{external}$.

The equilibrium of forces described in equation (2.3) can now be rewritten as:

$$\frac{1}{2}V^2\frac{C_0 d_0}{(d_0 - x)^2} - kx - b\frac{dx}{dt} - m\frac{d^2x}{dt^2} + ma_{external} = 0. \qquad (2.6)$$

Looking at the proposed structure as a purely mechanical system, in the absence of electrostatic actuation, equation (2.6) can be simplified into a second order system:

$$m\frac{d^2x}{dt^2} + b\frac{dx}{dt} + kx = ma_{external}, \qquad (2.7)$$

or in a more comprehensive way:

$$\frac{d^2x}{dt^2} + \frac{\omega_0}{Q}\frac{dx}{dt} + \omega_0 x = a_{external}. \qquad (2.8)$$

The resonance frequency of the mechanical system, ω_0, defined as $\omega_0 = \sqrt{\frac{k}{m}}$, and the quality factor, $Q = \frac{\sqrt{km}}{b}$, are extremely important parameters as they define the dynamic behavior of the structure. Overdamped systems are characterized by a $Q < 0.5$, while for $Q > 0.5$ the system is considered to be underdamped (shows an oscillatory behavior). If $Q = 0.5$, the system is critically damped.

Once understood the mechanics of the proposed device, it is essential to look back to the main subject of this chapter, the pull-in phenomenon.

At this point it is important to understand that the pull-in effect can be analysed static and dynamically. The static analysis assumes a quasi-static regime, where the applied voltage changes slowly enough so that the static force equilibrium is

reached at any moment in time. When this proposition is no longer valid it is mandatory to use a more universal approach, the dynamic analysis.

In this work, the pull-in analysis can be performed statically, as the control algorithm for the actuation guarantees the equilibrium state for each actuation voltage.

2.1.1 Nonlinear Static Analysis

If the applied voltage is smaller than the critical value, V_{pi}, the electrostatic force is small enough to be balanced by the elastic restoring force, creating what we call *static equilibrium*.

The static equilibrium of a electromechanical system means that either no electrostatic actuation is applied (rest position) or it changes slowly enough so that equilibrium is reached at any moment in time. Based on that, the dynamic equilibrium of forces described in equation (2.3) can be simplified to a static equilibrium by neglecting the inertia (function of acceleration) and damping forces (function of velocity). Analysing the case where no external force is applied to the structure, the equilibrium of forces can be reduced to:

$$F_{electrostatic} + F_{elastic} = 0. \tag{2.9}$$

Both the electrostatic, $F_{electrostatic}(x, V)$, and the elastic force, $F_{elastic}(x)$, depend on the displacement x. The equilibrium position for a given applied voltage, V, is obtained by solving equation (2.9). For small values of the actuation voltage V, the resultant electrostatic and elastic force dependence over the displacement is shown in figure 2.3. Three equilibrium solutions can be seen in the graph, named as x_1, x_2 and x_3.

Although mathematically correct, not all the solutions are important from a physical point of view. The third solution, x_3, is impossible to reach since it is situated beyond the total mechanical displacement d_0. Focusing on the interval of the achievable mechanical displacement ($[0, d_0]$), two equilibrium points can be found, x_1 and x_2, with the first stable and the second unstable. The stability of the equilibrium points can be understood by assuming small perturbations in the displacement x. Keeping in mind that the two forces act in opposite directions, around x_1, a small increment in the displacement causes a larger restoring

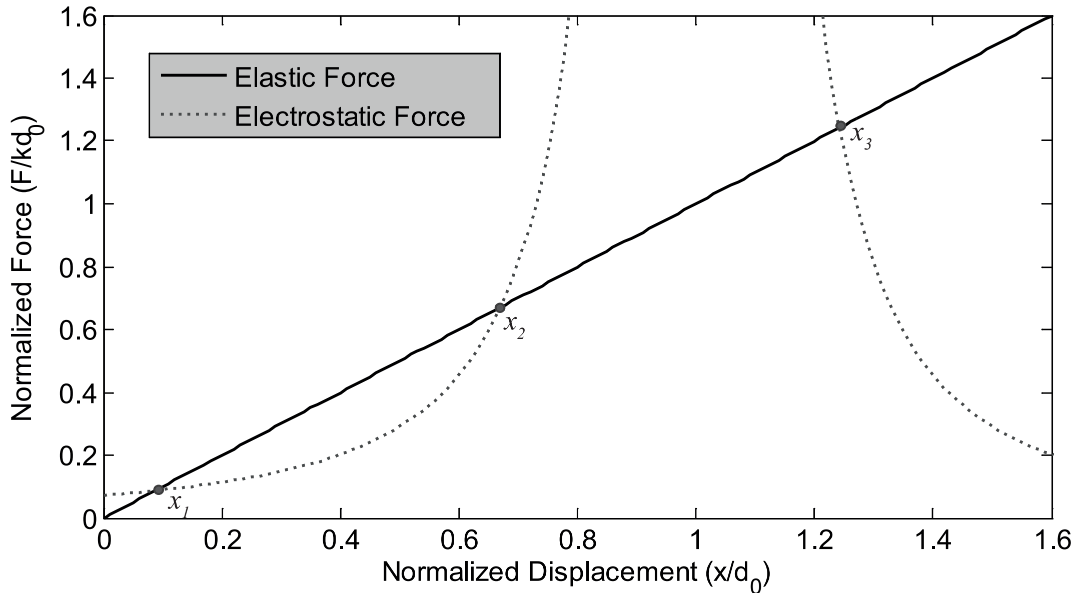

Figure 2.3: Variation of the system normalized forces with displacement x.

force ($F_{elastic}$) when compared to the repelling one ($F_{electrostatic}$), pushing back the movable plate to the equilibrium point. If the displacement decreases instead, the electrostatic becomes larger than the elastic force, and is the one that drives back the system to the equilibrium position. The same analysis can be done around equilibrium position x_2. If the displacement slightly decreases, the restoring force will push the movable electrode away from the initial equilibrium (x_2). When the displacement increases, the electrostatic force becomes larger than the restoring one, pushing the displacement even further away from x_2, making this a unstable equilibrium point.

At this point it is known that for small actuation voltages, the equilibrium of forces is possible, but beyond a critical value V_{pi}, no stable equilibrium points can be found (figure 2.4). This voltage level at which the system becomes unstable can be analytically calculated.

The previous stability analysis proved that equilibrium points exist when the elastic force balances the electrostatic one, $F_{elastic} = F_{electrostatic}$, and that those are stable when $\frac{dF_{elastic}}{dx} > \frac{dF_{electrostatic}}{dx}$. Based on these two propositions, the critical displacement x_{critic} can be defined by the threshold of stability:

$$\frac{dF_{elastic}}{dx} = \frac{dF_{electrostatic}}{dx} \quad \equiv \quad k = \frac{C_0\, d_0\, V^2}{(d_0 - x_{critic})^3} \quad \equiv \quad x_{critic} = \frac{1}{3} d_0. \tag{2.10}$$

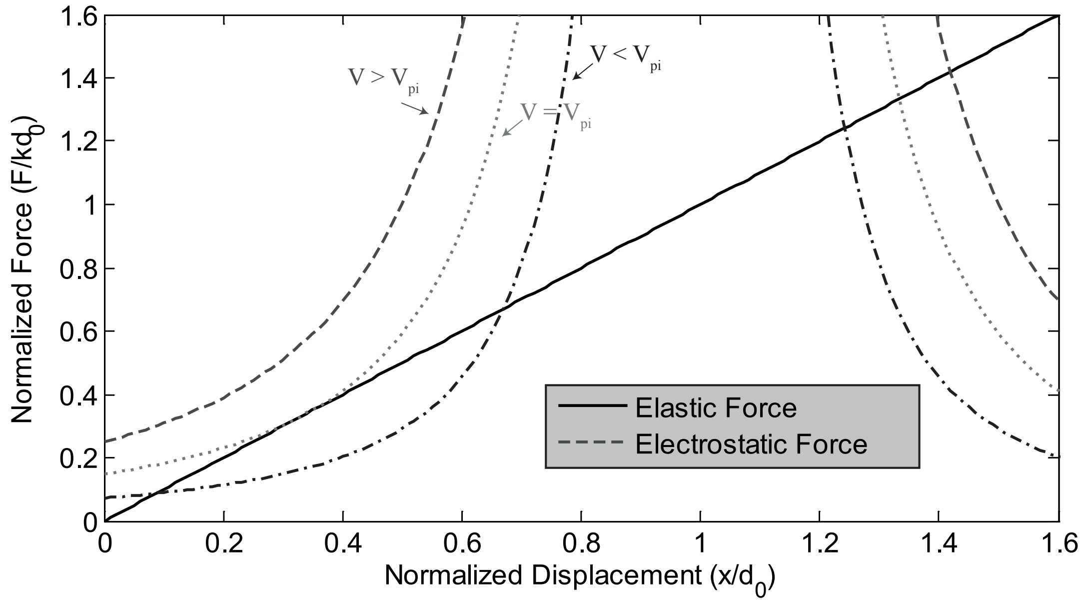

Figure 2.4: System normalized forces for different actuation voltages.

The pull-in voltage, V_{pi}, is the actuation voltage needed to reach the critical deflection, x_{critic}. The V_{pi} value can be calculated by assigning the critical displacement to equation (2.9):

$$V_{pi} = \sqrt{\frac{8}{27}\frac{{d_0}^2 k}{C_0}}. \tag{2.11}$$

When the applied voltage is higher than the pull-in voltage, the elastic force can no longer compensate for the electrostatic force and the movable plate will snap against the fixed one. In real electromechanical devices, the contact between the two electrodes should be avoided, preventing the electrical short-circuit as well as any other mechanical damage. It can be done by creating a mechanical stopper where the movable plate gets stopped before it reaches the surface of the other plate.

2.1.2 Using the Pull-In Voltage as a Transduction Mechanism

The pull-in voltage, V_{pi}, of an electrostatic parallel-plate actuator, as expressed in equation (2.11), is a function of the initial capacitance C_0, which in turn depends

on the initial gap d_0 (equation (2.1)). Considering now that the microstructure is tilted by an angle of θ, the movable electrode has a mass (m) that experiences a component of the gravitational force in the plane of the movable electrode, like it is shown in the force diagram presented in figure 2.5.

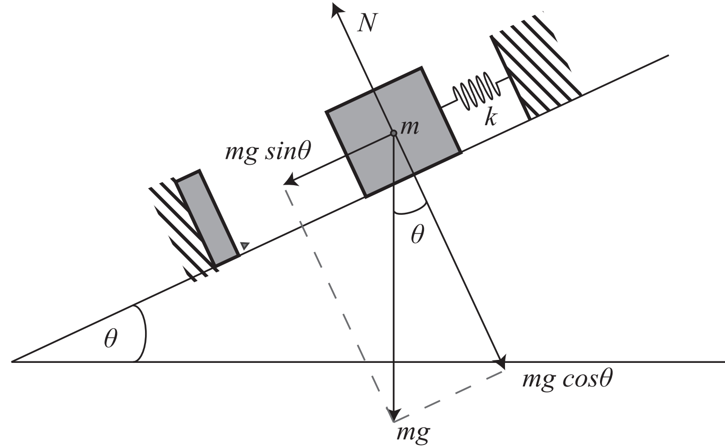

Figure 2.5: Force diagram for the 1-DOF parallel-plate device when exposed to an inclination θ.

The electrode motion generated by the in-plane force is limited by the elastic restoring force of the spring:

$$F_{tilt} = F_{elastic} \quad \equiv \quad mg\,sin\,\theta = kx \quad \equiv \quad x = \frac{mg\,sin\,\theta}{k}, \tag{2.12}$$

where x is the resultant displacement. The new gap between the electrodes, d, depends on the direction of the external force (positive or negative inclination) as $d = d_0 \pm x$.

This gap change leads to a different initial capacitance, C_x, and consequently a distinct pull-in voltage:

$$V_{pi} = \sqrt{\frac{8}{27}\frac{d^2k}{C_x}} \quad \equiv \quad V_{pi} = \sqrt{\frac{8}{27}\frac{d^3k}{\varepsilon_r wl}} \quad \equiv \quad V_{pi} = \sqrt{\frac{8}{27}\frac{(d_0 \pm x)^3 k}{\varepsilon_r wl}}. \tag{2.13}$$

Relying on that principle, if the pull-in voltage is continuously measured, the changes in the pull-in voltage are proportional to the inclination experienced by the MEMS structure. The pull-in voltage is determined by generating a ramped

voltage (sawtooth waveform), until the pull-in point is reached, like it is depicted in figure 2.6.

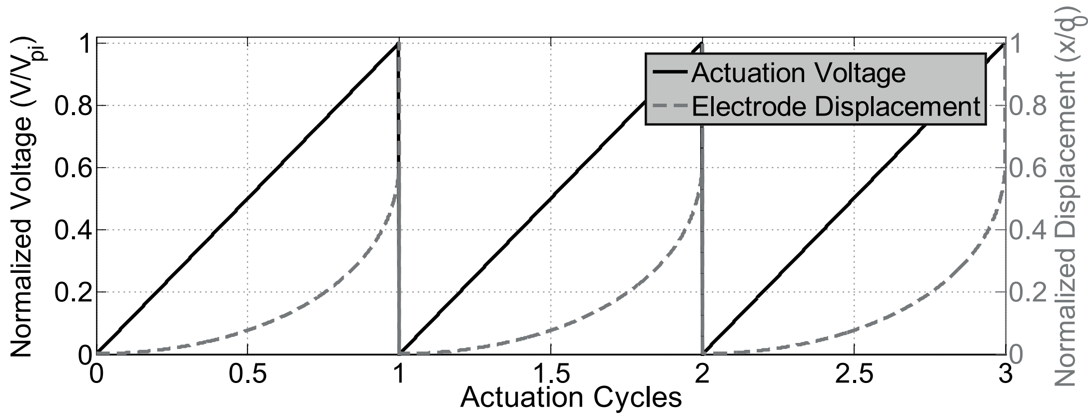

Figure 2.6: Representation of the pull-in voltage continuous measurement.

Concerning the actuation waveform, the applied voltage needs to be slowly increased, guaranteeing this way the previously explained static equilibrium at each voltage increment. This aspect will be further analysed in this chapter.

2.1.3 Direct Transduction vs Pull-In Voltage Based

One of the main advantages of using a pull-in voltage based transduction mechanism over the traditional direct transduction, like resistive, capacitive, resonant or thermal to name the most common, is the digital output of the sensor.

Moreover, the pull-in transduction does not require low noise, high sensitive readout electronics, since pull-in is characterized by a huge displacement change and therefore easy to detect.

A comparison between the pull-in approach and a direct differential capacitive transduction was performed [2.6]. The sensitivity results of the capacitive transduction showed that, in order to achieve similar resolution, much more precise and complex readout electronics are required. In the particular studied case, a readout circuit capable of measuring $6aF$ would be required. (The results that support these statments are presented in the experimental verification chapter (section 5.3.5)).

2.2 Principle of Operation

The main advantages of using the nonlinearities in the electromechanical coupling of MEMS devices as a way to create transduction mechanisms were already addressed. In what follows, the main characteristics of the sensor's working principle are presented.

2.2.1 Differential Operation

At the beginning of this chapter, in section 2.1, a simplified representation of the parallel-plate device was shown (figure 2.2). This type of differential capacitor scheme (two fixed and one movable electrode (figure 2.7)) allows pulling the structure to pull-in at both sides of the capacitor (named as left and right side).

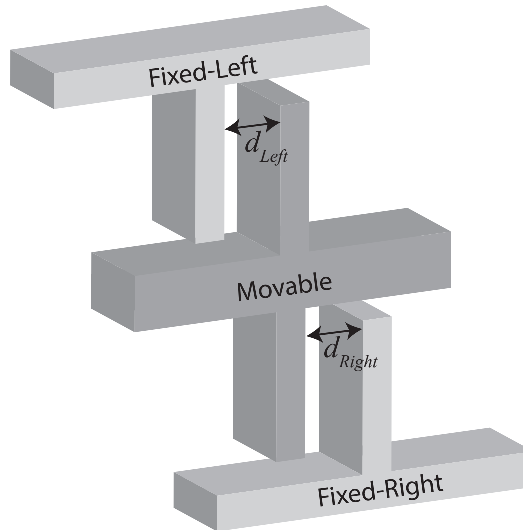

Figure 2.7: Drawing of the differential parallel-plate actuator.

This differential operation results in two different *asymmetric pull-in voltages*:

$$V_{pleft} = \sqrt{\frac{8}{27}\frac{{d_{left}}^3 k}{\varepsilon_r wl}}, \quad and \quad V_{pright} = \sqrt{\frac{8}{27}\frac{{d_{right}}^3 k}{\varepsilon_r wl}}. \tag{2.14}$$

Recalling that the tilting of the sensor creates a change in the gap (equation (2.12)) and consequently a change in the pull-in voltage (equation (2.13)), it is crucial to notice that this variation is opposite for each side, as $d_{left/right} = d_0 \pm \frac{mg\,sin\,\theta}{k}$.

It means that when the gap to the left fixed electrode, d_{left}, decreases (smaller V_{pleft}), the right side gap, d_{right}, increases by the same value (larger V_{pright}).

If the asymmetric pull-in voltages measurement is done alternately (figure 2.8), the difference in the pull-in voltages gives the measure of the that tilt the device is experiencing:

$$\Delta V_{pi}(\theta) = V_{pleft}(\theta) - V_{pright}(\theta). \tag{2.15}$$

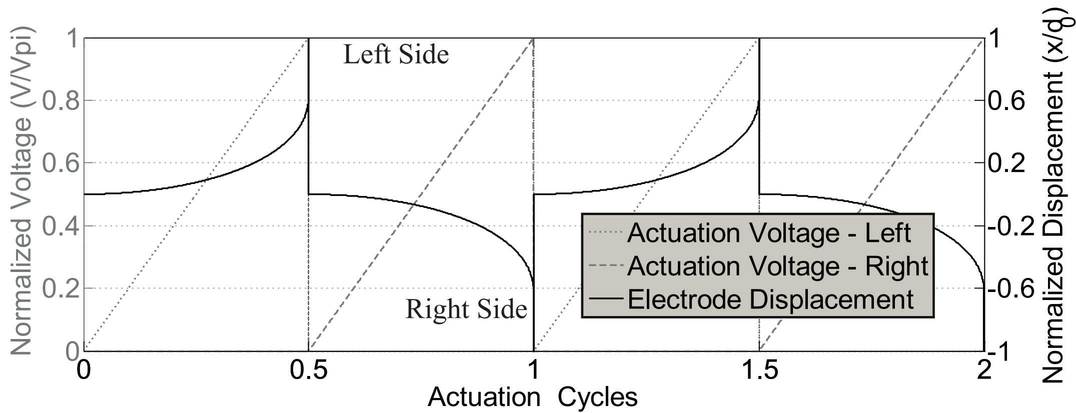

Figure 2.8: Representation of the differential pull-in voltage continuous measurement.

The use of a differential scheme brings a number of advantages, such as the improvement on the linearity and sensitivity of the sensor or the possibility of implementing auto-calibration and compensation mechanisms. Any external variation in the environment where the sensor is operating, other than inclination, will affect both pull-in voltages in the same proportion. Differential measurement will therefore cancel-out the pull-in voltages variations caused by external factors. In addition, the nominal pull-in voltage (in absence of inclination) can easily be calculated by using the mean of the two asymmetric pull-in voltages. Of particular importance is the device's sensitivity to temperature changes and will be addressed further in this chapter. At this point, it just needs to be mentioned that, as both pull-in voltages share the same mechanical spring and the device is symmetric, the differential pull-in voltage measurement will cancel-out (or at least minimize) the variations due to temperature changes.

2.2.2 Pull-In Detection

It has already been demonstrated that the sensor relies on the differential pull-in voltage measurements. The question that arises is: *how is the pull-in going to be detected?*

The pull-in phenomenon is characterized by the sudden change in the distance between electrodes of the MEMS device. This displacement needs to be quantified in order to detect the critical deflection ($x_{critic} = \frac{1}{3}d_0$). Taking into account that the proposed MEMS devices uses parallel-plate electrostatic actuators, the most wise way of measuring the displacement is by creating a separate set of sensing electrodes in the same mechanical structure.

In figure 2.9, a simplified schematic of the proposed MEMS device is shown, including the separate sensing and actuation electrodes. In resemblance with the actuation parallel-plates, the displacement sensing can be used in a differential way, through the creation of independent sets of electrodes for the left and right side.

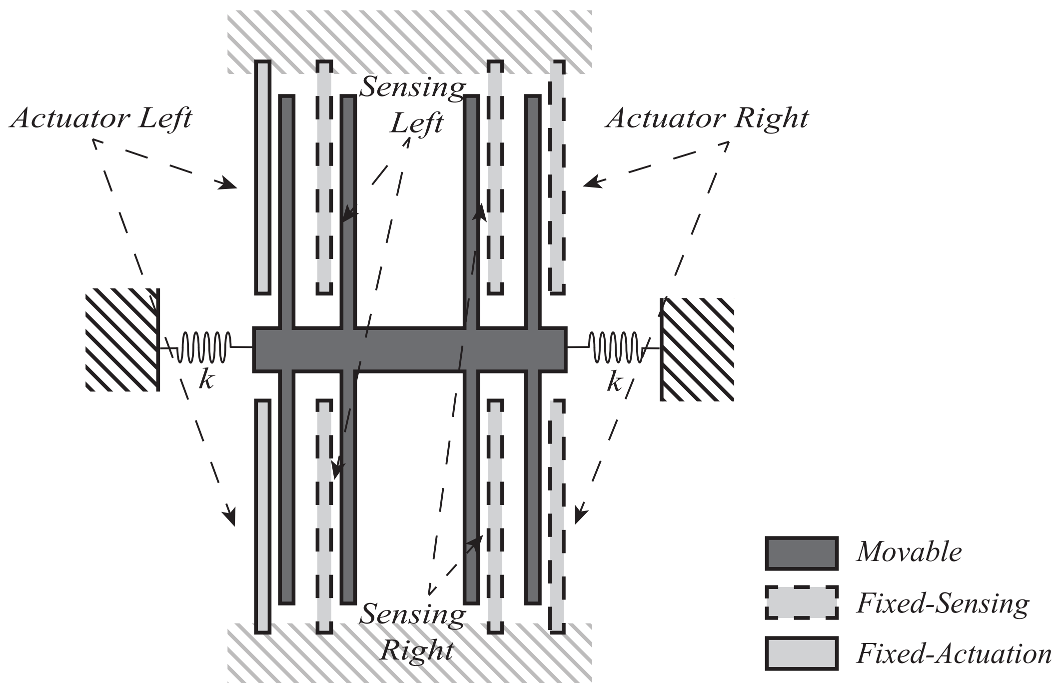

Figure 2.9: Schematic of the parallel-plate device with separate sensing and actuation electrodes.

The displacement change is now transduced to a variation in the sensing electrodes

capacitance. This change can then be detected by using a capacitive readout circuit that converts the sensing capacitance into voltage. By comparing the readout voltage with a reference (corresponding to a position beyond the critical displacement, x_{critic}), the pull-in point can be detected.

The choice of the reference voltage does not need to be very precise. There are only two constraints when choosing the reference: on one hand the reference value must represent a displacement beyond pull-in (1/3 of gap) while on the other hand the reference point shouldn't be too close to the maximum displacement, in order to prevent the structure from hitting the mechanical stoppers before returning to the rest position. Any change in the reference, while respecting this constrains, will not have any effect on the sensors' performance.

2.2.3 Actuation Voltage

Concerning the performance maximization of the sensor, the actuation voltage needs to be carefully controlled. The used waveform should take into account two limitations. First, given that high resolution is one of the key features of the proposed inclinometer, the maximum resolution of the actuation system should be used. Second, dynamic effects should be minimized by generating slow ramp voltages, that allows stable movements of the MEMS device. This would also prevent any malfunction resultant from a possible overshoot in underdamped devices.

If a single ramp voltage is used, for very high resolutions, this would result in a very slow ramp, greatly reducing the bandwidth of the sensor. Adding a DC (direct current) value to the ramp voltage would reduce the time per measurement, but some dynamic effects can appear in the step transition, increasing the noise level of the sensor. Hence, in order to increase the sensor's bandwidth while minimizing dynamic effects, a dynamic ramp voltage is used, where the slope of that ramp is dependent on the previous pull-in voltage value ($pVpi$), like it is shown in figure 2.10.

By using this dynamic ramp, the slope is dynamically decreased, getting to the minimum ramp slope when the applied voltage is near the critical value.

The digital output of the sensor, pointed as a key advantage of the proposed approach, is achieved by using a digital-to-analog converter (DAC) to generate the actuation voltage. Since the actuation voltage is critical for the sensor's resolution,

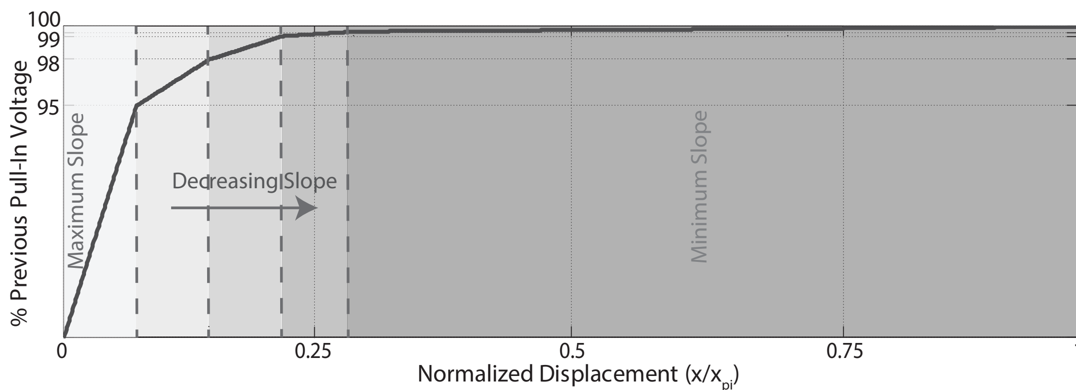

Figure 2.10: Representation of the dynamic actuation mechanism.

the DAC output total noise should be below it's minimum available step (1 LSB (least significant bit)).

2.3 Pull-In Voltage Stability

The pull-in static analysis presented in section 2.1.1 showed that the pull-in voltage is defined from the loss of the elastic and electrostatic equilibrium. Designing this type of structures requires the study of a few details. Microfabricated silicon beams usually exhibit residual stress that may cause buckling of the beam and strongly influences the behavior and temperature dependence of the device. To improve the long-term stability of the pull-in voltage and avoid problems related with residual-stress, single-sided anchored beams with the other end-free standing should be used [2.16].

Even if design precautions have been taken, a number of sources of errors, that result from the device operation, need to be analysed. The effect of the main sources of uncertainty on the pull-in voltage is analysed in the following sections.

2.3.1 Temperature

The pull-in voltage dependence over the dimensions of the spring and the electrodes' initial gap, implies an obvious relation with thermal expansion. The elastic restoring force of the beam varies inversely proportional with beam length, which increases with temperature. Besides that, the modulus of elasticity (Young's Modulus, E) in silicon is also dependent on temperature (negative relation). The com-

bination of these effects results in a temperature coefficient, TC, for the pull-in voltage.

Considering that the thermal expansion coefficient (α) is positive for silicon ($\alpha > 0$), the parallel-plate capacitor initial gap decreases with temperature (T) as $d_0(T) = d_0 - t\alpha T$. The electrodes dimensions change is represented in figure 2.11, were t serves as the electrode width.

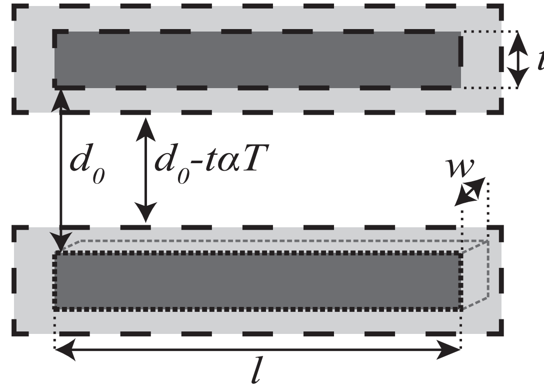

Figure 2.11: Parallel-plate dimensions changing with thermal expansion.

At a given temperature, the initial capacitance becomes:

$$C_0(T) = \frac{\varepsilon_r tl(1 + 2\alpha T)}{d_0 - t\alpha T}. \tag{2.16}$$

If the Young's Modulus thermal coefficient is represented by β (negative for silicon ($\beta < 0$)), the spring constant develops into:

$$k(T) = k(1 + (\alpha + \beta)T). \tag{2.17}$$

Taking into account the effect of temperature in the initial gap, $d_0(T)$, together with the capacitance change, represented in equation (2.16), and the spring constant (equation (2.17)), the pull-in voltage at a given temperature can be written as:

$$V_{pi}(T) = \sqrt{\frac{8}{27}\frac{d_0(T)^2 k(T)}{C_0(T)}} \equiv$$
$$V_{pi}(T) = \sqrt{\frac{8}{27}\frac{(d_0 - t\alpha T)^2 (k(1+(\alpha+\beta)T))}{\frac{\varepsilon_r tl(1+2\alpha T)}{d_0 - t\alpha T}}}. \tag{2.18}$$

The pull-in voltage thermal coefficient, TC, is now given by the derivative to temperature ($TC = \frac{\partial V_{pi}(T)}{\partial T}$). It is known that $|\beta| << 1$ and $|\alpha| << 1$ [2.17], what allows a simplification in the thermal coefficient calculation, as the quadratic therms can be neglected:

$$TC = \sqrt{\frac{8}{27}\frac{{d_0}^2 k}{C_0}} \left[\frac{\alpha - \beta + 3\alpha\frac{t}{d_0}}{2(1+(\alpha+\beta))}\right] \sqrt{\frac{1+(\alpha - \frac{t}{d_0}\alpha + \beta)\ T}{1+2\alpha T}}. \tag{2.19}$$

From the thermal coefficient calculated in equation (2.19), it is important to hold that, given the positive thermal expansion ($\alpha > 0$) [2.18], the negative Young's modulus temperature coefficient ($\beta < 0$) [2.19], and $|\beta| >> |\alpha|$, the pull-in voltage temperature coefficient is negative and as it depends on the temperature, T, is not constant.

Thermal Compensation

In theory, since both the spring (due to Young's Modulus changes and thermal expansion) and gap (due to thermal expansion) change with temperature [2.20], both left and right asymmetric pull-in voltages will also change. Nevertheless, as both pull-in voltages share the same mechanical spring and the device is symmetric, the differential pull-in voltage measurement should cancel-out the variations due to temperature changes. In that sense, the approach proposed here performs temperature compensation directly at the mechanical domain.

To validate this assumption, for the sake of simplicity, in a first step, the pull-in voltage thermal coefficient can be considered to be constant, $\alpha = cnst(\frac{TC}{V_{pin}})$, where V_{pin} is the nominal asymmetric pull-in voltage. If V_{pleft_0} and V_{pright_0} are the left and right asymmetric pull-in voltages at T_0 temperature, the differential pull-in voltage can be expressed as:

$$\Delta V_{pi}(T) = V_{pleft_0}(1 + \alpha(T - T_0)) - V_{pright_0}(1 + \alpha(T - T_0)). \quad (2.20)$$

The differential pull-in voltage expression (equation (2.20)) shows that, when the two pull-in voltages have the same value (absence of inclination), no thermal effects should be observed. But when the difference starts to increase, caused by the tilting of the sensor, the temperature component for each side becomes different, creating that way a temperature variation in the differential pull-in voltage. It means that, the pull-in voltage thermal coefficient TC expressed in equation (2.19) is different for each asymmetric pull-in voltage ($TC_{left} \neq TC_{right}$). Moreover, it can be deduced that the TC of the differential pull-in measurement (ΔV_{pi}) changes with the inclination.

Even though it is not possible to completely cancel temperature effects just by using differential measurements, they are strongly minimize when compared to the single side operation.

In addition to this first stage compensation, supplementary mechanisms can be used. Taking into account that the pull-in voltage in absence of inclination, named as nominal pull-in voltage, V_{pi_n}, can be found at any moment in time ($V_{pi_n} = \frac{V_{pleft}+V_{pright}}{2}$), it can be applied for compensation.

Once found the differential (ΔV_{pi}) and nominal (V_{pi_n}) pull-in voltage thermal coefficients, respectively $TC_{\Delta V_{pi}}$ and $TC_{V_{pi_n}}$, a compensation factor δ can be calculated ($\delta = \frac{TC_{\Delta V_{pi}}}{TC_{V_{pi_n}}}$) and applied as:

$$Compensated\ \Delta V_{pi} = \Delta V_{pi_T} + \delta(V_{pi_n T} - V_{pi_n T_0}), \quad (2.21)$$

where ΔV_{pi_T} is the measured differential pull-in voltage at a given temperature T, $V_{pi_n T}$ is the nominal pull-in voltage at that temperature and $V_{pi_n T_0}$ is the same voltage at the calibration temperature T_0.

It is believed that, other process related factors, like charge effects, might also influence the pull-in voltage dependence on temperature. Even though the presented compensation method should cancel these effects, further investigation is required.

The effectiveness of the proposed compensation mechanism is tested and discussed in the results chapter of this document.

2.3.2 Charge Effects

The studied capacitive MEMS actuators are comprised of parallel electrodes separated by a dielectric medium. In micromachined devices (figure 2.12), the electrostatic actuation is prone to parasitic charge buildup on dielectric layers, usually thin polymer layers that result from the DRIE processing. The surface charges yield a residual electrostatic force, which might cause a drift in the measured pull-in voltage.

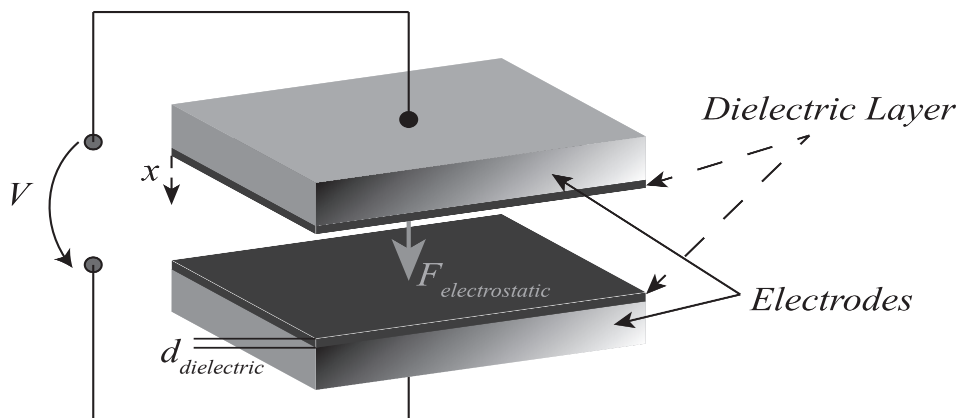

Figure 2.12: Parallel-plate MEMS actuator with dielectric layers.

Dielectric charging reliability issues have been deeply studied on RF (radio frequency) MEMS switches [2.21–2.25]. In these devices, the charging of the dielectric can even set the end of life for the switch, if the charge density exceeds a critical amount. The same principle can be applied on pull-in based MEMS sensors, where the pull-in voltage is used as the transduction mechanism.

When the parallel-plate structure is actuated for a long period of time, the large electric field applied to the dielectric induces charge that will be trapped in the dielectric and will start to accumulate **??**. From literature on RF MEMS switches, the dielectric charging can be divided in three major charging modes, two of them take place when the electrodes are not in contact (contactless charging), while the other (major one) takes place when they snap together (contacted charging). Since in our devices the contact is avoided by mechanical stoppers, only the contactless charging needs to be considered.

While defining contactless charging, two different charging modes can be specified, the injection mode and the induced mode **??**. Induced charging is the effect gener-

ated when a dielectric is placed inside an electric field, through the redistribution of internal charges and orientation of the dipoles, if any. The injection mode of contactless charging is a result of the injection from an enhanced electric field at sharp edges in the side wall of the electrode [2.22].

Factors that affect Dielectric Charging

Although it is a common problem, the physics behind the dielectric charging in MEMS devices are not completely clear yet. Even though, it is assumed that when a voltage is applied, the charges will be trapped either in the dielectric surface (surface charging), or in its interior (bulk charging). When the applied voltage generates a sufficiently high electric field, it is possible that the charges are injected in the dielectric due to a phenomenon similar to the Poole-Frenkel effect [2.26].

- Dielectric Thickness

  The effect of the dielectric thickness on charging effects in RF MEMS switches was studied in [2.27]. Assuming that the charge accumulation does not exist in the absence of a dielectric, the relation between the dielectric thickness and the accumulated charge can be defined by:

$$\sigma(d_{dielectric}) = \sigma_0 d^{\gamma}, \tag{2.22}$$

  where σ represents the accumulated charge, $d_{dielectric}$ is the dielectric thickness, while γ and σ_0 are experimentally obtained parameters. It is then possible to assume that for the same electric field, the thicker the dielectric the higher the charge injected [2.27, 2.28].

- Temperature

  A model that relates temperature with the amount of charge injected in the dielectric and the consequent pull-in voltage deviation, can be found in [2.23]. Based on experimental results, the charge density in the dielectric increases with the temperature according to:

$$Q^J = Q_{0J}\ exp\left(\frac{-E_A}{kT}\right), \tag{2.23}$$

where Q_{0J} is an experimentally obtained parameter, E_A the activation energy, k the Boltzmann constant and T the temperature.

- Humidity

  When the continuous operation of RF MEMS switches was tested at different humidity conditions, a positive linear dependence between the relative humidity and the accumulated charge was found [2.29]. It has also been proved that, an increase in the humidity will drastically reduce the dielectric charging time constant, what leads to a higher amount of charge trapped in the device, mainly due to surface charging [2.30].

- Packaging

  As a direct outcome of the proved humidity dependence, a suitable packaging that reduces the relative humidity, preferable below 1%, is of great interest because it restrains the charge density variation, leading to an increased lifetime [2.23]. By minimizing the bulk charging through the regulation of the humidity, the total charge accumulation is highly decreased (surface charging is negligible).

Pull-in variation due to Charge Effects

In order to quantify the pull-in voltage deviation, the amount of charge trapped in the dielectric needs to be calculated. By measuring the electric current during the charge and discharge phase of the MEMS device, the injected charge can be quantified. When the device is actuated (charge phase), the electric current of the actuation signal behaves in accordance with the following expression [2.21]:

$$I_{charge} = qA\frac{dQ}{dt} \;=\; qA\sum_{J}\frac{Q^J}{{\tau_c}^J}exp\Big(\frac{-t_{on}}{{\tau_c}^J}\Big), \qquad (2.24)$$

where q is the charge of one electron, A the area the dielectric and Q is the total charge. The maximum charge that the dielectric can hold for a given actuation voltage is represented by Q_J, ${\tau_c}^J$ is the time constant of the dielectric charging and t_{on} is the time during which the voltage is applied to the actuators' electrodes. The discharging process can be modeled in a similar way, by using the discharge time constant (${\tau_d}^J$) and the time without applying any voltage (t_{off}) [2.21]:

$$I_{discharge} = -qA\frac{dQ}{dt} \;=\; -qA\sum_J \frac{Q^J}{{\tau_d}^J} exp\Big(\frac{-t_{off}}{{\tau_d}^J}\Big). \tag{2.25}$$

The charge density, Q^J, is dependent of the actuation voltage, according to:

$$Q^J = Q_0^J exp\Big(\frac{V}{V_0^J}\Big), \tag{2.26}$$

with Q_0^J and V_0^J being experimentally obtained parameters. The time constant, τ^J, proved to be independent of the actuation voltage. The total charge density in the dielectric can now be expressed as:

$$Q = \sum_J Q^J \left[1 - exp\Big(\frac{-t_{on}}{\tau_c^J}\Big)\right] exp\Big(\frac{-t_{off}}{\tau_d^J}\Big). \tag{2.27}$$

As the result of this total charge density in the dielectric (equation (2.27)), the pull-in voltage variation can be calculated using:

$$\Delta V = \frac{qhQ}{\varepsilon_0 \varepsilon_r}, \tag{2.28}$$

accepting h as the dielectric thickness, Q the total charge density calculated using equation (2.27), ε_0 and ε_r the vacuum and air permittivity correspondingly.

As a summary, in terms of pull-in, the total charge density trapped in the dielectric creates an offset from the pull-in voltage initial value. The value of the offset depends on the electrical properties (charge density and dielectric permittivity) as well as the dielectric thickness.

Once again, the use of differential measurements works as a compensation mechanism in the mechanical domain for the undesired effects. In the specific case of charge effects, if the dielectric thin layers in the device have the same physical and electrical properties (thickness, permittivity and charge density), the charge related offset is completely canceled. It happens that, neither the dielectric thickness is uniform across the whole device, neither the charge density is equal for both sides (if the device is tilted, different actuation voltages are used).

Additional techniques can be used during the device operation to minimize even further these effects. One of the leading approaches is the use of bipolar actuations

(positive and negative voltages) instead of just positive actuation voltages [2.24]. This principle is based on the fact that when a positive voltage is applied to the electrostatic actuator, positive charges will be injected in the dielectric, while negative charges are injected during a negative actuation. Assuming a symmetric actuation (same actuation time and amplitude for both voltages), the negative charges will counteract the positive ones, resulting in a charge density equal to zero. However, as the charge injection is not exactly symmetric for positive and negative voltages, a residual charge density can still remain in the dielectric. Along with this bipolar actuation technique, the total charge density in the dielectric can be decreased by increasing the time between each actuation (off time), granting more time for the dielectric to discharge. These techniques are going to be tested during the experimental tests, aiming to minimize the described effects.

2.3.3 Humidity

Besides the temperature effect, changes in environmental factors, like the surrounding atmosphere humidity, can affect the stability of any capacitive structure. This strong dependence made capacitive detection the most commonly used measurement technique in commercial humidity sensors [2.31, 2.32].

The formerly presented pull-in analysis on air-gap capacitive structures was derived for ideal capacitors, with the permittivity of the air considered as a constant. However, the relative humidity (RH) might change the capacitance due to two different contributions. The first contribution is the air permittivity dependence on its RH [2.33]. The second one is related with the dielectric layer that lays on top of the electrodes due to the fabrication process (explained in charge effects section). Since the permittivity of water is much larger than that of most polymers [2.33, 2.34], upon water absorption a huge variation in the dielectric constant will be noticed.

To minimize these effects, the use a differential mode of operation can be considered as an appropriate solution. In the particular case of pull-in voltage measurements, if the device has no inclination ($V_{pleft} = V_{pright}$), the pull-in voltage variation due to the dielectric constant change is totally canceled in the differential mode. But when it is tilted, the contribution of the dielectric constant change on each voltage becomes different.

The effectiveness of the differential compensation was theoretically tested using

a dielectric constant variation of ±20% at a given inclination. The results were normalized to the nominal pull-in voltage, $V_{pi_n} = \frac{V_{pleft} - V_{pright}}{2}$ and are depicted in figure 2.13, showing that, a 14% change in the pull-in voltage is reduced to a less than 4% variation just by using the differential measurement.

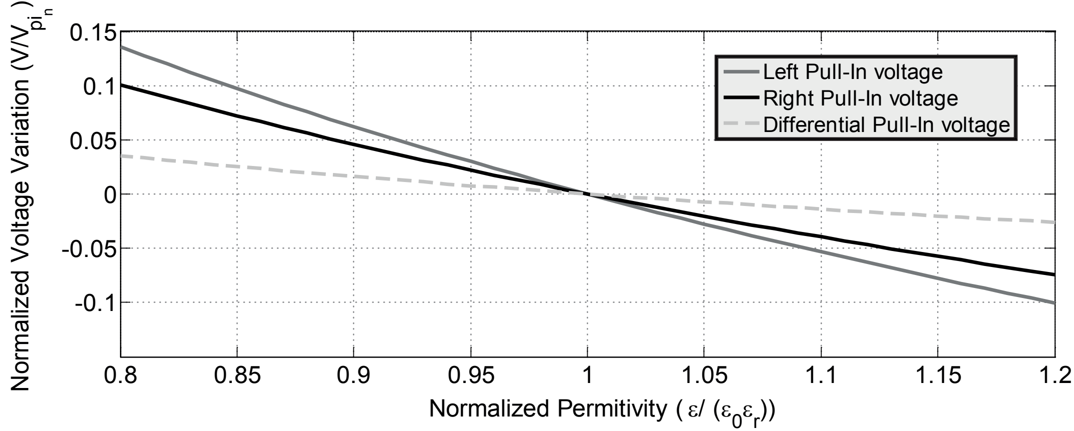

Figure 2.13: Effect of permittivity variation on pull-in voltage.

2.3.4 Noise

The pull-in voltage total noise can have a mechanical or an electrical origin [2.35].

In the mechanical domain, the molecular collision in the surrounding air creates an agitation in the movable structure, which is know as the mechanical-thermal noise [2.36]. Its contribution can be expressed as an additional noise force, F_{noise}, [2.36]:

$$F_{noise} = \sqrt{4k_BTb} \quad [N/\sqrt{Hz}], \tag{2.29}$$

where k_B is the Boltzman's constant, T is the temperature in Kelvin and b is the damping coefficient in $N.m/s$.

This extra noise force will generate a noise-displacement, x_{noise}, that adds to the structure displacement, resulting in a different pull-in voltage value. Considering the mass of the movable structure, m, the mechanical-thermal noise can be represented as a tilt noise:

$$\theta_{noise} = sin^{-1}\left(\frac{\sqrt{4k_BTb}}{9.8m}\right) \quad [^o/\sqrt{Hz}]. \tag{2.30}$$

The electrical contribution to the total measured noise is the one from the pull-in detection mechanism (readout-circuit), $N_{ReadOut}$, together with the actuation voltage noise, $N_{Actuation}$.

The total noise is the combination of all the noise sources, where the external acceleration noise, $N_{external}$, can be included: ${N_{total}}^2 = {N_{Mechanical}}^2 + {N_{ReadOut}}^2 + {N_{Actuation}}^2 + {N_{external}}^2$. It is expected to have the mechanical-thermal noise as the dominant noise source, and therefore the limiting factor for the sensor's resolution.

2.4 Conclusions

In this chapter, the theory behind the pull-in voltage based inclinometer has been explained. The study of the electromechanical coupling as a nonlinear static effect, in 1-DOF MEMS devices, allowed the understanding of the instability between the electrostatic force (increases non-linearly with displacement) and the elastic restoring force (increases linearly with displacement) at the pull-in point ($\frac{1}{3}d_0$). The voltage that generates the critical electrostatic force is called pull-in voltage, V_{pi}, and is used as the transduction mechanism. This well-defined voltage depends on the geometry and materials of the microstructure (capacitance, spring stiffness and rest-position gap), as well as on the external acceleration caused by the tilt of the sensor (change of the initial displacement).

The differential operation, using the two asymmetric pull-in voltages, improves the sensitivity of the sensor and works as a 1st stage compensation mechanism. A block diagram that summarises the proposed inclinometer is depicted figure 2.14.

The key element is the electrostatically actuated parallel-plate microstructure with distinct actuation and sensing electrodes. Since the device is asymmetrically actuated, two digital switches can be placed between the DAC and the microstructure actuators to enable the switching between the DAC output and the ground. This switching enables that the same output voltage is used on both actuation sides (eliminating differences in the actuation). It can also be used to prevent the movable part of the structure from hitting the mechanical stoppers, increasing the system's reliability (voltage is removed from the actuators as soon as pull-in is detected, enabling the movable structure to return to the rest position without reaching the stoppers). The pull-in phenomenon is detected through a sudden change in the sensing electrodes measured capacitance. This abrupt change is

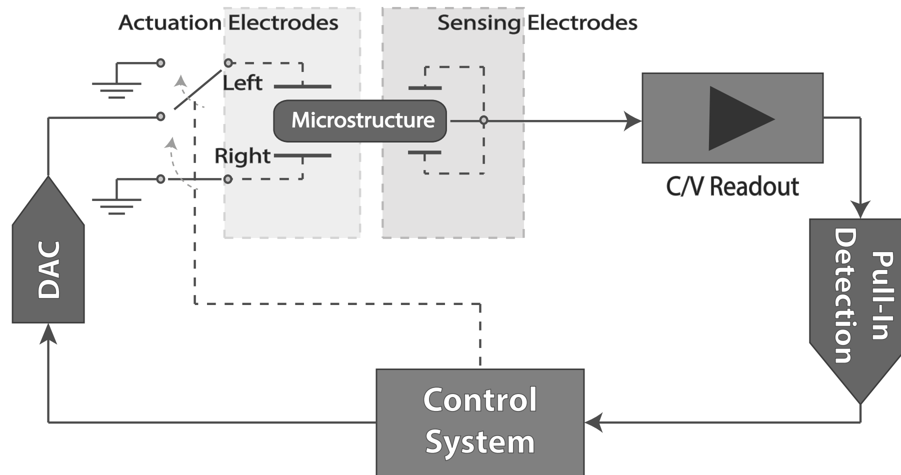

Figure 2.14: Simplified block diagram of the pull-in voltage based inclinometer.

detected by comparing the output of the readout circuit (C to V converter) with a reference voltage (corresponding to a position beyond the pull-in displacement, i.e., beyond 1/3 of gap).

The whole system in controlled by a digital unit, including the generation of the actuation voltage.

The stability limitations of the pull-in voltage were analyzed, showing that the proposed transduction mechanism is ultimately limited by the mechanical noise of the microstructure. The study of the unwanted effects of temperature, humidity and charge build-up proved the importance of using differential measurements as a way to improve the performance of the sensor. Additional compensation mechanisms were addressed and need to be tested during the characterization of the sensor.

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3

Capacitive MEMS Readout Circuits

In general, the readout of a micro-mechanical device involves converting the position or displacement of the device into a measurable form [3.1]. This information can be encoded in different forms, such as capacitance, resistance, or voltage, depending on the readout mechanism [3.2]. In section 2.2.2, it was referred that, the pull-in detection would be performed by a capacitive readout of the MEMS device sensing electrodes. Hence, the focus on this chapter is on analysing the existing capacitive readout circuit approaches.

Capacitive sensing is one of the most dominant mechanisms for MEMS inertial sensors, due to its high accuracy, low power and low cost properties [3.3, 3.4]. The performance of these high sensitivity capacitive sensors is dependent on two main parts: the sensing element (MEMS device) and the readout circuit. With the continuous request for higher performance, the readout circuit started playing an even more important role in the overall system noise level, linearity and dynamic range. Any error or unwanted effect on the readout circuit, will result in an output signal indistinguishable from the sensor output.

Capacitive readout circuits, in a broad way, consist of generating an output which is a function of the electrical charge that flows into the input. Usually, a voltage

output is generated, allowing this way, further processing with standard circuits like filters, amplifiers or data converters [3.5–3.7]. It is also common to convert the capacitance directly to the digital domain, also know as capacitance-to-digital converters (CDC) [3.8, 3.9]. Another alternative technique for the capacitance-to-voltage conversion (CVC) is provided by the capacitance-to-frequency conversion (CFC), where the sensing capacitance position information modulates the frequency of an output signal [3.10–3.12]. It can be implemented using an oscillator whose output frequency depends on the sensing capacitance. Additionally to these converters, the sigma-delta ($\Sigma\Delta$) electromechanical loop can also be used to implement readout circuits for capacitive sensors [3.13–3.15].

All the listed types of capacitance converters can be grouped into two major classes, namely the ones that work in the continuous time domain, generating a voltage value valid at any moment in time, and those that operate in the discrete time domain, with an output defined at a given sampling rate. An overview of the existing front-ends for capacitive MEMS sensors is presented in figure 3.1, with block diagrams of the typical implementation for each converter.

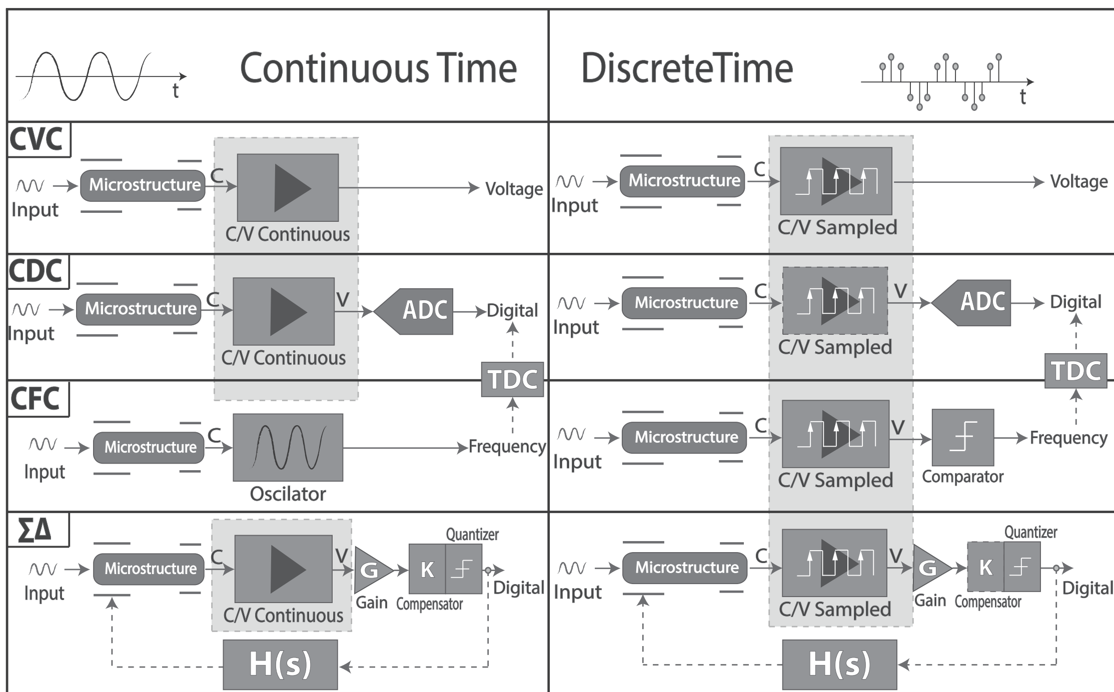


Figure 3.1: Capacitance converters generic architecture in the continuous and discrete time domains.

Considering that the transduction mechanism proposed for the realization of the sensor is the differential pull-in voltage, the sigma-delta electromechanical loop front-end is not a valid approach, therefore it is not addressed in this chapter. Since

the pull-in phenomenon can be detected in the analog domain, there is no need for any type of digitalization, ensuring the simplicity of the implementation (no analog-to-digital (ADC) or time-to-digital (TDC) converter is required). Given that, the focus of this chapter will be on the capacitance-to-voltage converters, either in the continuous or discrete time domain.

Before exploring the different conversion techniques, some general considerations about capacitance measurement are presented.

3.1 General Considerations

Previous to the analysis of the front-end electronics for capacitance measurement, let us understand how the MEMS device capacitance can be measured. To do so, a single capacitor MEMS device is used in this study.

The amount of charge, Q, stored inside the MEMS sensing capacitance, C_s, for a given excitation signal, V_{exc}, is a function of the electric capacitance as:

$$Q = C_s \times V_{exc} \quad [C]. \tag{3.1}$$

By definition, an electric current can be represented as the rate at which charge flows through a given surface. Given that, an electric current signal is generated upon variation on the charge in the sensing capacitance, $I_s = \frac{dQ}{dt}$ (figure 3.2).

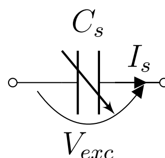


Figure 3.2: Capacitance measurement model.

According to equation (3.1), this charge variation can occur either due to a capacitance change, $\frac{dC_s}{dt}$, or as a result of a variation in the excitation voltage, $\frac{dV_{exc}}{dt}$. If a time independent (DC) V_{exc} is used, the generated current signal will be proportional to the capacitance variation as:

$$I_s = \frac{dQ}{dt} = V_{exc} \times \frac{dC_s}{dt}. \tag{3.2}$$

Regardless of the parasitic force inside the MEMS structure, caused by the DC excitation signal (will be addressed latter in this chapter), if the device is sensing a DC signal (i.e. inclination), according to equation (3.2), no output current will be generated. That is the reason why capacitive MEMS inertial sensors, need to be, invariably, AC (alternating current) coupled. The current signal can thus be written as:

$$I_s = \frac{dQ}{dt} = \frac{d(V_{exc} \times C_s)}{dt}. \tag{3.3}$$

It means that, the amplitude of the AC excitation voltage is modified by the sensor's capacitance, resulting in an output current signal similar to an amplitude modulation (AM). It is then important to figure out how the excitation signal specifications, namely frequency and amplitude, can bring about undesired effects on the measurement process.

3.1.1 Coupling Signal Amplitude

Ideally, the excitation signal would not produce any residual electrostatic force in the MEMS device through the sensing electrodes. Nevertheless, it is unavoidable. The generated parasitic electrostatic force, through the sensing electrodes, can be calculated using:

$$F_{elect} = \frac{1}{2} \frac{C_s}{{d_0}^2} V^2, \tag{3.4}$$

where C_s is the sensor's sensing capacitance, d_0 the initial gap and V the applied voltage. Conforming to (equation (3.4)), the electrostatic force is proportional to the square of the applied voltage. In the case that an AC signal ($V_0\ sin(\omega t)$) is applied to the sensing electrodes, the electrostatic force can be expressed as:

$$F_{elect} = \frac{1}{2} \frac{C_s}{{d_0}^2} \Big(V_0\ sin(\omega t)\Big)^2, \tag{3.5}$$

where:

$$\Big(V_0\ sin(\omega t)\Big)^2 = -\frac{1}{2} \Big[(V_0\ cos(2\omega t) - V_0\Big] = \frac{V_0}{2} - \frac{V_0}{2}\ cos(2\omega t). \tag{3.6}$$

The resultant force can be divided in two different electrostatic elements, a frequency dependent (AC):

$$F_{elect} = -\frac{1}{2}\frac{C_0}{{d_0}^2}\frac{V_0}{2}\, cos(2\omega t), \tag{3.7}$$

and a frequency independent (DC):

$$F_{elect} = \frac{1}{2}\frac{C_0}{{d_0}^2}\frac{V_0}{2}. \tag{3.8}$$

The electrostatic force, generated by the excitation signal, shows a dependence on the device capacitance and initial gap, as well as on the coupling signal amplitude and frequency. Disregarding the frequency of the excitation signal (will be addressed in the next subsection), the parasitic electrostatic force (DC component) can be minimized by using a low amplitude coupling signal, without overlooking the required signal to noise ratio (SNR).

Recalling that, in this study, the pull-in voltage is used as the transduction mechanism and the structure is continuously actuated up to the pull-in point, this residual electrostatic force has an effect in the pull-in voltage, as the total electrostatic force acting on the device becomes:

$$F_{electrostatic} = F_{actuation} + F_{sensing}, \tag{3.9}$$

where $F_{actuation}$ is the electrostatic force at the actuation electrodes (generated by the actuation voltage) and $F_{sensing}$ is the electrostatic force at the sensing electrodes (generated by the excitation signal).

Let's then analyse the coupling signal effect at the pull-in point (1/3 of the initial gap). Assuming that a constant excitation signal amplitude is used ($V_0 = Cnt$) and the device is not tilted ($displacement = 0$), according to equation (3.9), the additional electrostatic force in the sensing electrodes ($F_{sensing}$) reduces the actuation electrostatic force ($F_{actuation}$) needed to reach the pull-in. It is translated into a negative offset in the measured pull-in voltage. Since, in these conditions, the excitation signal effect will always be constant, no additional noise will be added to the pull-in voltage measurement. The optimal sensing signal amplitude, is the result of a trade-off between the pull-in voltage offset and the charge to

current ratio. As an example, if the MEMS device pull-in voltage is larger than $4V$ and an excitation signal with an amplitude of $100mV$ is used, the generated sensing electrostatic force at the pull-in point is less than 0.5% of the actuation electrostatic force, therefore can be neglected.

The tilting of the sensor will change the initial gap, d_0, the capacitance, C_0, and consequently the pull-in voltage of the sensor. This variation will modify the impact of the sensing electrostatic force in the device, due to the non-linear relation between the electrostatic force and the pull-in voltage. The outcome of this variation is the intensification of the sensor's non-linearity.

3.1.2 Coupling Signal Frequency

Up to this point, the coupling signal effect has been studied without taking care of the frequency effect, which means just considering the DC component (equation (3.8)). When starting to look at the frequency dependent electrostatic force, or AC component (equation (3.7)), it is relevant to understand that, the coupling signal frequency will place some constraints to the front-end electronics, namely the gain-bandwidth-product, the required area or the power consumption.

Due to the structure dynamics, if the excitation signal frequency is much higher than the MEMS natural frequency, the mechanical structure will not react to its AC component. To understand that, a typical frequency response of a parallel-plate MEMS device is shown in figure 3.3.

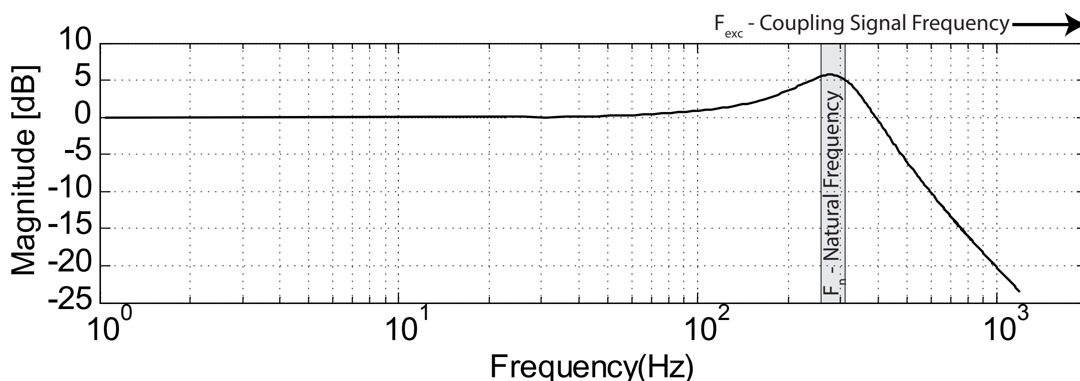


Figure 3.3: Typical frequency response of a capacitive parallel-plate MEMS device.

In order to prevent any undesired oscillation at the excitation frequency, a lower limit for this coupling signal can be defined. Looking at the the bode plot present

in figure 3.3, this limit can be defined as at least ten times higher than the mechanical bandwidth of the MEMS device (typically smaller than 5kHz), resulting in a minimum attenuation of $20dB$.

An other aspect that is important, when studying the optimal excitation frequency, is the capacitor impedance dependency on frequency:

$$Z = \frac{1}{j\omega C}. \tag{3.10}$$

The decreasing of the capacitor impedance with frequency implies that, higher frequency signal results in a higher current per voltage relationship. The output current of a AC coupled non-varying capacitor can be expressed as:

$$I = C\frac{dV}{dt} = -\omega C V_0 sin(\omega t), \tag{3.11}$$

where the input AC signal is equal to $V_0 cos(\omega t)$. In figure 3.4, the wave forms of the input voltage signal and the output current are depicted, showing that the maximum output current is equal to $\omega C V_0$ when $sin(\omega t) = -1$.

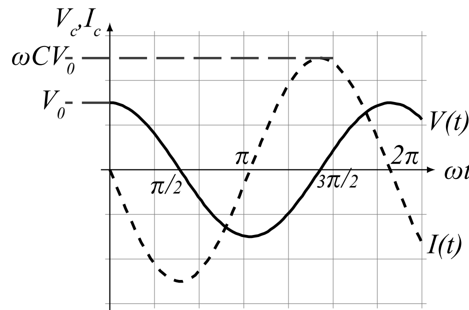


Figure 3.4: Input voltage and output current wave forms.

This maximization of the sensor's output current with the excitation frequency will lower the flicker noise level ($1/f$) (typically sufficiently low at roughly 100 kHz [3.16]), as well as improve the signal to noise ratio. Besides that, smaller RC time constants for the continuous time circuits are allowed, reducing the chip area.

3.1.3 Device and Coupling Parameters

To be comparable, the foregoing analyses of capacitive MEMS readout circuits architectures need to be performed using the same device parameters, along with the same coupling signal specification.

In virtue of limiting the front-end electronics complexity and power consumption, the excitation voltage source parameters used in this theoretical analysis are presented in table 3.1.

Table 3.1: Coupling signal parameters.

Signal	**Frequency**	**Amplitude**
V_{exc}	1MHz	$100mV$

In what concerns the MEMS device parameters, for this chapter study, the specifications that need to be established are the sensing capacitance and the capacitance change. The reference values were chosen based on a typical parallel-plate MEMS device [3.17] and the parameters are presented in table 3.2. The bi-directional displacement is limited by the mechanical stoppers located at $0.25\mu m$ from each fixed electrode.

Table 3.2: MEMS device parameters: sensing electrodes.

Displacement	**Rest**$(2.25\mu m)$	**Minimum**$(0.25\mu m)$	**Maximum**$(4.25\mu m)$
C_{left}	$4.525pF$	$40.728pF$	$2.396pF$
C_{right}	$4.525pF$	$2.396pF$	$40.728pF$

3.1.4 Differential Capacitors - Modulation Configurations

In the case of a differential capacitor structure, as the one presented in this work, also know as half-bridge configuration [3.7], there are two ways to performing the capacitance modulation. Either a single-ended carrier is used to excite the middle electrode, resulting in a differential capacitance measurement from the outer electrodes (figure 3.5a), or a differential carrier is used to excite the outer electrodes, producing a single-ended output from the middle electrode (figure 3.5b).

Both modulation techniques, presented in figure 3.5, will be analysed in the continuous and discrete domains.

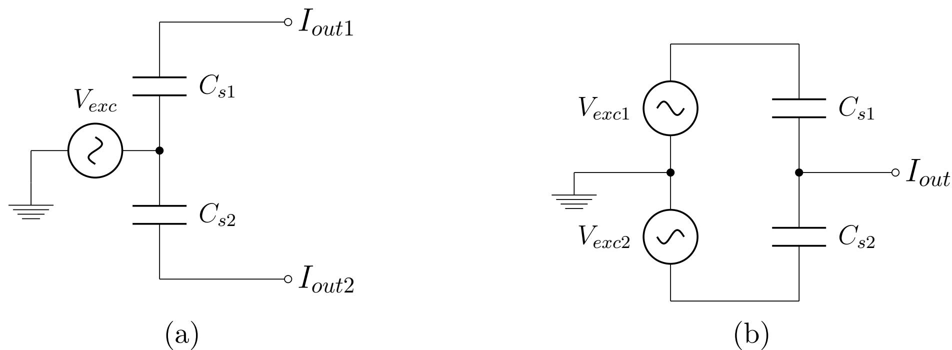


Figure 3.5: Differential capacitor modulation: a)Exciting the middle electrodes; b)Exciting the outer electrodes.

3.1.5 Parasitic Capacitance

In order to understand which readout architecture suits better the system requirements, it is important to realize that, in addition to the capacitive sensor itself, parasitic capacitances can be found in the fabricated devices.

Even though the devices used in the realization of the sensor have a differential capacitor configuration, the study of the parasitic effects will be done by analysing each sensing capacitor at a time. In the diagram of figure 3.6, one of the sensing capacitors is represented, C_s, coupled by the AC excitation signal, V_{exc}, as well as the different parasitic capacitors present in the device.

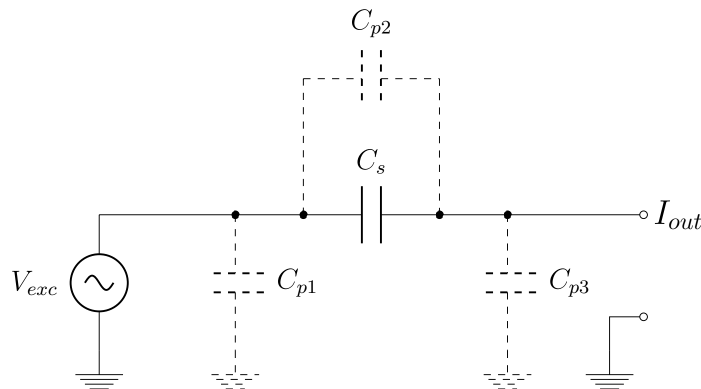


Figure 3.6: Single sensing capacitor, including parasitic capacitors.

Let us look at each parasitic capacitance in the MEMS device individually.

The only way to avoid the undesired effects caused by the parasitic capacitor C_{p1} is by using a load insensitive excitation source, which means, using a voltage coupling signal. On the other hand, to be insensitive to parasitic capacitance C_{p3}, a fixed DC voltage needs to be kept at the output node, only managed by using a current

output signal. The parasitic capacitor C_{p2}, which is in parallel with the sensor capacitor, can not be overlooked in this single capacitor analyses and will lead to an offset in the output current signal.

Since while the AC voltage excitation signal, the parasitic capacitors C_{p1} and C_{p3} can be neglected, the foregoing analyses is reduced to the parasitic capacitor in parallel with the sensor (C_{p2}).

Even if the differential capacitance architecture of the MEMS device, in theory, can compensate the sensing output current for the parasitic capacitor C_{p2}, this capacitance will be used in the circuit analysis. For the sake of simplicity, from now on, the parasitic capacitor related to sensing capacitor C_{s1} will be named as C_{p1}, while the parasitic capacitor related to sensing capacitor C_{s2} will be labeled as C_{p2}.

3.2 Continuous Time

Continuous-time front-ends are characterized by the continuous output voltage, proportional to the sensing capacitance. Usually, these front-ends are divided into two subgroups, those that work at the resonance frequency of the micro-mechanical element and those that modulate the signal to a higher frequency.

Performing the continuous-time readout at the resonance frequency of the sensor element leads to certain design and performance limitations [3.5]. Firstly, large time constants are needed to avoid attenuation, large biasing resistors are required, increasing the flicker ($1/f$) noise inflicted by all the active components. Most of these effects can be reduced if the output signal is modulated to a frequency higher than the mechanical resonance frequency (section 3.1.2). Those are the reasons why the resonance frequency operation is out of the scope of this thesis, therefore only the higher frequency modulation will be studied.

3.2.1 Dual Source, Single Readout

The first differential approach to be analysed is a single output configuration where two AC voltage sources, with a phase shift of 180°, are required. The schematic of this configuration is depicted in figure 3.7.

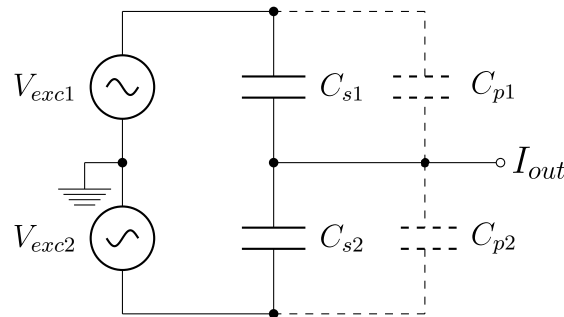


Figure 3.7: Differential configuration: dual source, single output.

In this capacitors configuration, when both sensing capacitors (C_{s1} and C_{s2}) have the save value, the resultant output current should be zero. Since the parasitic capacitor C_{p1} and C_{p2} are in parallel with each sensing capacitor (figure 3.7), if both parasitic capacitors have the same value, they will cancel each other, adding no offset to the output current. Since we can not assume that the parasitic values are equal for both sides, or that they stay always the same, they can not be ignored.

At this point, a drawback of this approach can already be found. The need of two different voltage sources reveals that, any mismatch in the voltage amplitude, frequency or phase will result in an output signal indistinguishable from the sensor signal. Every change in the sensor's output capacitance will represent a variation on the output current I_{out}.

Amplification stage

In the previous sections it was shown how to convert the sensor's capacitance into current, by means of a excitation signal. Now, we need to find out how to convert this electric current into a voltage signal that is proportional to the capacitor value. In electronics design, the most common current to voltage converter is the transimpedance amplifier (TIA), usually implemented using an operational amplifier (figure 3.8), where the input current signal, I_{in}, is converted into voltage, V_{out}, through the feedback impedance Z_{fb}.

Knowing that the generated electric current corresponds to the charge variation in the sensing capacitor (electric current is the time differential of charge), the amount of charge transferred during a given period can be calculated by integrating the current:

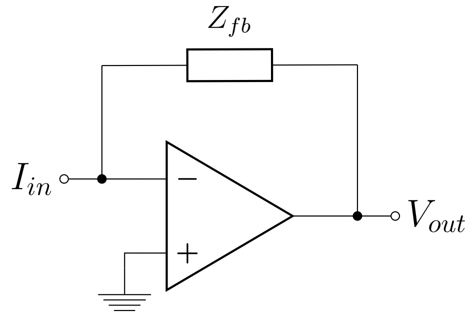


Figure 3.8: Typical transimpedance amplifier.

$$i = \frac{dQ}{dt} \Leftrightarrow Q = \int idt. \tag{3.12}$$

In the electronic domain, this means that the transimpedance amplifier needs to work as a current integrator, where an output voltage proportional to the integrated value of the input current is produced. This configuration is also known as charge amplifier and the basic schematic is shown in figure 3.9.

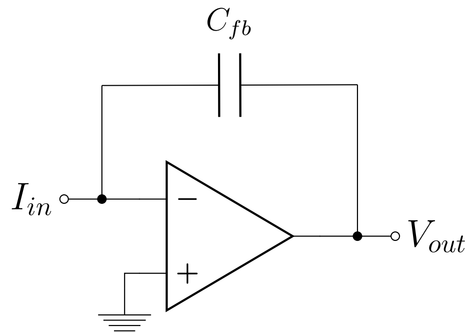


Figure 3.9: Charge amplifier basic configuration.

The grounded non-inverting input of the amplifier forces the voltage in the inverting input to be zero, creating what can be called as a "virtual ground". In the charge amplifier configuration, this balance in the input differential pair is achieved by charging the feedback capacitor, C_{fb}, with charge injected through negative input. Basically, the working principle of the charge amplifier can be described as a charge to voltage converter, where the output voltage is explained by the definition of capacitance:

$$C = \frac{Q}{V} \Leftrightarrow V_{out} = \frac{Q_{fb}}{C_{fb}}, \tag{3.13}$$

where Q_{fb} is the charge that flows through the input and is integrated in the

feedback capacitor C_{fb}. A charge amplifier sensing a capacitive sensor expressed as C_s, is shown in figure 3.10.

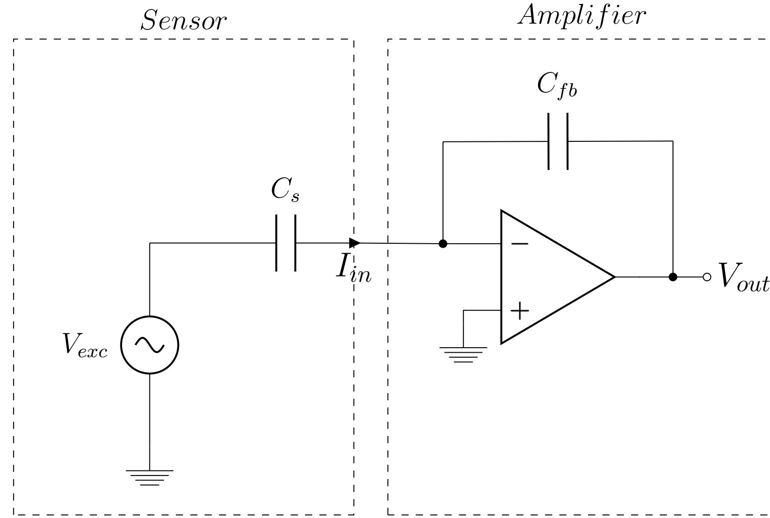


Figure 3.10: Charge amplifier sensing a capacitive sensor.

The capacitance value of C_s is sensed by measuring the charge, Q_{C_s}, that it stores for a given input voltage, V_{exc}: $Q_{C_s} = V_{exc} \times C_s$. The charge variation in C_s will generate a current, I_{in}, which in turn will be integrated by the charge amplifier. Ideally, the charge in the feedback capacitor ($Q_{C_{fb}}$) can be assumed to be equal to the charge in the sensor (Q_{C_s}) ($Q_{C_s} = Q_{C_{fb}}$).

According to equation (3.13), the charge amplifier output expression can be written in terms of the sensor's capacitance value as:

$$V_{out} = \frac{C_s}{C_{fb}} V_{exc} \qquad [V]. \tag{3.14}$$

Regarding the charge amplifier configuration depicted in figure 3.9, the amplifier bias current will act as an additional source of charge, what would result in the saturation of the amplifier at one of the power rails. To solve that, a resistor is connected in parallel with the feedback capacitor, resulting in the circuit presented in figure 3.11.

The feedback resistor R_{fb} will lower the discharging rate of C_{fb} by providing a path to the bias current of the amplifier, avoiding this way the amplifier from drifting to saturation. Nonetheless, the addition of the feedback resistor will change the frequency response of the amplifier, by creating a pole defined by:

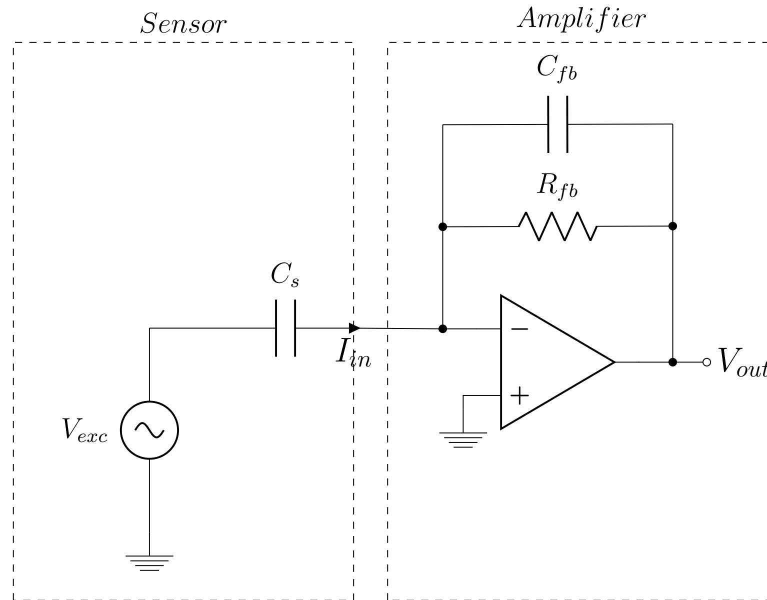


Figure 3.11: Compensated charge amplifier sensing a capacitive sensor.

$$f_{pole} = \frac{1}{2\pi R_{fb} C_{fb}} \qquad [Hz]. \tag{3.15}$$

The typical charge amplifier frequency response, shown in figure 3.12, demonstrates that the low cutoff frequency needs to be calculated, in order to avoid the attenuation of the signal. This is accomplished by moving the feedback pole to a much lower frequency than the coupling signal.

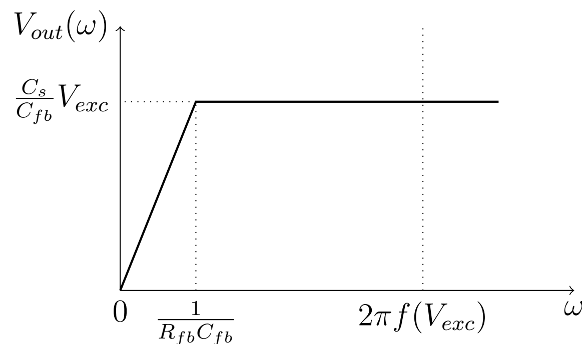


Figure 3.12: Charge amplifier frequency response.

Lets consider now the differential sensing capacitor when using the dual source, single output charge amplifier topology.

While switching from single capacitor sensor (used for exemplification), to the differential capacitor, matter of study, a non-zero parasitic capacitance in parallel

with the differential sensing capacitor needs to be taken into account (figure 3.13).

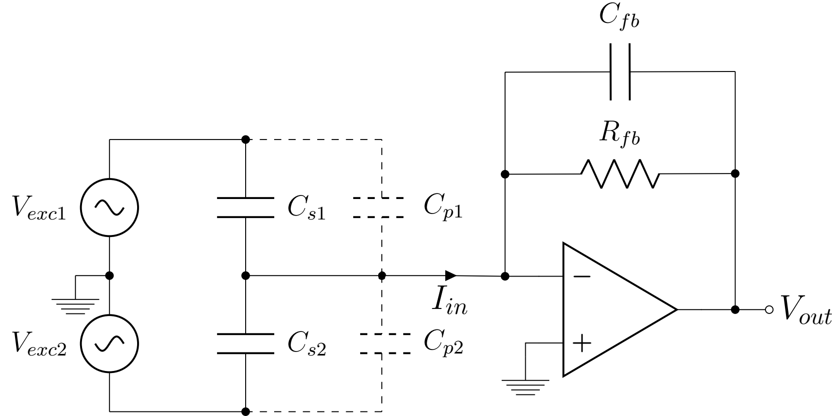


Figure 3.13: Charge amplifier sensing a differential capacitive sensor (dual source, single output).

If both parasitic capacitances have the same value ($C_{p1} = C_{p2}$), they will cancel each other, adding no extra charge to the amplifier. However, any slight change in the current path, or in the device fabrication process can change the parasitic capacitance and consequently changing the output. The charge amplifier output voltage, for this differential approach, becomes then:

$$V_{out} = -\frac{C_{s1} + C_{p1}}{C_{fb}} V_{exc1} + \frac{C_{s2} + C_{p2}}{C_{fb}} V_{exc2}. \tag{3.16}$$

Simulated Results

A Simulink model of the charge amplifier based architecture was created, in order to validate the proposed approach. For this model, the parameters of the capacitive sensor (sensing capacitors) presented in table 3.2, as well as the excitation signal (table 3.1) were considered. Assuming that a maximum output voltage of 1.5V is required (maximum capacitance change) and the parasitic capacitance is $100fF$, the feedback capacitor calculated using equation (3.16) becomes equal to:

$$C_{fb} = \frac{|-(40.728pF + 100fF)100mV + (2.396pF + 100fF)100mV|}{|1.5V|} = 2.56pF. \tag{3.17}$$

Now, regarding the 1MHz coupling signal, it is crucial that the feedback pole frequency (equation (3.15)) is at least one decade smaller ($f_{pole} \leq$ 100kHz). Given

that, the feedback resistor minimum value can be found using:

$$f_{pole} \leq 100kHz \Leftrightarrow \frac{1}{2\pi C_{fb} R_{fb}} \leq 100kHz \Leftrightarrow R_{fb} \geq 621.7k\Omega. \quad (3.18)$$

The feedback resistor (R_{fb}), calculated in equation (3.18), is considerably large for integration and, if needed, should be reduced by decreasing the charge amplifier gain (increasing the feedback capacitor). Since the main purpose of this chapter is to understand the basic principles of different readout topologies, without getting into much detail, the $621.7k\Omega$ feedback resistor will be assumed as reasonable and will be used in the next simulations.

According to the feedback capacitor calculation (equation (3.17)), the circuit should have a maximum output voltage amplitude of $1.5V$ at the maximum displacement point, that happens, when one of the sensing capacitors (C_{s1} or C_{s2}) is at is maximum value ($40.728pF$), while the other has the minimum capacitance value ($2.396pF$). This corner situation was simulated and the results are shown in figure 3.14. The charge amplifier simulated voltage output amplitude, when the sensing capacitors difference is maximized, shows that the desired gain was achieved ($23.52dB$).

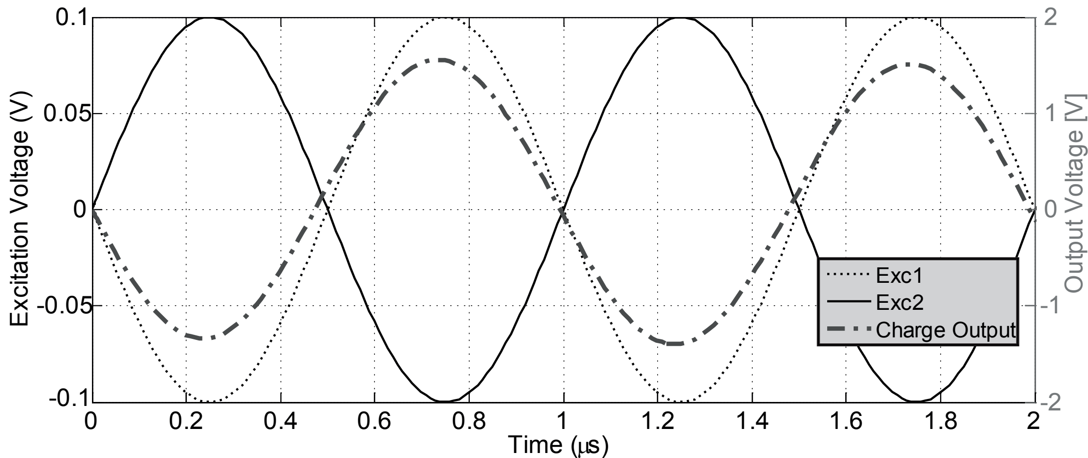


Figure 3.14: Charge amplifier maximum output voltage, using $C_{s2} = 40.728pF$ and $C_{s1} = 2.396pF$.

A frequency analysis was performed to the circuit model and the resulting bod plot is presented in figure 3.15.

In accordance with the calculation, the low frequency pole, formed by the feedback impedance, is located one decade before the excitation signal frequency (100kHz).

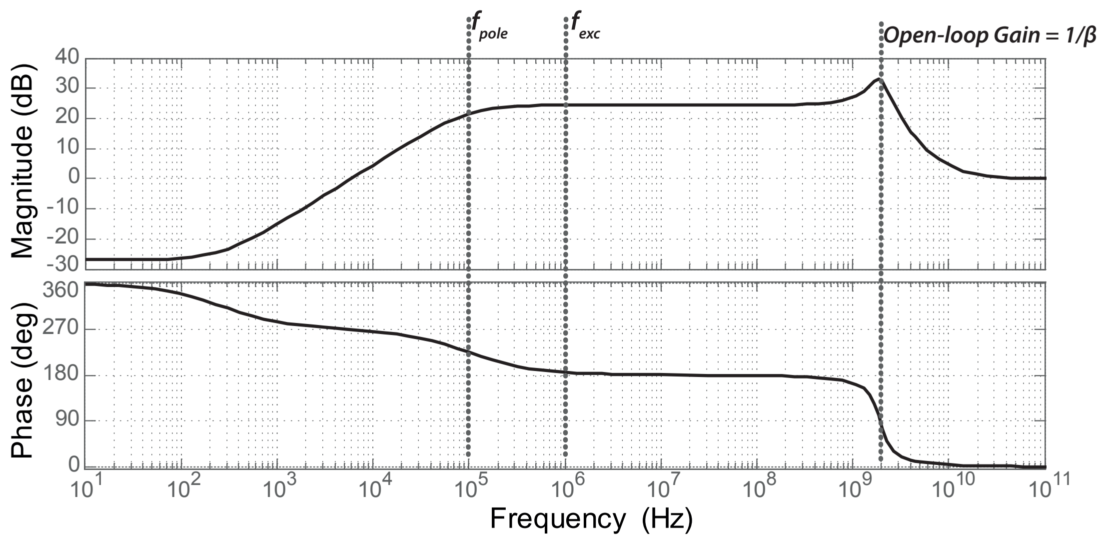


Figure 3.15: Bode plot of the charge amplifier.

At the oscillation frequency, a phase shift lower than 2 degrees is observed, what is perfectly acceptable. Around 1GHz, an amplitude peak can be seen, which is the result of the interception of the first order pole from the feedback factor ($1/\beta$) with the first order zero from the operational amplifier open loop gain. At this frequency, oscillation might occur and if undesired effects result from that, a compensation can be added by creating a zero at a lower frequency (<1GHz), in order to limit this high frequency response to a suitable range. In figure 3.16 a modification to the charge amplifier architecture is presented, where the high frequency zero is obtained by adding a resistor in series with the sensor's output capacitance.

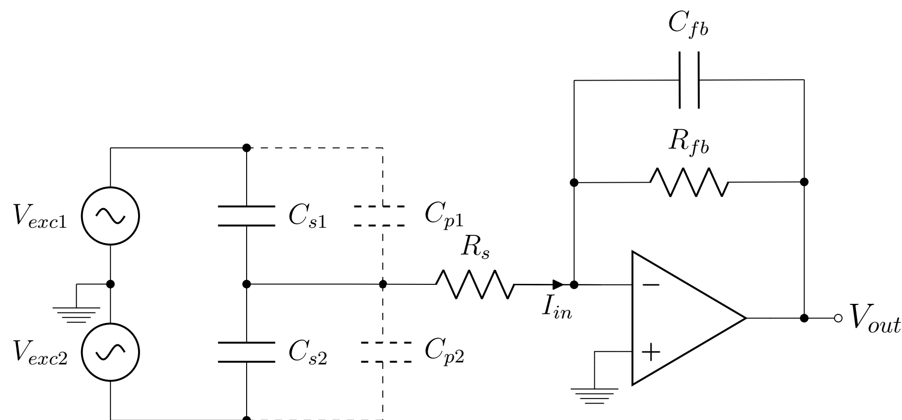


Figure 3.16: Proposed charge amplifier modification to limit high frequency response.

The $-3dB$ point of the high frequency zero, created by the series resistance R_s, is

defined by:

$$f_{zero} = \frac{1}{2\pi C_s R_s} \qquad [Hz]. \tag{3.19}$$

It should be kept in mind that, this compensation zero frequency will change with the sensing capacitor variation (C_s). A frequency range for the zero needs to be defined when calculating R_s. Looking at equation (3.19), the highest frequency of the zero will be when the sensing capacitor is at its minimum, which means, at the rest position, while the lowest frequency will be when the capacitance is maximum (at pull-in point). Based on that, the resistor value can be calculated in a way that the maximum frequency of the zero is at least one decade before the peak frequency ($\leq 100MHz$), while the minimum frequency is at least one decade after the excitation frequency ($\geq 10MHz$). For this particular case, these constraints resulted in a 130Ω series resistor and the resultant frequency response is presented in figure 3.17.

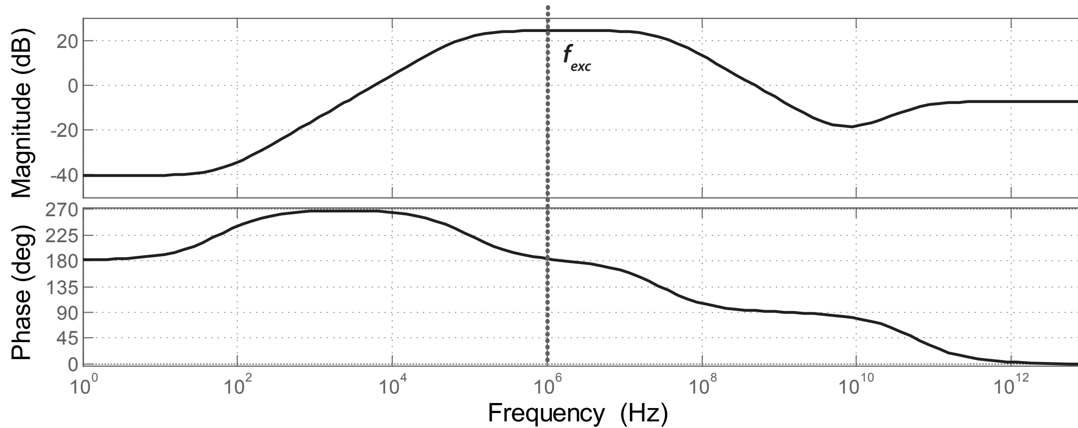


Figure 3.17: Bode plot of the charge amplifier with the compensation resistor ($C_{s2} = 40.728pF$ and $C_{s1} = 2.396pF$).

3.2.2 Single Source, Differential Readout

The differential sensing electrodes in the MEMS device creates the possibility of using a different continuous time readout configuration. This time, a single voltage source is used, generating a differential current output, as depicted in figure 3.18.

If both sensing capacitors have the same value ($C_{s1} = C_{s2}$), both output current signals will be equal as well ($I_{out1} = I_{out2}$), resulting in a zero differential output

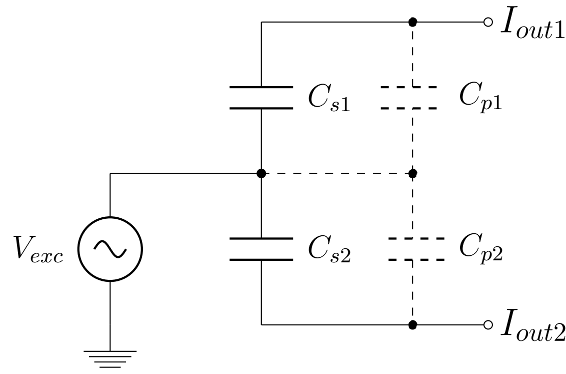


Figure 3.18: Differential topology: single source, differential readout.

($I_{out1} - I_{out2} = 0$). Assuming that parasitic capacitors C_{p1} and C_{p2} are identical, the additional charge injection due to the parasitic capacitance will be in the same proportion for both sides, resulting again in a differential output equal to zero. Since only one excitation signal is used for both sensing capacitors, any change or deviation in the voltage source signal will not have a direct effect in the output signal, in contrast with the dual source approach.

It is of common knowledge that, differential signals have the main advantage over single-ended as they are "immune" to environmental noise. Interfering electric signals, e.g. from power lines, will result in a common-mode signal corruption avoided by means of a differential operation. Therefore, this approach is expected to present better results using, when compared to the previously presented one (Dual source, singe output).

Amplification stage

Similarly to the previously presented readout topology, the amplification stage of this readout circuit is based on a current integrator transimpedance amplifier. Since the sensor's output current will be in a differential mode, a fully differential transimpedance amplifier is required (figure 3.19).

The working principle of the fully differential charge amplifier, or current integrator, is identical to the single-ended version presented in section 3.2.1. Firstly, like in the single output charge amplifier, the feedback impedance Z_{fb} should be composed by a resistor R_{fb} and a capacitor C_{fb} connected in parallel.

To minimize the parasitic electrostatic force, no DC voltage level should be applied to the MEMS sensing capacitors (section 3.1). It means that, the fully differential

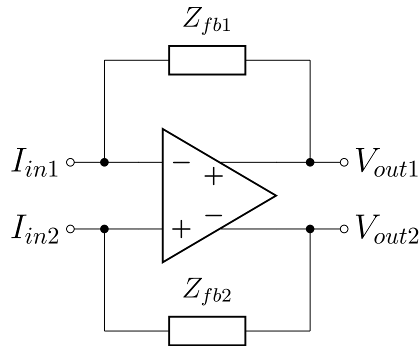


Figure 3.19: Fully differential transimpedance amplifier.

output common mode voltage, controlled by the reference input V_{cm}, needs to be grounded, obtaining a zero centered output differential signal. The fully differential charge amplifier schematic is shown in figure 3.20.

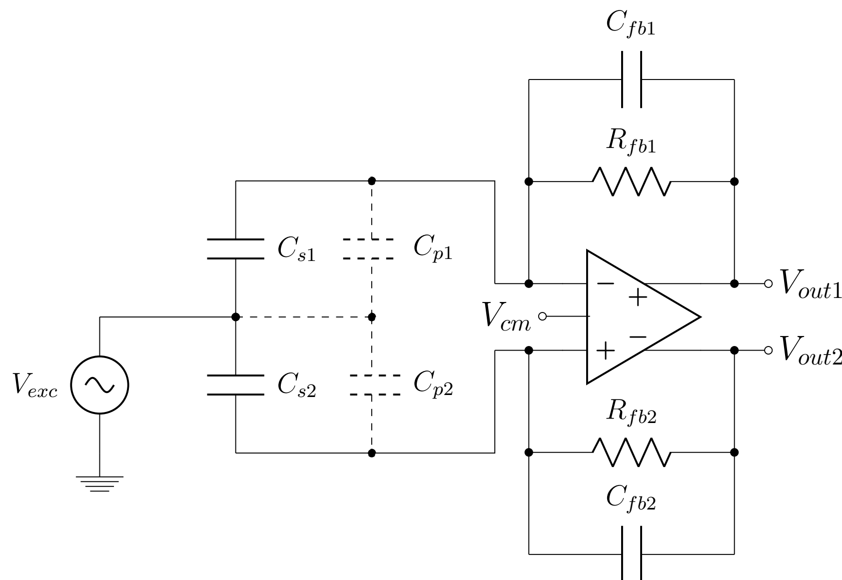


Figure 3.20: Fully differential charge amplifier.

In the single ended amplifier, the non-inverting input of the the operational amplifier is grounded, enabling the integration of the charge that flows through the inverting input in the feedback capacitor. The fully-differential approach presented in figure 3.20 does not secure the required ground at the amplifier inputs. It can be ensured by using a pull-down bias resistor (R_b) at each amplifier input (figure 3.21).

The differential charge amplifier output voltage, as in the single ended charge amplifier (equation (3.16)), is defined by the feedback capacitor (C_{fb1} and C_{fb2}). Considering that the noise from the signal routing or the power supply will be

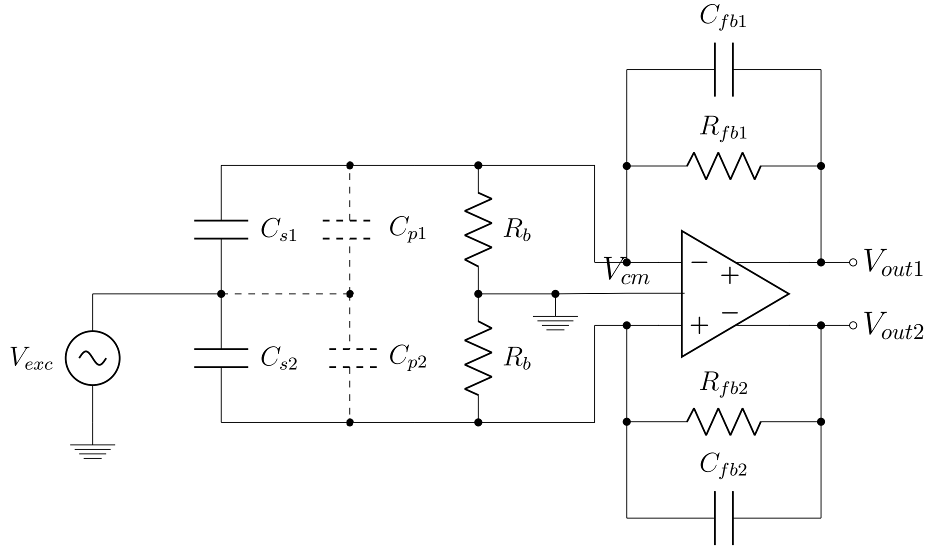


Figure 3.21: Fully differential charge amplifier with bias resistors.

materialized as a common mode voltage, by rejecting the common mode output voltage, the overall amplifier noise immunity level is increased. For that reason, the output of interest is reduced to the differential mode output voltage ($V_{out,DM}$), as:

$$V_{out,DM} = \Big(-\frac{C_{s1} + C_{p1}}{C_{fb1}} + \frac{C_{s2} + C_{p2}}{C_{fb2}} \Big) V_{exc}. \tag{3.20}$$

Simulation Results

Keeping the same device and excitation signal parameters (tables 3.1 and 3.2), a differential charge amplifier Simulink model was created. The new feedback impedance (R_{fb} and C_{fb}) values are now calculated using equation (3.20). Since the output signal is in differential mode, the maximum output voltage of the amplifier should be dimensioned as the maximum difference between the two single ended outputs, which means, for this simulation, a maximum differential voltage of $3V$. Assuming a parasitic capacitance of $100fF$, the feedback capacitor is determined as:

$$C_{fb} = \frac{|-(40.728pF + 100fF) + (2.396pF + 100fF)|}{\frac{|3V|}{100mV}} = 1.278pF, \tag{3.21}$$

where:

$$C_{fb} = C_{fb1} = C_{fb2}. \tag{3.22}$$

To achieve the desired feedback pole frequency, the new feedback resistor, R_{fb} (R_{fb}=R_{fb1}=R_{fb2}), is calculated:

$$f_{pole} \leq 100kHz \Leftrightarrow \frac{1}{2\pi C_{fb} R_{fb}} \leq 100kHz \Leftrightarrow R_{fb} \geq 1.245M\Omega. \tag{3.23}$$

The fully differential charge amplifier was simulated using the maximum capacitance difference ($C_{s1} = 40.728pF$, $C_{s2} = 2.396pF$). The $3V$ maximum differential output voltage was achieved (figure 3.22).

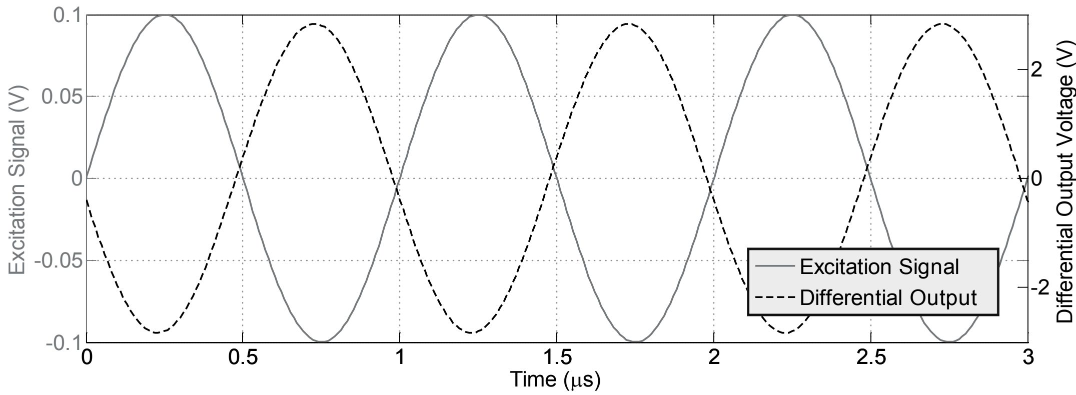


Figure 3.22: Output voltage of the fully differential charge amplifier [C_{s1} = 40.728pF and $C_{s2} = 2.396pF$].

The transient analyses of the proposed amplifier showed that the desired gain was achieved by adding the pull-down resistor in the inputs of the amplifier. In order to figure out the frequency behavior of the amplifier after adding these resistors, a linear analyses was performed and the resultant bode plot is shown in figure 3.23.

The low frequency response is limited by the feedback pole (< 1MHz), while the pull-down bias resistor creates a zero with the sensing capacitance ($F_{zero_bias} = \frac{1}{2\pi C_s R_b}$) (> 1MHz). The high frequency response of the amplifier can be limited by adding a resistor in seres with the sensing capacitor, as in the single-ended version, creating a zero at $F_{zero} = \frac{1}{2\pi C_s R_s}$. The resultant frequency response is presented in figure 3.24.

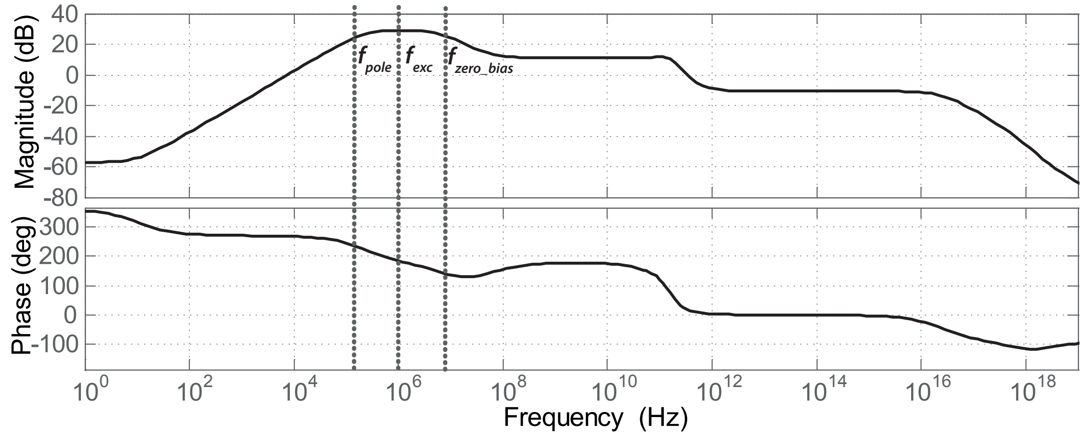


Figure 3.23: Fully differential charge amplifier bode plot ($C_{s1} = 40.728pF$, $C_{s2} = 2.396pF$).

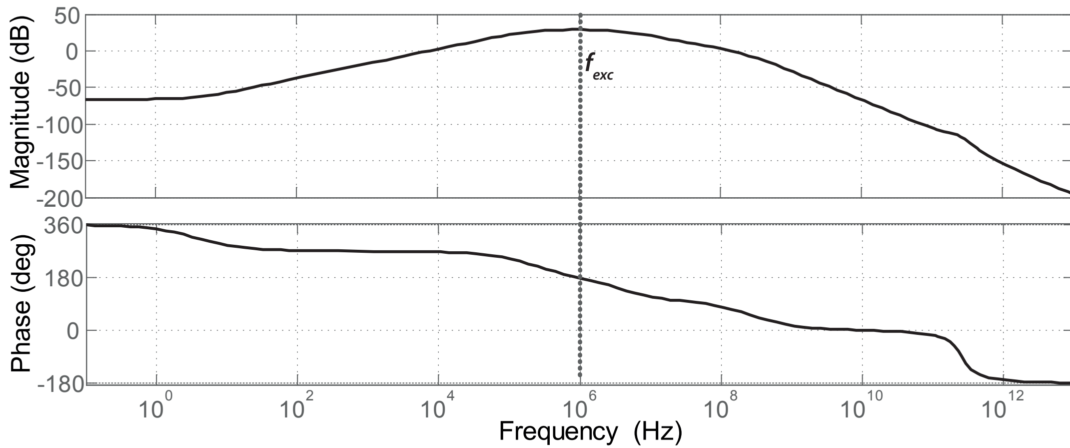


Figure 3.24: Bode plot of the fully differential charge amplifier compensated for high frequency ($C_{s1} = 40.728pF$, $C_{s2} = 2.396pF$).

3.2.3 Noise Contribution

Considering that ideally, the readout circuit total noise should be lower than the mechanical thermal noise of the MEMS structure, the charge amplifier noise contribution should be minimized. In this particular case (pull-in based), the readout noise is not as critical as in the direct transduction approaches, but it is important to understand the noise sources within the circuit.

The two major sources of noise in the charge amplifier are the feedback resistor and the input differential pair of the amplifier. The noise contribution through the feedback resistor is due to its thermal noise:

$$\overline{v_{n,R_fT}} = \sqrt{4k_BTR_{fb}} \qquad [V/\sqrt{Hz}], \tag{3.24}$$

where k_B is the Boltzmann constant and T is the temperature. The amplifier differential pair noise addition to the system, through the input transistor, can be divided in several noise types. The thermal noise, calculated using:

$$\overline{v_{n,IT}} = \sqrt{\frac{8}{3}\frac{k_BT}{gm}} \qquad [V/\sqrt{Hz}], \tag{3.25}$$

where gm is the transcondutance of the input mosfet. The flicker noise:

$$\overline{v_{n,IF}} = \sqrt{\frac{K}{C_{\text{ox}} \cdot WL}} \qquad [V/\sqrt{Hz}]. \tag{3.26}$$

being K the process-dependent constant, C_{ox} the oxide capacitance in mosfet devices, W and L the channel width and length respectively and lastly the shot noise due to the leakage current fluctuations that can be written as:

$$\overline{i_{n,IS}} = \sqrt{2qI_G} \qquad [A/\sqrt{Hz}], \tag{3.27}$$

where q is the electron elementary charge and I_G is the mosfet leakage current. The total noise contribution can be formulated as:

$$\overline{i_{(n,Total)}} = \overline{i_{(n,IS)}} + \frac{\overline{v_{(n,R_fT)}}}{R_f} + (\overline{v_{(n,IT)}} + \overline{v_{(n,IF)}})(1 + \frac{C_s}{C_{fb}}) \qquad [A/\sqrt{Hz}]. \tag{3.28}$$

3.2.4 Demodulation

When the sensor capacitance charge is modulated to a higher frequency, it also needs to be demodulated in order to retrieve the sensor information. The demodulation method is common to both excitation techniques, hence it is discussed in a generic way.

The capacitance modulation result can be analytically explained as the multiplication of the sensor input signal, $V_{in} = Asin(\omega_1 t + \phi_1)$, with the coupling signal, $V_{exc} = Bsin(\omega_2 t + \phi_2)$:

$$V_{in} \times V_{exc} = A \times B[sin(\omega_1 t + \phi_1) \times sin(\omega_2 t + \phi_2)]. \tag{3.29}$$

From the trigonometry laws, it is known that $sin\alpha \times sin\beta = -\frac{1}{2}[cos(\alpha+\beta) - cos(\alpha-\beta)]$, which yields a modulated signal (V_{mod}) equal to:

$$V_{mod} = -\frac{AB}{2} \times \Big[cos\Big((\omega_1+\omega_2)t+(\phi_1+\phi_2)\Big) - cos\Big((\omega_1-\omega_2)t-(\phi_1-\phi_2)\Big)\Big]. \tag{3.30}$$

Considering a $700mV$ input signal at a 50kHz frequency, to emulate the sensor input, and a $1V$/1MHz coupling signal, the resultant charge amplifier double-side output signal is depicted in figure 3.25, which is in accordance with equation (3.30).

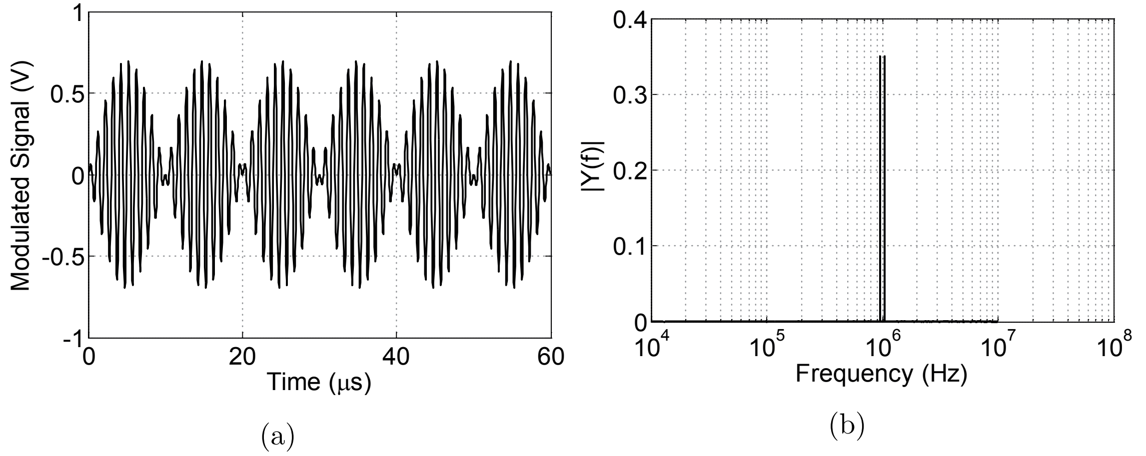
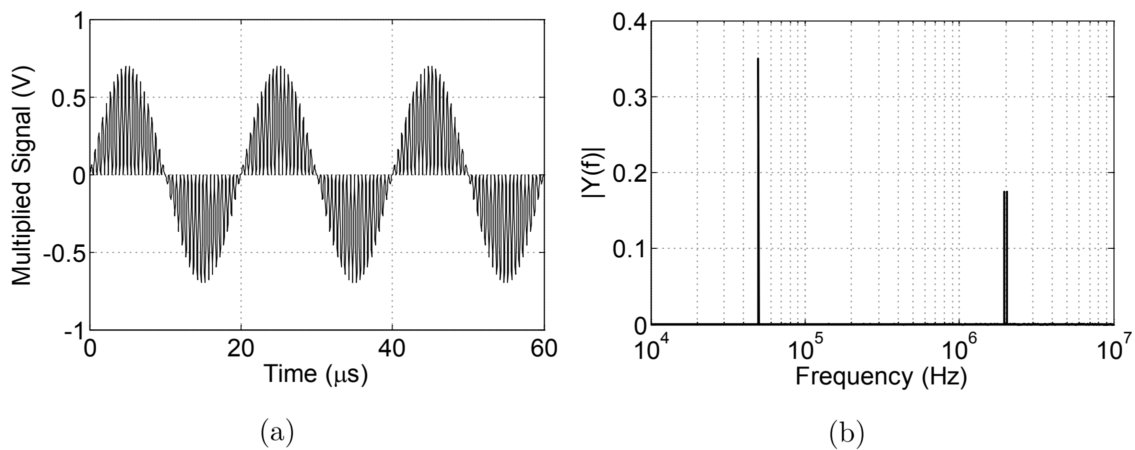


Figure 3.25: Input signal (50kHz) modulated with a 1MHz coupling signal: a)Modulated signal amplitude; b)Modulated signal FFT.

If the modulated signal, V_{mod}, is multiplied with the same coupling signal ($V_{mod} \times V_{exc} = V_{mod} \times Bsin(\omega_2 t + \phi_2)$), the double-side signal central frequency is doubled ($2\omega_2$) and a component at the input signal frequency is generated (figure 3.26):

$$\begin{gathered} V_{demod} = \frac{1}{4} \times \Big[- AB^2 sin\Big((\omega_1 - 2\omega_2)t + (\phi_1 - 2\phi_2)\Big) \\ -AB^2 sin\Big((\omega_1 + 2\omega_2)t + (\phi_1 + 2\phi_2)\Big) + 2AB^2 sin\Big((\omega_1)t + (\phi_1)\Big)\Big]. \end{gathered} \tag{3.31}$$

The signal of interest can then be obtained by filtering the high frequency components. Summarizing, a continuous-time front-end, in addition to the charge



(a) (b)

Figure 3.26: Result of the modulated signal multiplication with the 1MHz coupling signal: a)Multiplied signal amplitude; b)Multiplied signal FFT.

sensitive amplification circuit, requires a demodulation stage to retrieve the sensor information. The elements of a generic CVC are presented in the block diagram of figure 3.27.

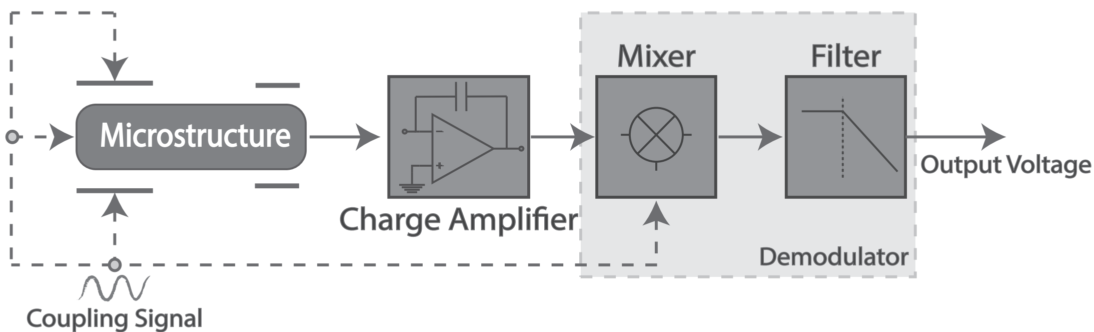


Figure 3.27: Block diagram of the generic continuous time C/V converter.

3.3 Discrete Time

In the case of inertial sensors, the signal of interest is always a continuous time signal, such as acceleration or inclination. The measurable capacitance, which is proportional to the signal of interest, is also a continuous time signal. So, when the capacitance is measured using a sampling readout circuit (discrete time), the continuous time information is mapped in a band defined by the Nyquist frequency [3.18], setting the theoretical maximum bandwidth of the readout. The noise and high frequency components of these circuits need to be studied in order

to avoid the corruption of the sensing signal band.

Sampled-data circuits are widely used as a way to overcome some of the continuous-time circuits drawbacks. When aiming for high voltage gain amplifiers, in CMOS technology, the open-loop output resistance needs to be maximized, approaching hundreds of kilo-ohms. This degrades the precision of the circuit when used as a continuous time feedback amplifier and adds thermal noise to the signal of interest.

In the particular case of the charge amplifier (section 3.3), both of the configurations require a very large feedback resistor, used to provide the amplifier bias current without affecting the AC behavior in the frequency band of interest. Some times, these feedback resistors become prohibitively large for integration, increasing the need to investigate other biasing methods for these capacitive feedback circuits, namely discrete time methods.

3.3.1 Switched Capacitor Amplifier

A widely biasing method is the switched capacitor amplifier. Switched capacitor circuits are extensively used in analog signal processing circuits and is one of the most used architectures for capacitive sensing due to its accurate frequency response as well as good linearity and dynamic range.

Considering the simple switched capacitor schematic depicted in figure 3.28, three different switches will control the amplifier operation. The input voltage, applied to the left plate of the sensing capacitor, is controlled by S_1 and S_3, which switches between V_{in} and the ground, while the unity-gain feedback is provided by S_2.

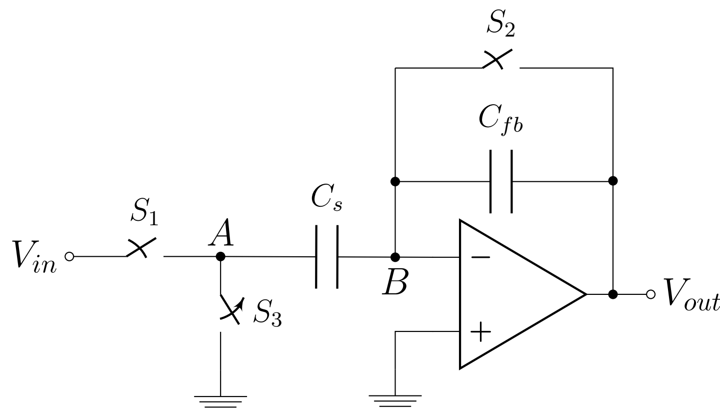


Figure 3.28: Schematic of a switched capacitor amplifier.

The working principle of the switched capacitor amplifier can be divided in two

phases, the sampling phase and the amplification phase. In the sampling phase, S_1 and S_2 are ON while S_3 is OFF (figure 3.29a). In this mode, a virtual ground is created at point B, leading to a zero output ($V_B \approx V_{out} \approx 0$), while the voltage across the sensing capacitor is equal to the input voltage ($V_s = V_{in}$). On the other hand, in the amplification stage S_1 and S_3 are OFF and S_2 is ON, connecting the left plate of the sensing capacitor to the ground ($V_A = 0$) (figure 3.29b). During this phase, the charge stored in C_s during the sampling phase (the amount of charge stored is equal to $V_{in}C_s$) will be transferred to the feedback capacitor, resulting in an output voltage equal to:

$$V_{out} = -V_{in}\frac{C_s}{C_{fb}}. \tag{3.32}$$

The switches in the amplifier are controlled by two non-overlapping clock signals, ϕ_1 and ϕ_2, swapping this way between the sample and the amplify mode (figure 3.29c).

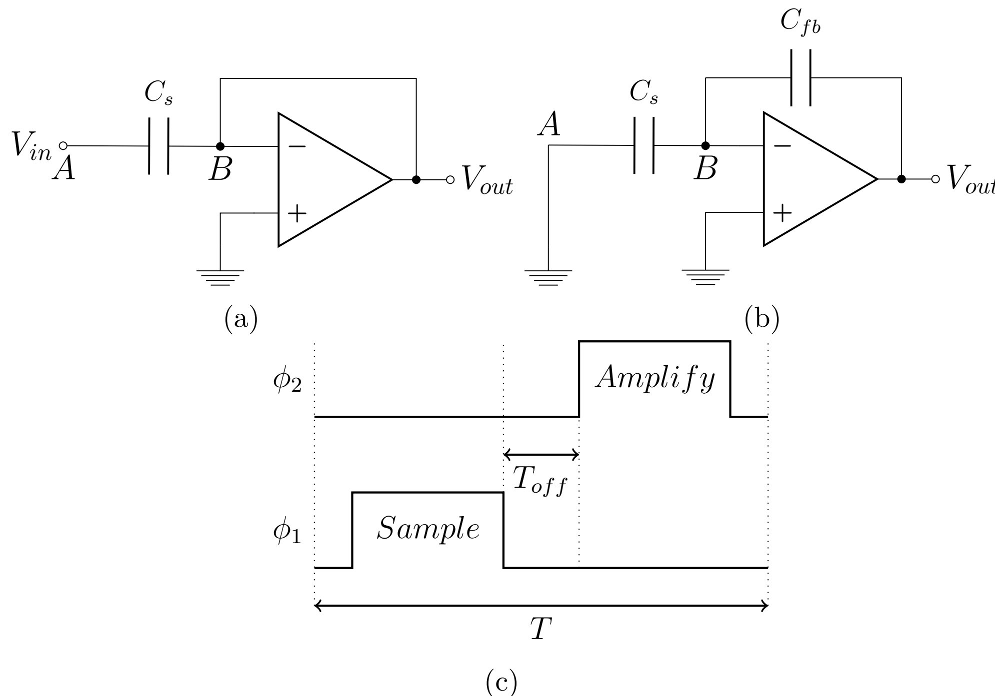


Figure 3.29: Switched capacitor equivalent circuit: a)Sampling phase; b)Amplification phase; c)One period of the non-overlapping clocks.

In the circuit of figure 3.28, when the amplifier is switching from the sample to the amplify mode, an input-dependent charge injection or charge loss can occur. To avoid that, a proper timing for the control clock signals need to be used, namely,

turning S_2 OFF before S_1. After turning S_2 OFF, the total charge at point B remains constant and equal to $-V_{in}C_s$, making the circuit insensitive to the charge injection from $S1$. In the next phase, when A is connected to the ground (after the circuit is completely settled), the voltage across C_s is nearly zero, meaning that the total charge was transferred to C_{fb} (equation (3.32)). From the time where S_2 turns OFF until S_1 turns OFF too, the input voltage might change but no error will be introduced to the output voltage, because the sampling instant is defined by the turn OFF of S_2. Based on that, three different clock signal might be used for a proper switching timing as show in figure 3.30.

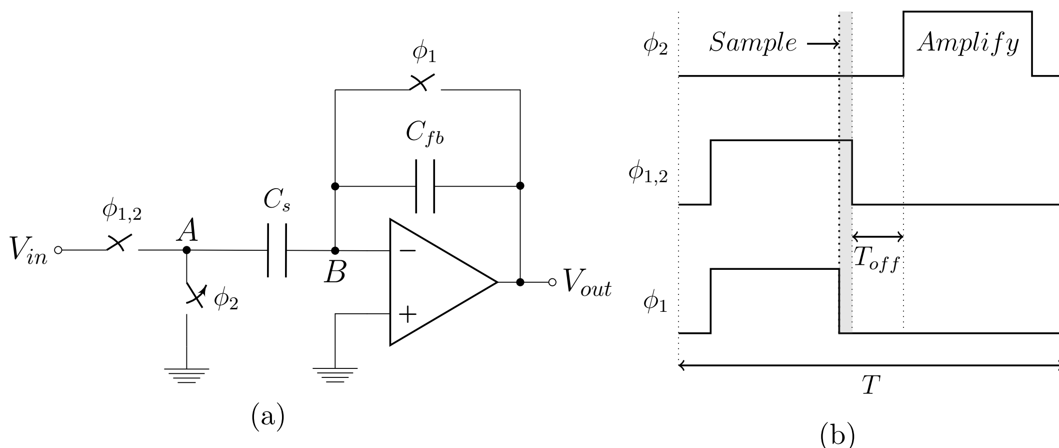


Figure 3.30: Switched capacitor avoiding parasitic charge injection: a)Schematic; b)Control clock signals.

Simulation Results

Aiming to cement the theoretical concepts, a Simulink model was used as a way to understand the effects of a $-200mV$ input signal in a fixed sensing capacitor ($C_s = 5pF$). The simulations were performed using a feedback capacitor (C_{fb}) of $2.8pF$, resulting in an expected output voltage around $357mV$. The simulated results, with a control clock signal of 2MHz, are shown in figure 3.31.

In the sampling stage, the node 'A' voltage is equal to the input signal, while the output voltage is equal to zero. During the amplifying stage, an output voltage equal to $-V_{in}\frac{C_s}{C_{fb}}$ is generated and sustained until the next sampling phase.

The biasing signal properties need to be carefully selected to minimize the resultant parasitic forces. In this switched capacitor architecture, the voltage applied to the sensor electrodes, which means, the voltage signal in the node 'A', is equal to a

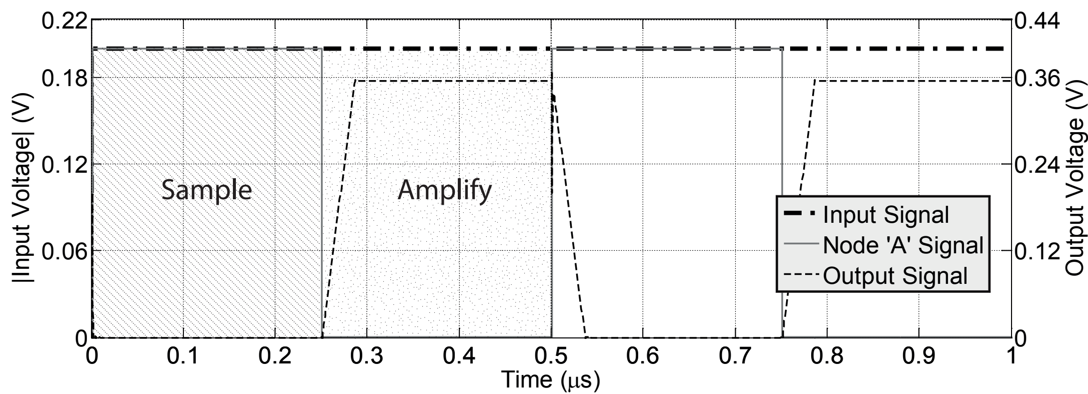
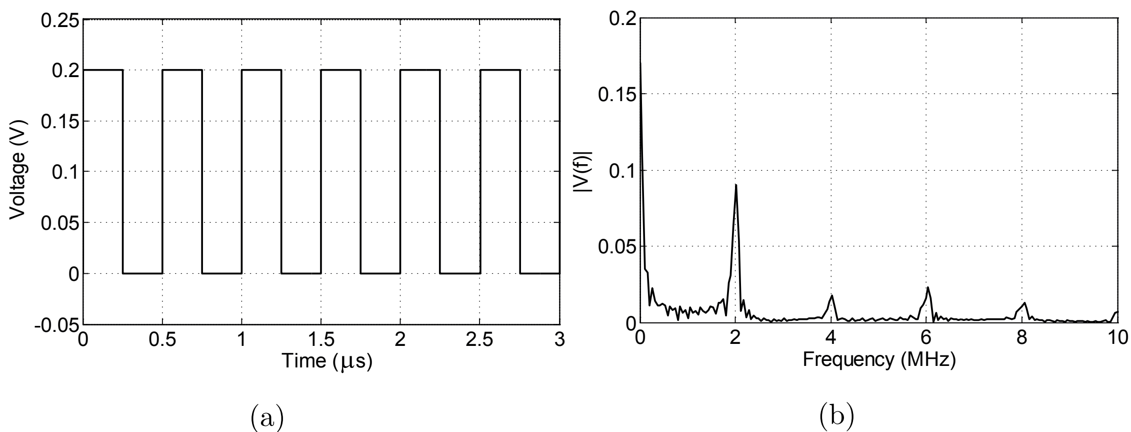


Figure 3.31: Simulation results of a simple switched capacitor amplifier.

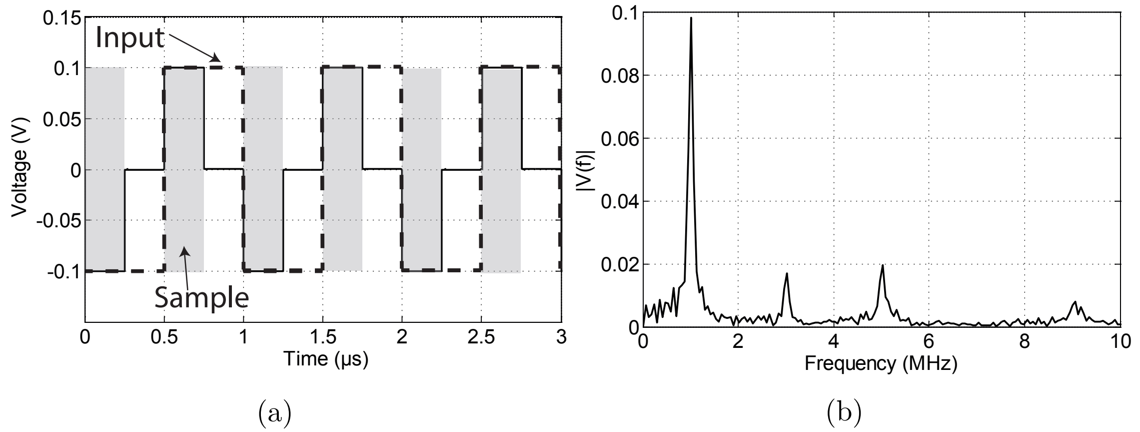
square wave at the same frequency as the control clock signal, with a peak-to-peak amplitude equal to V_{in}, figure 3.32a. In the fast Fourier transform (FFT) of the node 'A' signal (figure 3.32b), along with the 2MHz clock frequency a DC component can be seen.



(a) (b)

Figure 3.32: Applied excitation signal: a)Node 'A' signal; b)Node 'A' signal FFT.

The DC component of the node 'A' signal needs to be removed, by using a zero centered square wave input signal, eliminating this way the parasitic force that emerges from it. If this input signal frequency if of half of the clock signal (1MHz), in each sampling phase, the node 'A' voltage will change between V_{in} and $-V_{in}$ (figure 3.33a). The new FFT of node 'A' signal, shown in figure 3.33b, proves that the DC component was completely removed.



(a) (b)

Figure 3.33: Applied excitation signal without DC component: a)Node 'A' signal; b)Node 'A' signal FFT.

3.3.2 Single Ended Switched Capacitor Readout

The differential capacitive structure in the MEMS device, like in the continuous time approaches, allows the use of different configurations. Similarly to the continuous time study, the first approach to be analysed is the dual source, single output configuration (section 3.2.1), where two different source signals with 180° phase shift are used. The switched capacitor readout schematic becomes equal to the one depicted in figure 3.34.

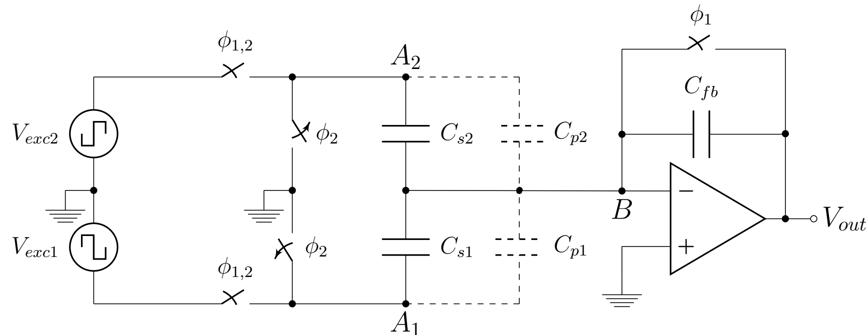


Figure 3.34: Single ended switched capacitor readout circuit.

The need of two different input square waves can be seen as a drawback and an additional source of errors. To avoid that, these excitation signals can be replaced by two symmetric DC signals (V_{in} and $-V_{in}$), if correctly sampled, where V_{in} is the peak voltage of V_{exc} (figure 3.35).

At this point, the readout circuit output is a sampled signal. Given that, there are two ways of measuring that value. The sampled output signal can be converted

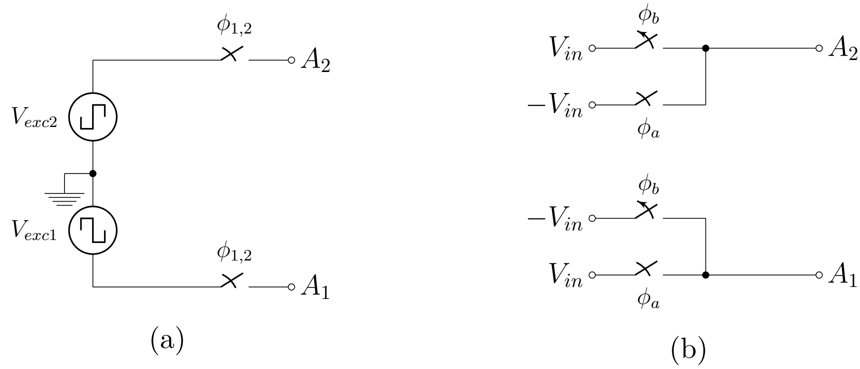


Figure 3.35: Switched capacitor input configuration: a)Square wave input; b)DC input.

to the digital domain, by using a sampled comparison (Δ Σ based operation - out of the scope for this chapter), or converted to a continuous time signal by means of sample and hold circuit (figure 3.36).

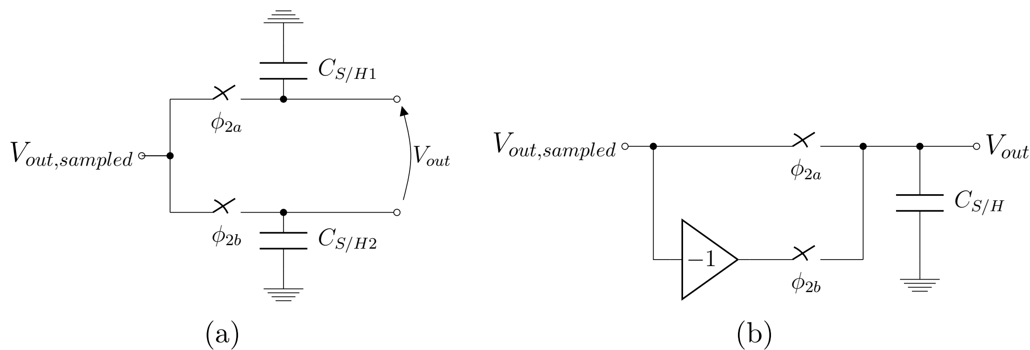


Figure 3.36: Sample and hold circuits: a)Differential output; b)Single-ended output.

By using a differential output, figure 3.36a, the common-mode noise injection is avoided. The resultant complete circuit is represented in figure 3.37, and the required control clock signals are depicted in figure 3.37b.

The use of the sample and hold circuit, at the output of the switched-capacitor circuit, avoids the requirement for a demodulation stage, since the output voltage is already a continuous time signal. An analog compensation or filter circuit might be required to remove any noise inferred by the switch commutation or by any input mismatch.

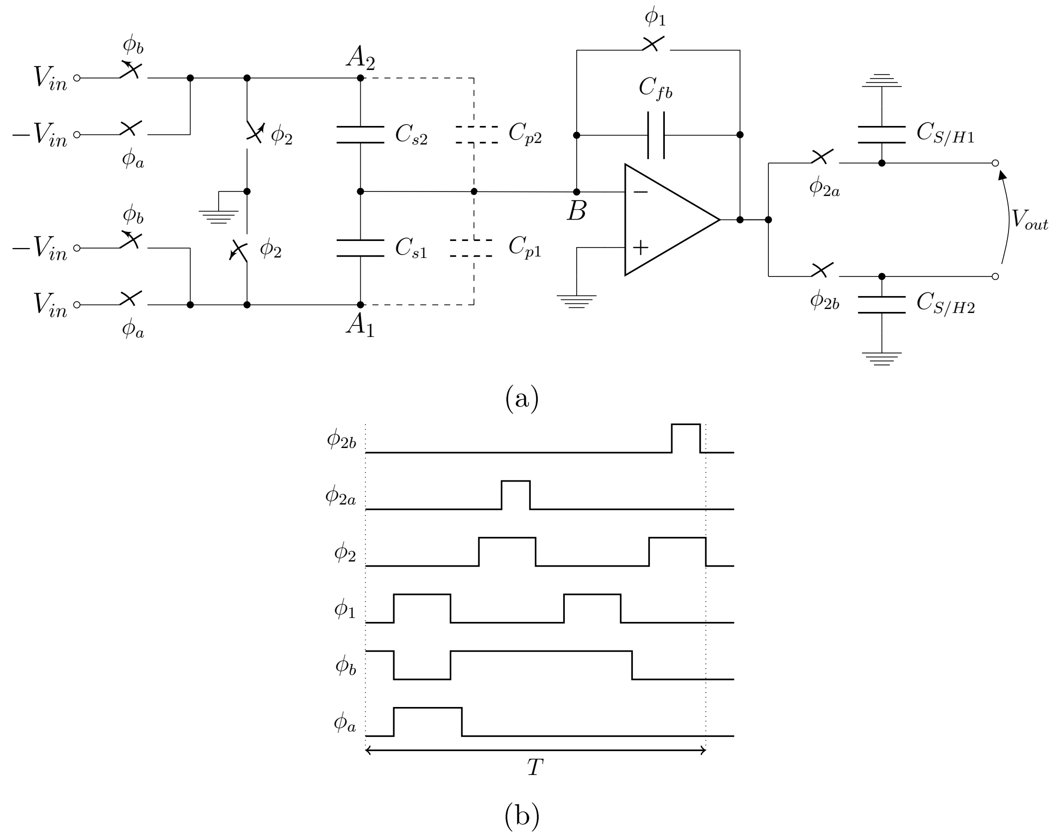


Figure 3.37: Switched capacitor avoiding parasitic charge injection: a)Schematic; b)Control clock signals.

Simulated Results

The switched capacitor architecture was simulated using a Simulink model, where two voltage controlled capacitors were used as the structure sensing capacitors. The capacitance value was controlled by a 1KHz sine wave with an amplitude that corresponds to the total gap, i.e. corresponds to a $2.25\mu m$ displacement. The theoretical $3V$ output at the maximum displacement point was achieved, as shown in the simulated results on figure 3.38.

3.3.3 Fully Differential Switched Capacitor Readout

Using the switched capacitor circuit in a fully-differential configuration benefits from using only one excitation source, as well as the rejection of the common-mode noise input. The schematic for the proposed circuit, excluding the common-mode voltage control, is depicted in figure 3.39. The switching control clock signals are presented in figure 3.39b.

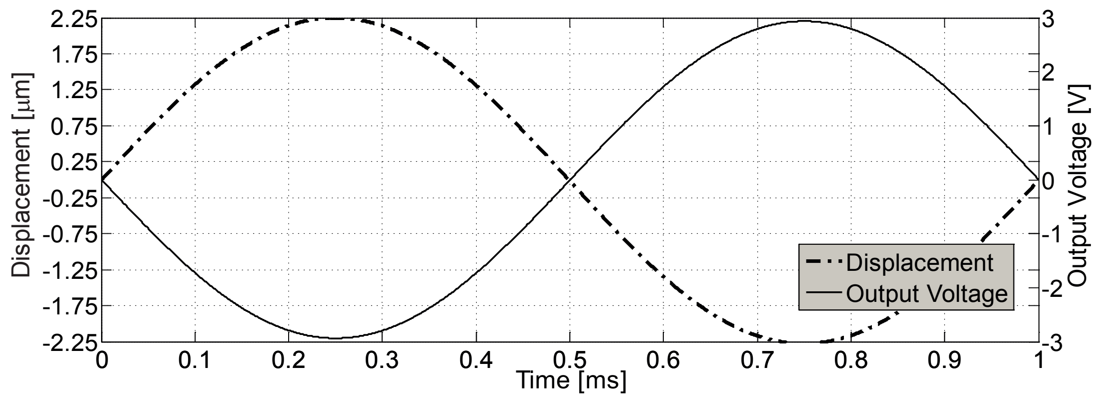


Figure 3.38: Simulated Result.

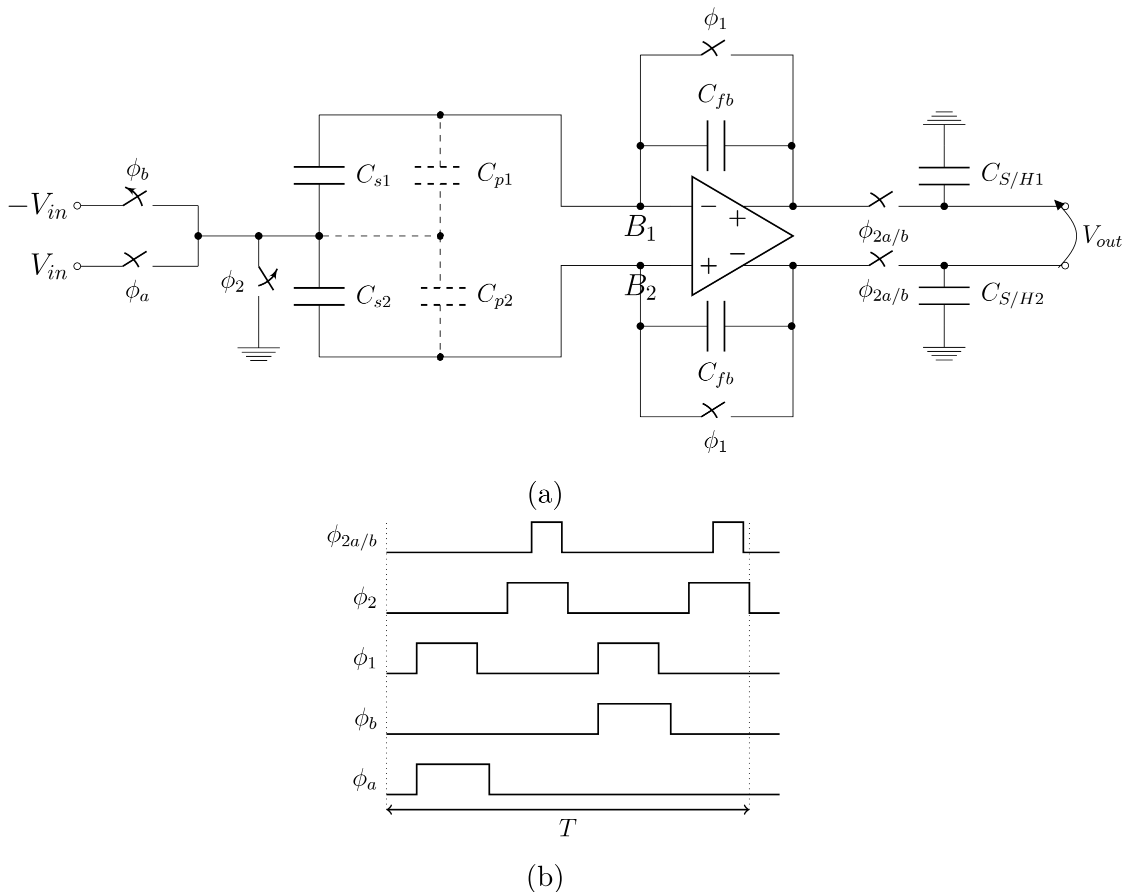


Figure 3.39: Fully differential switched capacitor avoiding parasitic charge injection: a)Schematic; b)Control clock signals.

Simulated Results

To validate the studied concepts, a Simulink model was created and used to simulate the circuit behavior, where two voltage controlled capacitors were used as the

structure sensing capacitor. The capacitance value was controlled by a 1KHz sine wave with an amplitude that corresponds to the total gap, i.e. corresponds to a $2.25\mu m$ displacement.

The simulated results of the proposed switched capacitor circuit are depicted in figure 3.40.

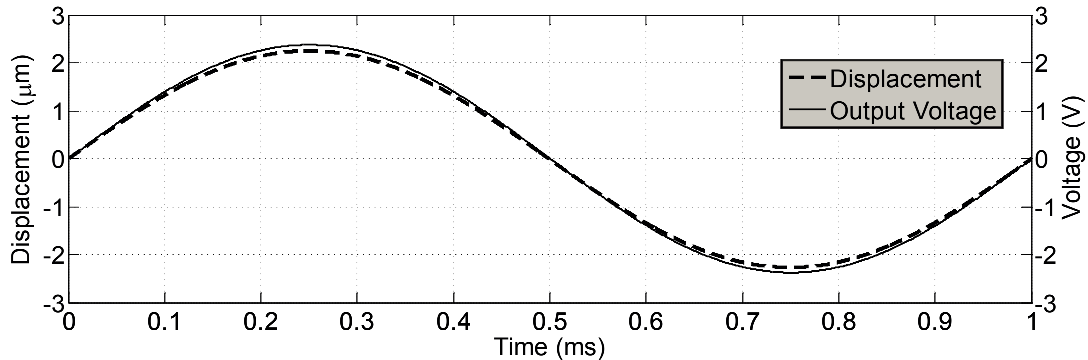


Figure 3.40: Simulated Result.

3.3.4 Noise Contribution

The main sources of noise in a switched capacitor circuit are the switches and the amplifier [3.19]. By analysing the simplified switched capacitor schematic presented in figure 3.30, the noise sources in each operating phase can be identified (figure 3.41). In the amplifying phase, the sample-and-hold circuit switch was added to the schematic as SW_4.

The resistors R_{on1},R_{on2},R_{on3} and R_{on4} represent the ON resistance of the SW_1, SW_2, SW_3 and SW_4 switches. The sample-and-hold circuit capacitance is represented as C_L, while the differential sensing capacitances are used as C_{s1} and C_{s2}.

Assuming that a multi-stage frequency compensated operational amplifier is used ($GBW = \frac{gm}{Cc}$), the mean-square noise power, induced by the switches, can be expressed as [3.5]:

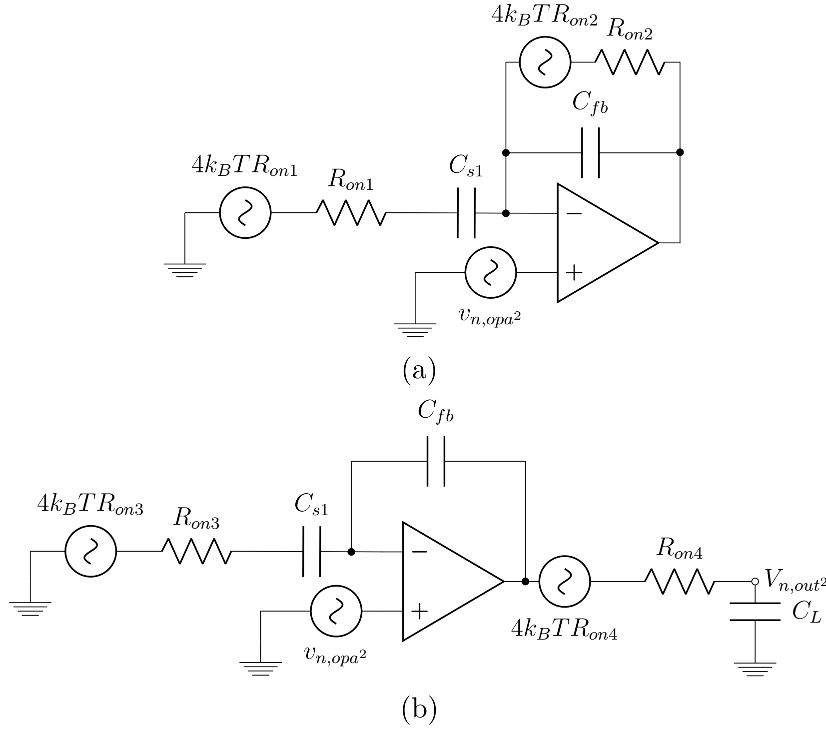


Figure 3.41: Switched capacitor noise contribution: a)Sample phase; b)Amplifying phase.

$$C^2_{n,sw,rms} \approx \frac{k_BT.gmR_{on1}.{C_{s1}}^2}{Cc.{V_{exc}}^2} + \frac{k_BT.C_{s2}}{{V_{exc}}^2} + \frac{k_BT.gmR_{on2}{C_{s1}}^2}{Cc.{V_{exc}}^2} + \frac{k_BT}{\left(\frac{{C_L}^2}{C_{s1}{C_{s2}}^2} + \frac{{C_L}^2}{{C_{s2}}^3} + \frac{C_L}{{C_{s2}}^2}\right).{V_{exc}}^2}. \tag{3.33}$$

The first two terms correspond to the noise injection by SW_1 and SW_2 in the sample phase (noise sample into C_{s1} and C_{s2}), while the last two terms are caused by SW_3 and SW_4 in the amplification phase (sampled into C_L). Looking at the equation, it can be seen that the first and third terms depend on the amplifier transcondutance, gm, therefore the noise bandwidth can be reduced. It means that the terms that are not limited by the amplifier bandwidth will dominate the switches noise contribution.

The mean-square noise power of the operational amplifier can be expressed as [3.5]:

$$C^2_{n,opa,rms} = \frac{4\gamma_n k_BT}{3} \times \left[\frac{{C_{s1}}^2}{Cc.{V_{exc}}^2} + \frac{(C_{s1} + C_{ss})^2}{Cc.{V_{exc}}^2}\right]. \tag{3.34}$$

The noise contribution of the amplifier can be reduced through the increasing of the compensation capacitor Cc.

The total noise contribution can then be simplified to the switches thermal noise that is not limited by the amplifier bandwidth, namely the second and fourth terms of equation (3.33).

3.4 Conclusion

In this chapter, various front-end circuits for capacitive MEMS devices were presented. The major available architectures were compiled and presented in figure 3.1. The main focus of this study was on the capacitance-to-voltage converters, since the pull-in detection can be performed in the analog domain, no digital output signal is required. These capacitance-to-voltage converters were then divided into two categories, those that operate in the continuous-time and discrete-time domains.

It is know that the continuous-time readout circuits can operate at the mechanical resonance frequency of the MEMS device or at a higher frequency. The typically low resonance frequency requires large time constants and therefore large areas, increasing the input-referred noise of the resistor used for DC biasing as well as the flicker (1/f) noise contribution of the operational amplifier. Those are the reasons why the higher carrier frequency modulation was the one studied here.

By using the higher frequency modulation the biasing resistor noise contribution is reduced, as it is the flicker noise. On the other hand, higher operation frequency demands for higher consumption. An additional demodulation stage is also required to retrieve the desired sensor information.

In the discrete-time domain, an alternative approach for the CVC implementation was proposed. These switched capacitor approaches eliminate the need of large biasing resistors, as the switching takes care of the proper biasing. Based on that, smaller silicon area and lower power are required, making it a very attractive solution for integration, specially in applications that do not require high SNR. The use of a sample-and-hold circuit at the output generates the desired continuous-time signal.

Based on these conclusions and considering the pull-in based transduction mech-

anism (large capacitance change), as well as the differential capacitive sensing structure of the MEMS devices, the selected architecture for this application was the fully-differential switched capacitor (section 3.3.3).

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4

Integrated System Implementation

Different prototypes of the proposed MEMS inclinometer were designed and implemented, in order to experimentally study the proposed transduction mechanism. The implementation of these prototypes includes the design and fabrication of the MEMS sensing element, as well as the interface electronics. On an early stage, the interface electronic circuit was realized at the PCB level using COTS and a FPGA to implement the digital functionalities. Later, when the approach was validated [4.1], a mixed-signal integrated circuit was designed and fabricated. In this new implementation, as shown in figure 4.1, the capacitance-to-voltage converter and the pull-in detection mechanism, previously performed using an ADC, were implemented in the integrated circuit analog domain, while the sensor control and communication is now in the digital part of the same integrated circuit. The DAC, used to generate the actuation voltage, is external in both approaches.

This chapter presents the implemented system in detail. Since the final goal was to implement the interface electronics in an integrated circuit, only this approach is addressed here. First, in section 4.1, the sensing element design characteristics and the fabrication process used are introduced. Then, in section 4.2 and section 4.3, the custom ASIC implementation is described, starting with the analog circuits,

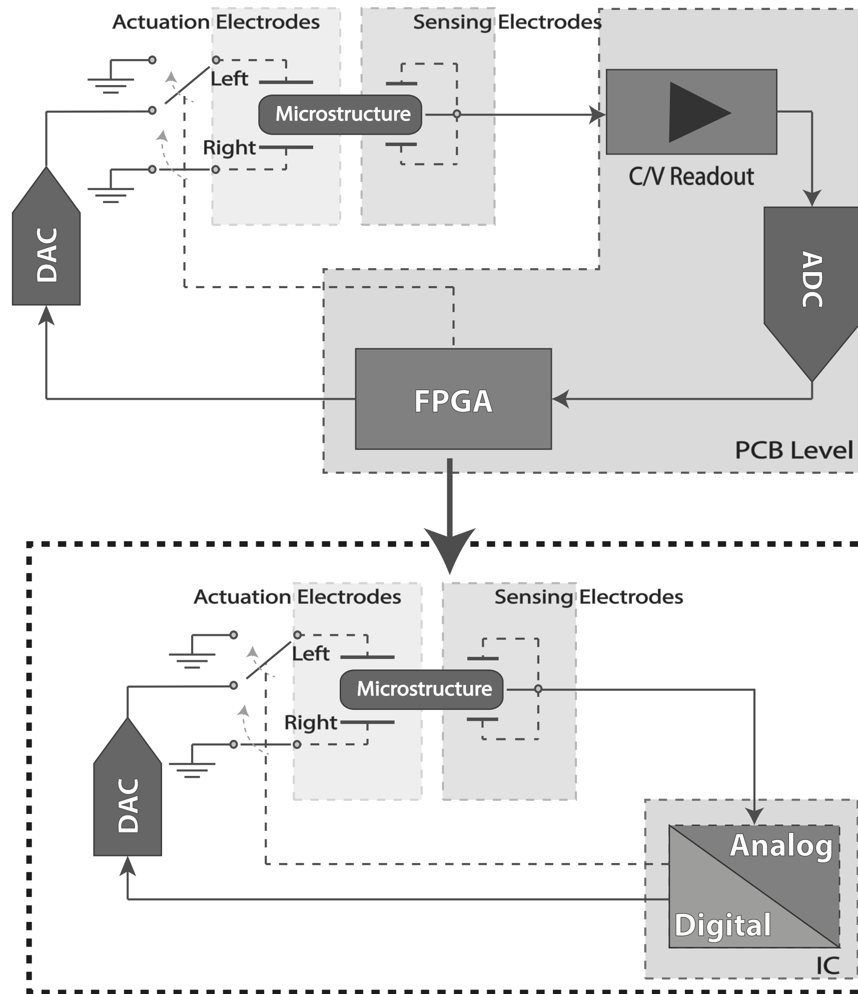


Figure 4.1: Block diagram highlighting the changes between the FPGA based approach and the ASIC one.

followed by the digital control and communication. The system final integration is described in section 4.4 and the conclusions are drawn in section 4.5.

Before moving forward to the system implementation, some considerations need to be stated. The ASIC was designed and manufactured using a $0.35\mu m$ CMOS technology from Austriamicrosystems (AMS) with a nominal supply voltage of $+3.3V$ [4.2]. The technology provides analog capacitors and high-ohmic polysilicon resistors. The digital control system was implemented, taking into consideration that the external DAC to be used is the single 20-bit, unbuffered voltage-output DAC from Analog Devices AD5791, that uses a SPI (serial peripheral interface) compatible 3-wire serial interface with clock rates up to 35 MHz [4.3].

4.1 MEMS sensing Element

For the realization of the sensor prototypes used throughout this work, different sets of microelectromechanical devices were designed and fabricated. These devices have been fabricated using micromachining processes, from the Iberian International Nanotechnology Laboratory (INL). Based on a Silicon-On-Insulator (SOI) wafer, different active layer thicknesses were used ($25\mu m$ and $50\mu m$).

SOI processes are commonly used for in-plane capacitive movable structures, as the thick active layers provide large sidewall areas and therefore large capacitance values. The large active layer thickness also enables the design of large proof mass devices, which is really important when designing inertial sensors (it increases sensitivity while reducing the Brownian noise). The high aspect ratio capabilities of the micromachining process is required for designing small gaps, obtaining this way, large capacitances and low pull-in voltages.

The design of a microstructure must take into consideration the micromachining process limitations and characteristics, while aiming to obtain the desired device behavior. The fabricated microstructures have been designed aiming to maximize pull-in sensitivity to acceleration, minimize mechanical-thermal noise and maximize the sensing capacitance change. The different micromachined structures, used in the experimental work throughout this thesis are described in this chapter, although the design and parameters decisions are out of the scope of this thesis [4.4].

4.1.1 Fabrication Process

In this work four sets of microstructures were used. Two of them were fabricated using a $25\mu m$ SOI wafer (#2 and #3) while the others were micromachined on a $50\mu m$ SOI wafer (#1 and #4). The designs of the devices named as #1 and #2 are very similar only differing on the spring widths and size of the extra mass (#1 structure has smaller spring width than #2). These two dedicated microstructures (#1 and #2) were fabricated using the same process, which allows processing capacitive microstructures with four folded-springs and extra proof-mass using $25\mu m$ and $50\mu m$ SOI wafers. The extra mass is the result of keeping a portion of the handle wafer attached to the movable part of the microstructure, similar to the process reported in [4.5]. The main fabrication steps are shown in figure 4.2a:

1. Wafer Preparation: Initially, a 2.5μm layer of silicon dioxide (SiO_2) is deposited on the backside (BS) of the wafer by plasma-enhanced chemical vapor deposition (PECVD).

2. Extra Proof-Mass Hard-Mask Patterning: The BS oxide is then patterned by reactive ion etching (RIE), for definition of the extra proof-mass.

3. Metal Layer: A 330nm thick metal layer is sputtered on the front side (FS) and patterned for pads and routing.

4. Microstructure Patterning: A SiO_2 layer of 3μm is deposited on the FS by PECVD and patterned, to serve as hard-mask for the definition of the microstructure.

5. Sensors Structure Etching: Using the buried oxide as etch stop, the front and back sides are sequentially etched using deep reactive ion etching (DRIE).

6. Structure Release: The structure is finally released by dry Hydrofluoric Acid (HF) vapor etching.

Using a similar fabrication process to the one used in devices #1 and #2, the structure #3 was fabricated without any extra proof-mass attached to the movable part. The resulting process is the same as the previously described one, only differing on the back-side patterning shape (no extra proof-mass needs to be defined), and in the microstructure pattern (different points presented below - points 2 and 4). In this process, the indicated step is performed using a resist sacrificial layer, as no hard-mask is needed (active layer of 25μm). The resulting process is shown in figure 4.2b:

2. Back-Side Patterning: The BS oxide is then patterned by RIE, for definition of the back-side cavity.

4. Microstructure Patterning: A resist layer is coated on the FS, followed by a lithography.

For the fabrication of the microstructure #4, a slightly different process was adopted. This time, no back-side mask is used as the structure release is performed from the front-side. The fabrication steps are represented in figure 4.2c:

1. Metal Layer: A 465nm thick metal layer is sputtered on the front side and patterned for pads and routing.

2. Metal Patterning: Metal layer is patterned for pads and routing using RIE.
3. Hard-mask preparation: A SiO_2 layer of $3\mu m$ is deposited on the FS by Chemical Vapor Deposition (CVD). A resist sacrificial layer is coated and patterned, to define the hard-mask.
4. Microstructure Patterning: The oxide layer is patterned using RIE, to serve as hard-mask for the definition of the microstructure.
5. Sensors Structure Etching: Using the buried oxide as etch stop, the front side is etched using the Bosch process (DRIE).
6. Structure Release: The structure is finally released by HF vapor etching.

The major difference between the first two fabrication processes (used in #1, #2 and #3) and the last one (used in #4) is the handle-wafer etching. Releasing the movable structures without opening a cavity on the back side leads to an easier fabrication process, since no back-side mask is needed, therefore less fabrication time. Even though this is a major advantage when testing new designs (more devices can be fabricated in the same time period), higher parasitic capacitances in these devices are expected, when compared to the ones with a cavity in the substrate.

4.1.2 Fabricated Devices

All the fabricated devices are in-plane capacitive movable structures (parallel to the die plane). The parallel-plate capacitor structure is formed by an array of electrodes in the movable proof-mass (comb-like structure) together with a fixed one. The capacitance area is defined by the thickness of the SOI active layer, the overlapping length and the number of electrodes. Each device is composed by two sets of actuation electrodes, for the left and right side pull-in measurement, and two sets of sensing electrodes, enabling differential capacitive readout. Additionally, even though they are not used in this work, device #3 has two sets of linear actuators, referred to as comb-fingers, that enable the possibility of testing additional compensation and calibration mechanisms.

As introduced in previous chapters, the fabricated devices were designed with mechanical stoppers that limit the device displacement and prevent contact between the movable and fixed parallel-plates. The gaps between the parallel-plates were

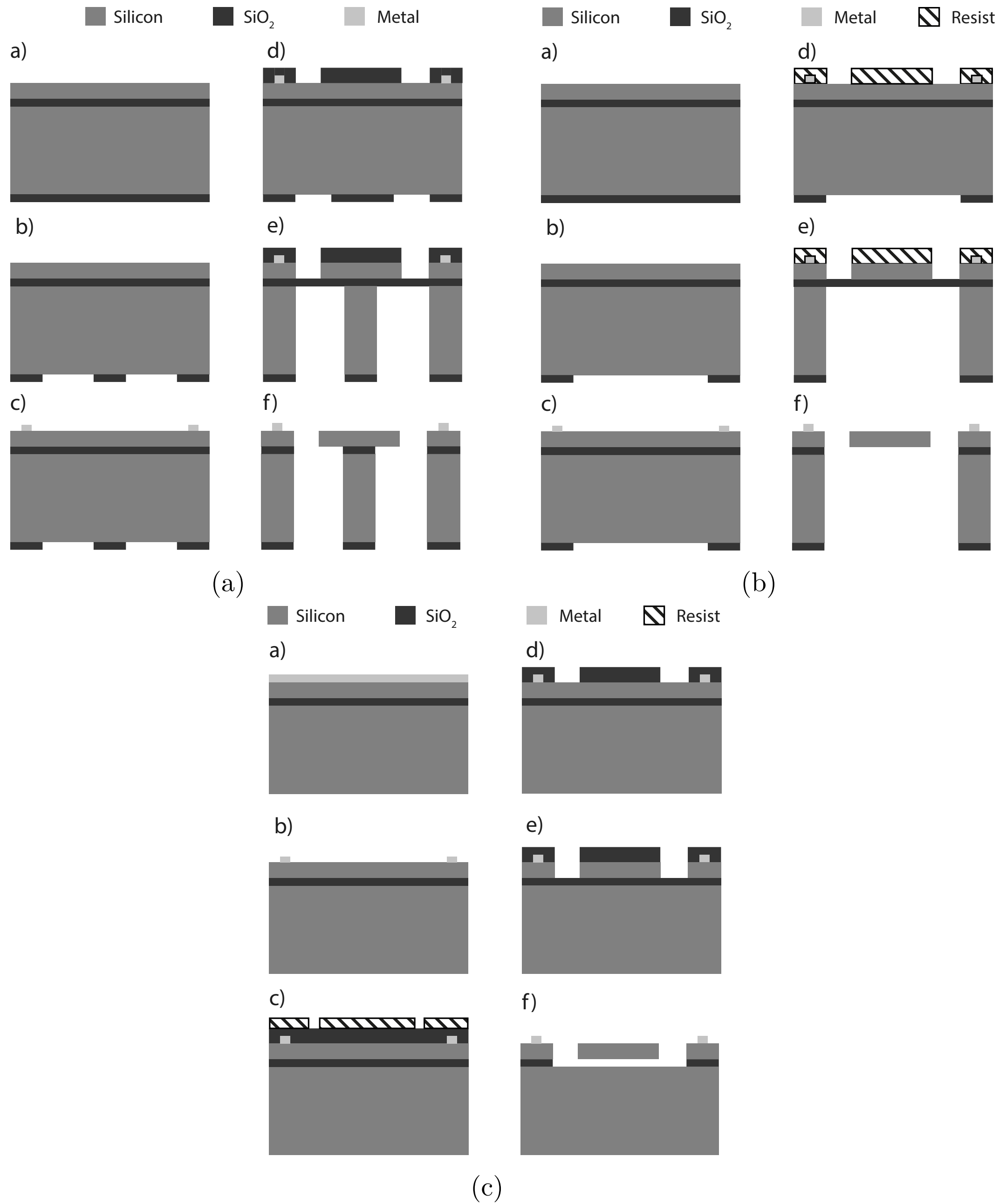


Figure 4.2: Fabrication process of the sensing devices. a) With extra proof-mass (#1 and #2). b) With backside cavity (#3). c) Without backside etching (#4).

standardized at $2.25\mu m$-wide for all the devices, and the stoppers $2\mu m$ apart from the movable mass. In this way, the proof mass can move $2\mu m$ to each side (gap variation between 0.25 and $4.25\mu m$) without contact occurring between the movable and fixed electrodes. To avoid large currents flowing through the device during contact, the stoppers are powered at the same voltage potential as the movable mass.

In each device, the proof-mass is suspended on four flexible beams, acting as springs. The design of the beam will define the dominant degree-of-freedom of the mass displacement, which in this case should be perpendicular to the plane of the parallel-plates capacitors. The springs architecture is specially important when aiming to minimize the displacement in other directions to a negligible state, which turns the structure into a 1-DOF device. In order to obtain compliant enough springs without compromising its feasibility, different spring designs were used.

Elastic Spring

The elastic coefficient of the spring is calculated by applying elementary elasticity equations. If the simplest spring design is considered (single beam fixed at one end), with a force that is applied perpendicular to its length, l (with bending angle constrained), the linear stiffness coefficient is given by [4.6]:

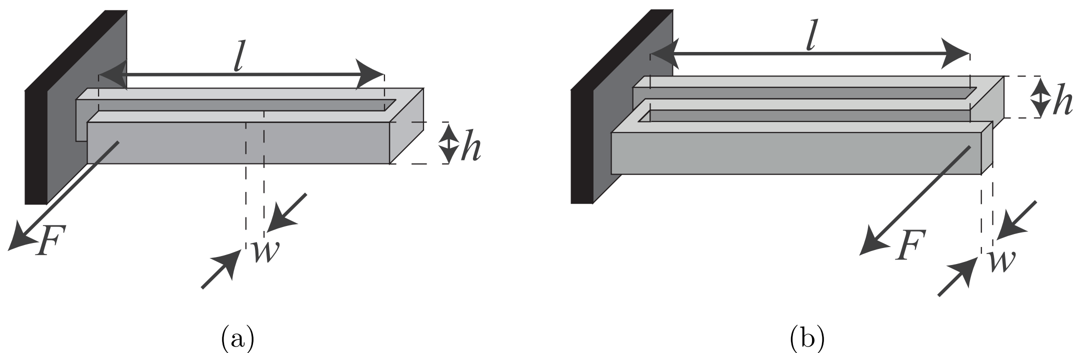
$$k = \frac{12EI}{l^3}, \tag{4.1}$$

where E is the elastic modulus of the material, Young's modulus, and I is the momentum of inertia of the cross-sectional area of the beam. This momentum of inertia for a specific bending direction is given by:

$$I = \frac{hw^3}{12}, \tag{4.2}$$

where h is the beam height and w corresponds to the width (considering the bending in the direction of the width). The Young's modulus of silicon in the bending direction is of about 169GPa, since the SOI wafers where the devices were fabricated have the device layer surface with (100) orientation.

On the fabricated devices, two different spring designs can be found. Structures #1, #2 and #4 have simple folded springs, represented in figure 4.3a, while device #3 was designed with bi-folded springs (figure 4.3b). Considering that the elbows, or folding points, are rigid, the deflection is divided by the number of beams (2 in the folded designs or 3 in the bi-folded ones). The resulting stiffness coefficient (of one spring) is then defined by:



(a) (b)

Figure 4.3: Different spring designs. a) Folded spring (#1, #2 and #4). b) Bi-folded spring (#3).

$$\frac{1}{k_{spring}} = \frac{1}{k_{beam_1}} + \frac{1}{k_{beam_2}} \left(...\right) + \frac{1}{k_{beam_n}}. \tag{4.3}$$

As the inertial mass is suspended on 4 springs (folded or bi-folded, depending on the device), the total stiffness coefficient for each device is $k_{total} = 4 \times k_{spring}$. The springs were designed taking into consideration the maximum displacement of the mass, $2\mu m$, in order to assure that the spring is always operating in the linear region (obeying to Hooke's law).

Scanning electron microscope (SEM) images of the fabricated structures are shown in figure 4.4, showing the separated sensing and actuation electrodes. According to the previously defined notation, the devices fabricated with extra proof-mass are depicted in figure 4.4a, namely structure #1 and #2 (differing on the thickness of the active layer #1-25μm, #2-50μm). The 25μm thick structure with comb actuators and cavity in the handle wafer, structure #3, is represented in figure 4.4c, while figure 4.4b is the image referring to the device named as #4, with no cavity in the substrate and a 50μm device layer.

A compilation of the main design parameters of the four different fabricated devices is presented in table 4.1. It is important to notice that, these are analytically calculated parameters, using standard atmospheric conditions.

4.2 Analog Circuit

Based on the analysis performed in chapter 3, the readout circuit topology that has been chosen is based on a discrete-time capacitance-to-voltage converter. The

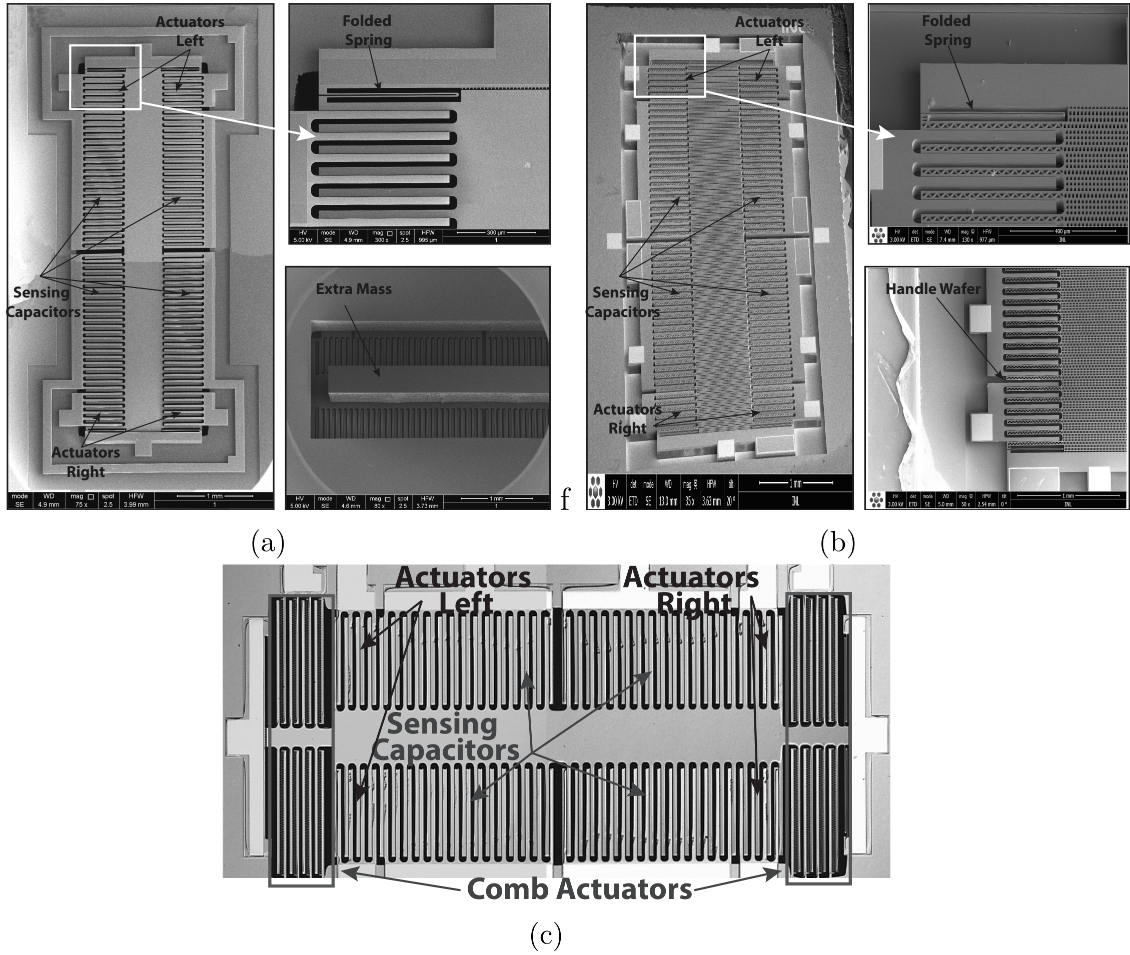


Figure 4.4: SEM images of the fabricated MEMS devices. a) Extra mass device (#1 and #2). b) Device with handle wafer (#4). c) Device with comb-fingers (#3).

Table 4.1: MEMS devices design parameters.

Device Parameters	**#1**	**#2**	**#3**	**#4**
Mass (m)	$3.52mg$	$3.52mg$	$0.149mg$	$0.425mg$
Mechanical spring (k)	$20.8N/m$	$19.7N/m$	$4.461N/m$	$6.159N/m$
Zero-displacement gap (d_0)	$2.25\mu m$	$2.25\mu m$	$2.25\mu m$	$2.25\mu m$
Natural resonance frequency (f_0)	$385Hz$	$377Hz$	$870Hz$	$606Hz$
Damping coefficient (b)	$10.6mN.s/m$	$1.54mN.s/m$	$0.756mN.s/m$	$4.6mN.s/m$
Actuation capacitance (Ca_0)	$1.32pF$	$0.662pF$	$0.394pF$	$1.18pF$
Sensing capacitance (Cs_0)	$5.06pF$	$2.54pF$	$1.48pF$	$4.53pF$
Mechanical-thermal noise	$21.7\mu°/\sqrt{Hz}$	$8.36\mu°/\sqrt{Hz}$	$137.5\mu°/\sqrt{Hz}$	$118.8\mu°/\sqrt{Hz}$
Quality factor (Q)	0.814	5.40	1.078	0.353
Active Layer Thickness	$50\mu m$	$25\mu m$	$25\mu m$	$50\mu m$
Extra proof-mass	*yes*	*yes*	*no*	*no*

pull-in transduction enables relaxing on the readout noise floor, as compared to a directly transduced capacitive sensor.

A simplified block diagram of the designed analog circuit is presented in figure 4.5. The circuit can be divided in 4 major blocks: the CVC, responsible for converting the MEMS sensing capacitance into voltage; the pull-in detection mechanism; the control signals generation block, that controls the generation of the non-overlapping clocks and the temperature insensitive current generator. Each of these "sub-circuits" is going to be addressed individually in this chapter.

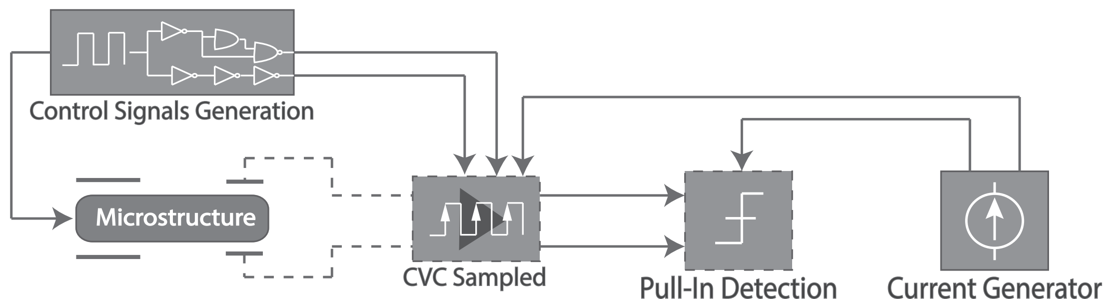


Figure 4.5: Block diagram of the analog circuit main components.

Taking into account that different sensing microstructures can be tested using the developed readout circuit, the system has been developed with some configurable parameters, specifically, the capacitance-to-voltage converter gain and input voltages, as well as the pull-in detection reference value.

4.2.1 Capacitance to Voltage Converter

The main, and probably most important, component of the entire ASIC is the CVC. Any malfunction in this stage will be propagated to the system output, compromising the overall sensor's performance.

The readout of the sensor's capacitance is performed with a discrete-time differential switched capacitor circuit, introduced in detail in section 3.3, and the resulting schematic is shown in figure 4.6a. The differential output voltage calculation was already explained, but for the sake of convenience, it is rewritten below (ignoring the parasitic capacitances):

$$V_{out} = -\left(\frac{C_{left}}{C_{fb}} - \frac{C_{right}}{C_{fb}}\right)V_{in}. \tag{4.4}$$

From the previously studied circuits, a few modifications can be seen in the proposed schematic. Considering that, the circuit has been designed to operate using

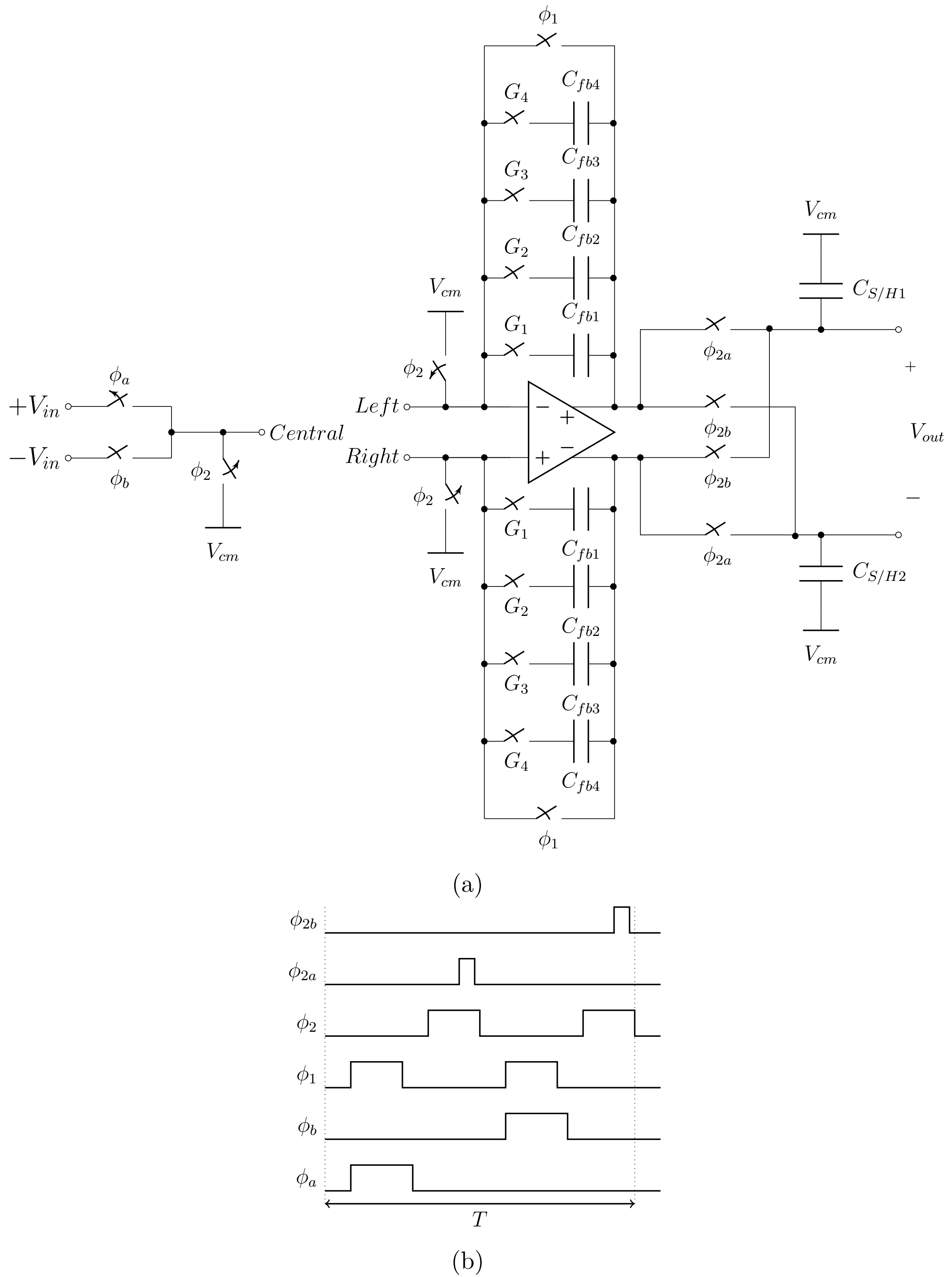


Figure 4.6: Fully differential switched capacitor CVC with a chopped sample-and-hold output: a)Schematic; b)Control clock signals.

a single supply $(+3.3V)$, a common-mode input voltage, V_{cm}, is used as reference. This way, it can be guaranteed that the readout circuit and the MEMS sensing

device are centered at the same voltage.

Two additional switches were added at the amplifier input, in order to guarantee that, in the amplifying phase, there is a known voltage potential at both amplifier inputs. By doing that, the output voltage generated through the feedback capacitor is secured as $V_{out} = V_{cm} \pm (V_{in} \times \frac{Cs}{Cfb})$. Taking into account that the used input voltage, during the sampling phase, changes between $+V_{in}$ (during the period a) and $-V_{in}$ (during the period b), the sample-and-hold circuit is used as a chopper stabilizer. In each semi-cycle, a and b, the output polarization is inverted, hence a continuous output signal is achieved (V_{out}).

Different feedback capacitors were added to the switched capacitor converter, as a way to choose the desired CVC gain. The feedback capacitors' values, used in the circuit, are presented in table 4.2. As more than one capacitor can be selected at a time, different gain configurations can be selected (controlled by the digital unit).

Table 4.2: Capacitors values.

Capacitor Name	C_{fb1}	C_{fb2}	C_{fb3}	C_{fb4}	$C_{S/H1}$	$C_{S/H2}$
Value	$250fF$	$500fF$	$1pF$	$2pF$	$1pF$	$1pF$

Control Switch

Until this point, the switches used on the circuit have been referred to without specifying how they have been implemented. A MOS transistor can serve has a switch, as it is capable of conducting current in either directions, just by exchanging the roles of the source and drain terminals. A serious limitation of using a MOS switch can be noticed when an input signal level is close to V_{DD}, since the output provided by an NMOS switch cannot track the input. For $V_{out} \approx V_{in}$, the transistor must operate in the deep triode region ($V_{in} < V_{DD} - V_{th}$), as a way to avoid the ON resistance to increase considerably, as:

$$R_{on,N} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{DD} - V_{in} - V_{th})}. \tag{4.5}$$

The same principle can be applied to PMOS switches when $V_{in} \leq |V_{th}|$, as the ON resistance is given by:

$$R_{on,P} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{in} - |V_{th}|)}. \quad (4.6)$$

This problem can be overcome by employing complementary switches, also know as transmission gate. By combining the two transistors, and using a complementary control signal (figure 4.7a), an equivalent ON resistance is obtained:

$$R_{on,eq} = R_{on,N} || R_{on,P} \equiv$$
$$R_{on,eq} = \frac{1}{\mu_n C_{ox} \frac{W_n}{L_n}(V_{DD} - V_{thN}) - \left[\mu_n C_{ox} \frac{W_n}{L_n} - \mu_p C_{ox} \frac{W_p}{L_p}\right] V_{in} - \mu_p C_{ox} \frac{W_p}{L_p} |V_{th}|}. \quad (4.7)$$

From equation (4.7), it can be concluded that, if both transistors are dimensioned in a way that: $\mu_n C_{ox} \frac{W_n}{L_n} = \mu_p C_{ox} \frac{W_p}{L_p}$, then, if body effects are ignored, $R_{on,eq}$ is independent of V_{in} (figure 4.7b).

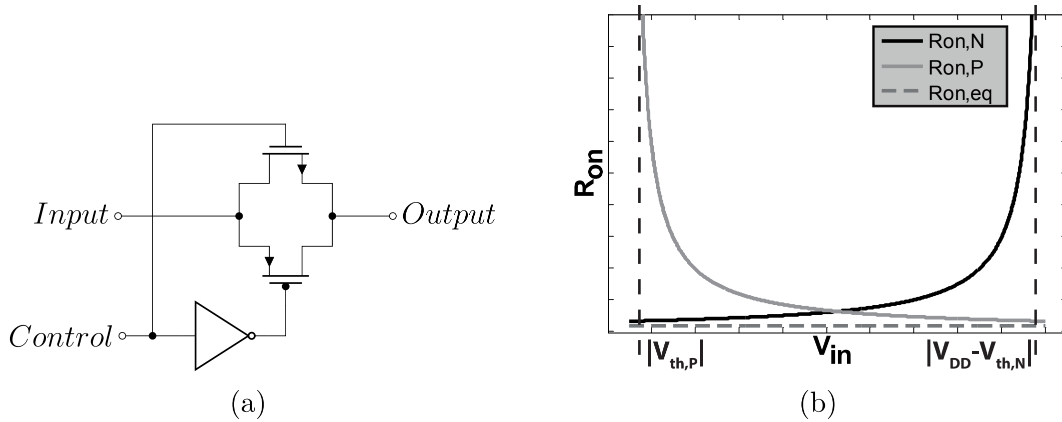


Figure 4.7: Transmission gate. a) Complementary switch schematic. b) On-resistance of the complementary switch.

The presented solution is used throughout the entire circuit design to implement all the required switches, only changing the transistors' sizes to achieve the desired ON resistance.

Excitation Signal

In an attempt of give more configurability to the readout circuit, the amplitude of the input signals, $+V_{in}$ and $-V_{in}$, was designed to be digitally selected from a

predefined voltage range. These excitation signals are generated by a resistor-based voltage divider, as shown in figure 4.8, in order to take advantage of the high-ohmic polysilicon resistors available in the used technology. This architecture allows creating the desired circuit in a smaller area, when compared with a capacitor based one, without significantly increasing the power consumption.

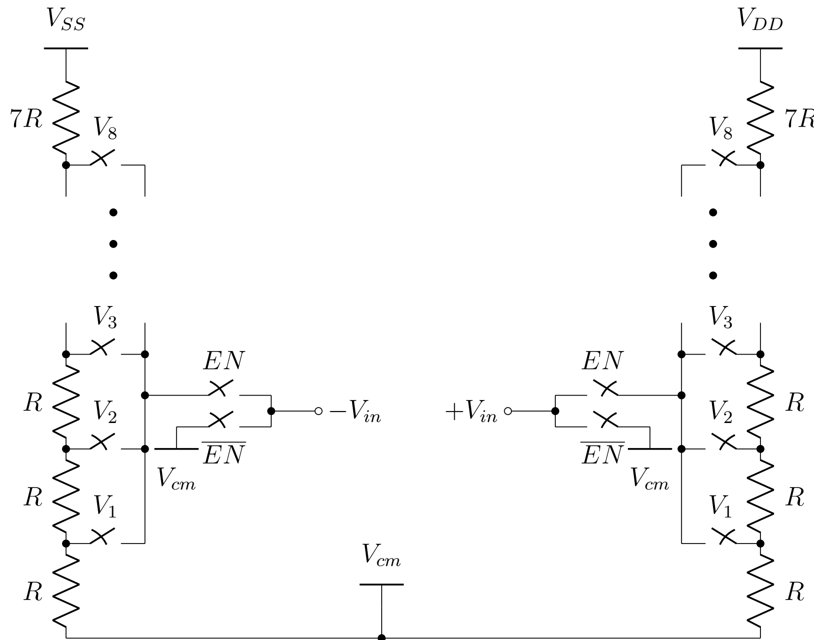


Figure 4.8: Configurable input voltage generation.

The input voltage amplitude can be selected from 8 different values, $V_1 - V_8$, in which the value is defined by the total current, $I = \frac{VDD-VSS}{2\times(8R+7R)}$. An unitary resistor value of $10K\Omega$ is used, that given the $+3.3V$ single supply retrieves a current of $11\mu A$. The input voltages ($+V_{in}$ and $-V_{in}$) can then be chosen from values between $V_{cm} \pm 110mV$ and $V_{cm} \pm 880mV$, with $110mV$ of resolution.

A 3-8 decoder, based on digital standard cells from CORELIB was implemented, enabling this way, the control of both input voltages using 3 control bits (figure 4.9).

An enable signal, EN, was added to the circuit so that no voltage is applied to the movable electrodes of the MEMS structure when the system is not working (common-mode voltage, V_{cm}, is applied).

The outputs of this simple digital-to-analog converter are buffered, before applying to the switched capacitor circuit, as shown in figure 4.10 (enable signals not represented).

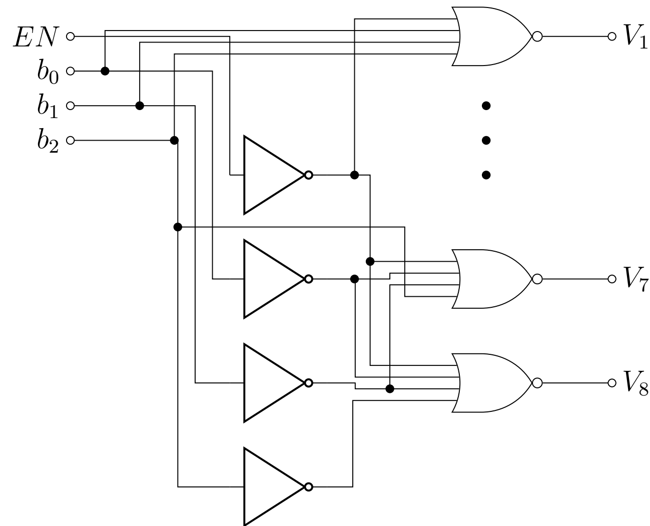


Figure 4.9: 3-8 decoder implementation.

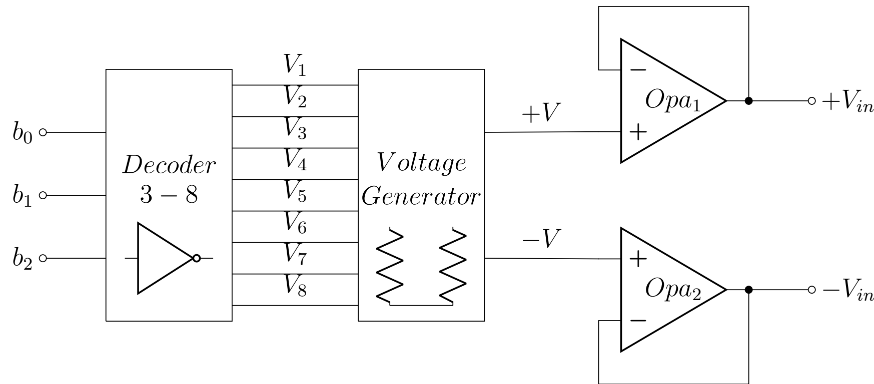


Figure 4.10: Excitation signal generation circuit.

Since both generated voltages are symmetrical, with reference to the common-mode voltage (V_{cm}), and they can get to values close to the power rails, some precautions need to be taken on the design of the amplifiers.

If the same amplifier architecture is used to buffer both voltages, in order to avoid any output saturation, two rail-to-rail amplifiers need to be used, which would add unnecessary complexity to the circuit. Alternatively, two complementary amplifiers can be used (Opa_1 and Opa_2), where different channel types are used in the differential pair of the first amplification stage.

The amplifier named as Opa_1 was designed as a 2-stage operational amplifier, using n-Channel input transistors in the first stage, and a common-source amplifier as the second stage, having a p-Channel input drive transistor, like it is shown in figure 4.11. Having a p-Channel source follower as the second amplification stage allows output voltages up to V_{DD}, with a lower limit defined by the V_{DS} voltage of

the nmos transistor (M_7). Hence, this amplifier is used to buffer the more positive input voltage signal, $+V_{in}$.

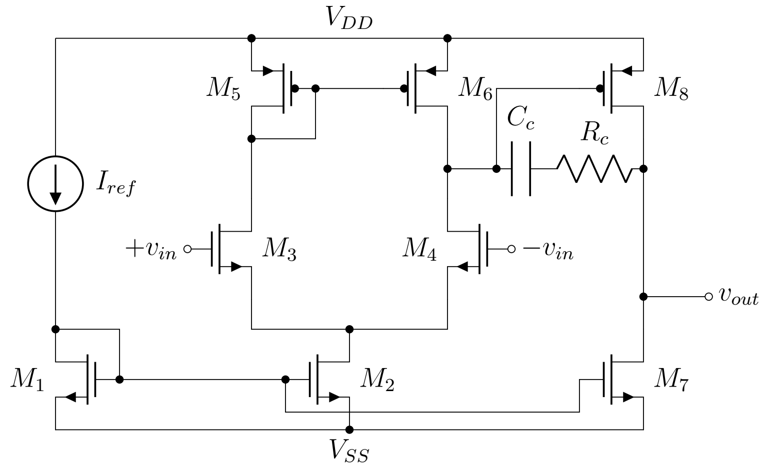


Figure 4.11: Operational Amplifier with n-Channel input stage.

The AC response of the amplifier was simulated, in order to find the achieved DC-gain and gain-bandwidth product (GBW). The simulation results are shown in figure 4.12.

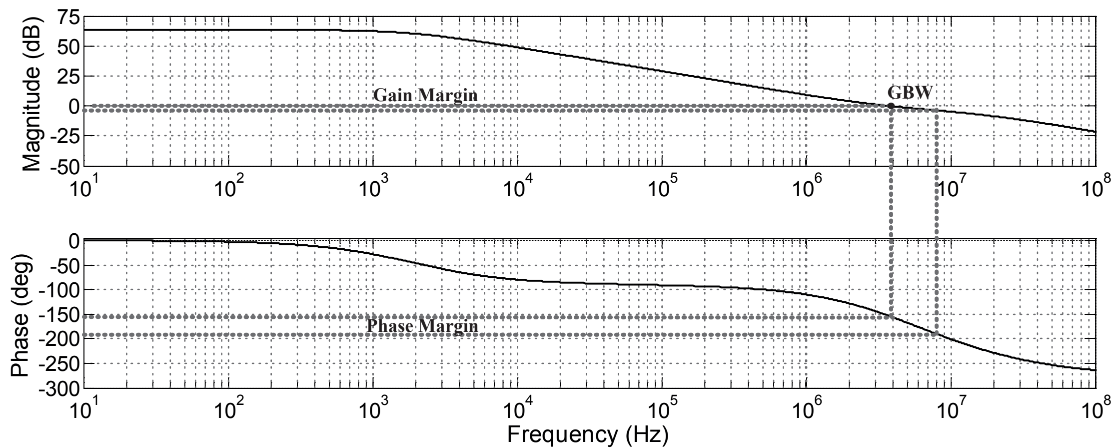


Figure 4.12: Bode diagram of the n-Channel input stage operational amplifier.

The phase margin of 40° shows that the amplifier is stable during closed loop operation, which is the case of the unitary loop gain used here. It is relevant to see that, a GBW of 4MHz was reached, validating its use at the circuit operating frequency (1MHz).

The less positive input voltage, $-V_{in}$, is buffered by a 2-stage operational amplifier with p-Channel transistors in the input differential pair, and a n-Channel source follower in the second stage (figure 4.13). This time, the output voltage is upper

limited by the V_{DS} of the pmos transistor (M_8) of the second stage and can be as low as V_{SS}.

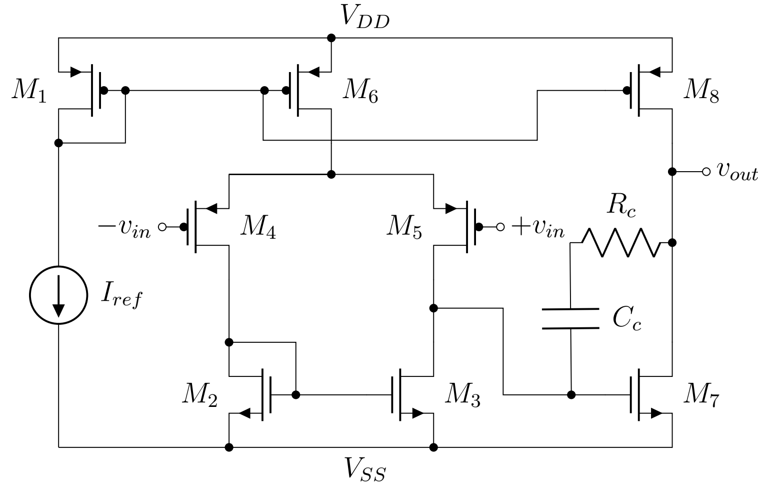


Figure 4.13: Operational Amplifier with p-Channel input stage.

The simulated results of the designed amplifier AC response are shown in figure 4.14, highlighting the DC-gain, GBW and phase margin.

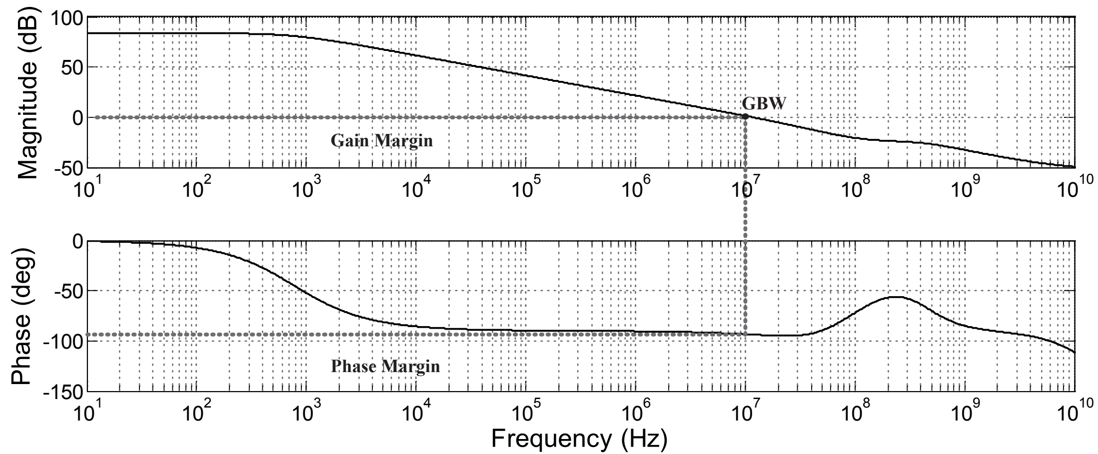


Figure 4.14: Bode diagram of the p-Channel input stage operational amplifier.

The stability of the amplifier is secured by a phase margin close to 85°. Such large margin can be looked to as an over-compensation on the amplifier, that might reduce its bandwidth. But given the 10MHz GBW, it is not a constraint for the given application. For this particular case, the DC-gain of 83dB could be reduced, minimizing the power consumption, but as it was designed aiming for a general-purpose amplifier (can be used in different parts of the circuit), it can benefit from larger gains.

Fully-differential Amplifier

The central component of the entire CVC is the fully differential amplifier. In this circuit, a multi-stage differential amplifier was implemented, aiming to have high gain (provided by the first stage) and high output swing (provided by the second stage).

A folded cascode operational amplifier with, PMOS loads (M_1 and M_2) was used as the input stage, while a common-source amplifier was used as the second stage. The schematic of the designed amplifier is depicted in figure 4.15. The NMOS active loads of the first stage (M_3 and M_4) are biased by a control signal, V_{cmfb} (generated by a common-mode feedback circuit), in order to inject or bleed current from the differential pair as required (explained latter in this section).

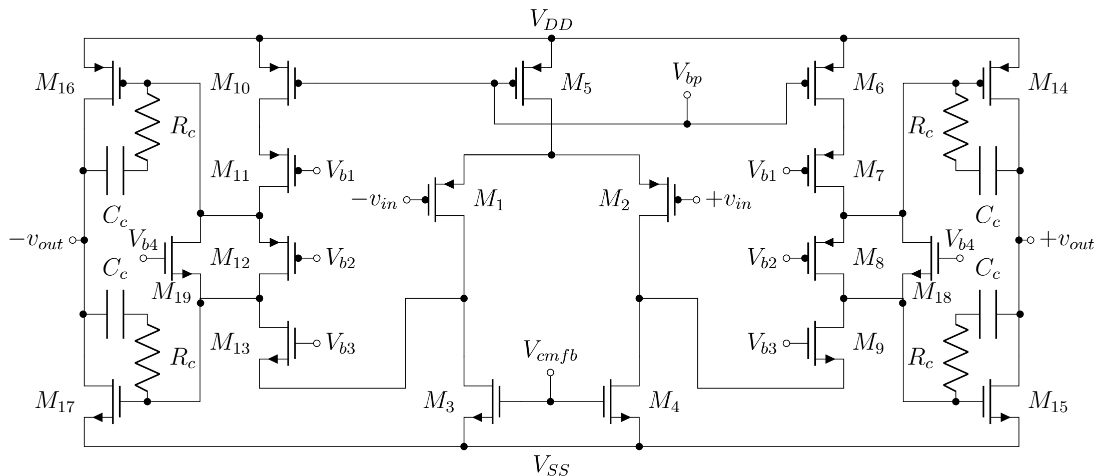


Figure 4.15: Multi-stage fully-Differential amplifier schematic

One drawback of the folded cascode operational amplifiers is the high number of biasing voltages required, which is translated into a complex biasing network. Based on the required voltages, a biasing circuit was designed as shown in figure 4.16.

In single ended amplifiers, the circuit in the feedback loop can set both, the common-mode (CM) and differential mode (DM) voltages. In differential feedback, the same rule can not be applied, as it is not capable of holding the CM (not enough gain). For that reason, fully-differential amplifiers require an external high-gain common-mode feedback circuit (CMFB) to set the output common-mode voltage (V_{cm}).

This CMFB loop should be able to keep the V_{cm} stable without influencing the differential mode signal (V_{dm}). In a broad way, a CMFB circuit averages both

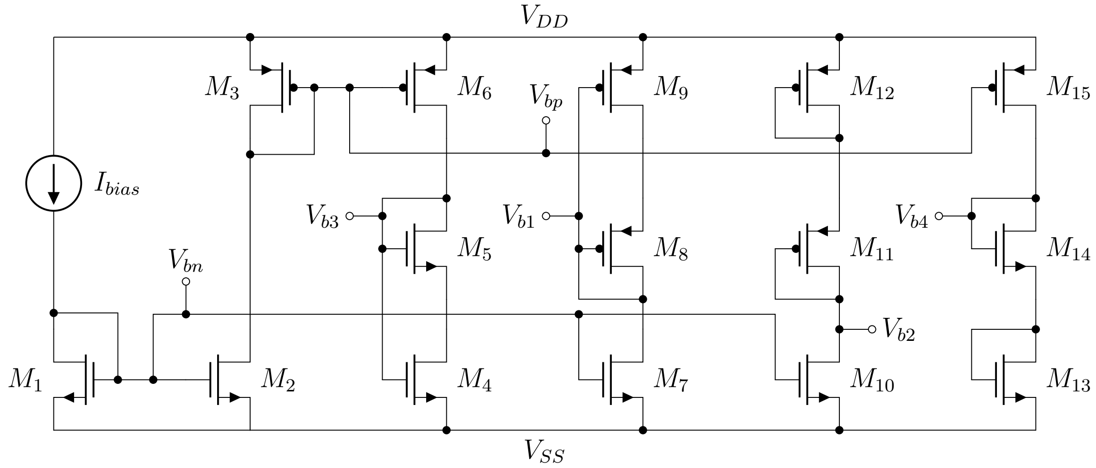


Figure 4.16: Biasing network schematic for the fully-differential amplifier.

differential output voltages ($+V_{out}$ and V_{out}) to produce a common mode voltage, V_{cmfbi}. It is then compared with the desired reference common-mode voltage, V_{cm}, usually equal to the average of the two power supplies, or analog ground. The difference between V_{cmfbi} and V_{cm} is amplified, and the resultant error is used to change the common-mode biasing voltage of the amplifier differential pair V_{cmfb}, forcing that way V_{cmfbi} and V_{cm} to be equal.

Different sensing and averaging techniques for CMFB circuits can be used, such as continuous time and switched capacitors approaches. In this work, the differential outputs are averaged using a resistor based voltage divider, and the error to the desired V_{cm} is sampled using a switched capacitor circuit (figure 4.17).

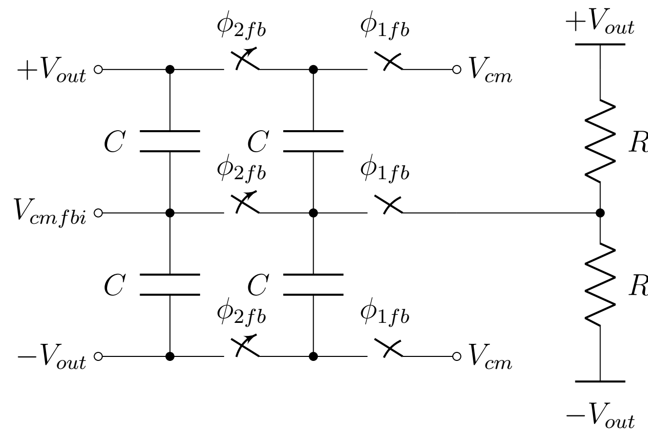


Figure 4.17: Switched capacitor common-mode feedback circuit for the fully-differential amplifier.

The resulting error voltage from the switched capacitor sampling circuit, V_{cmfbi},

is then amplified using the high-gain network shown in figure 4.18. This circuit defines the required biasing voltage, V_{cmfb}, to balance the differential pair of the feedback loop circuit, and therefore center the output on V_{cm}.

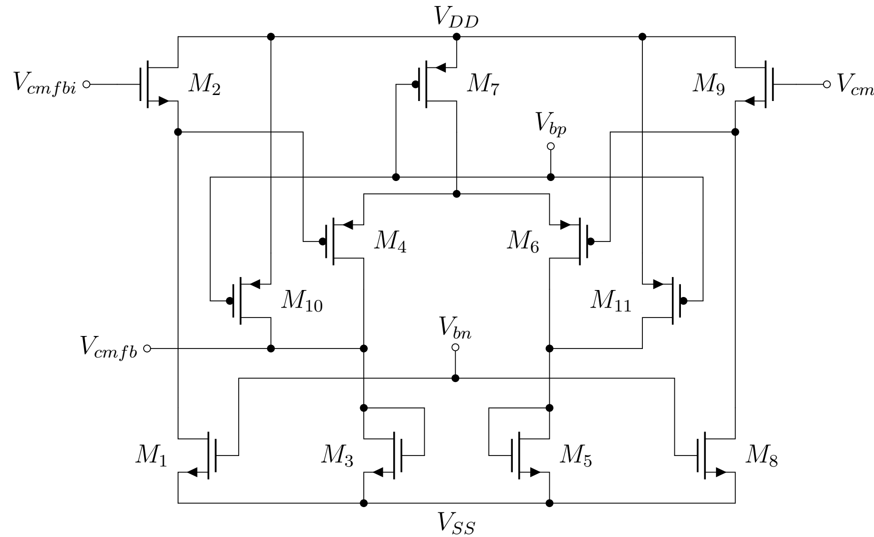


Figure 4.18: Common-mode feedback loop for the fully-differential amplifier.

The frequency response of the amplifier is presented in figure 4.19.

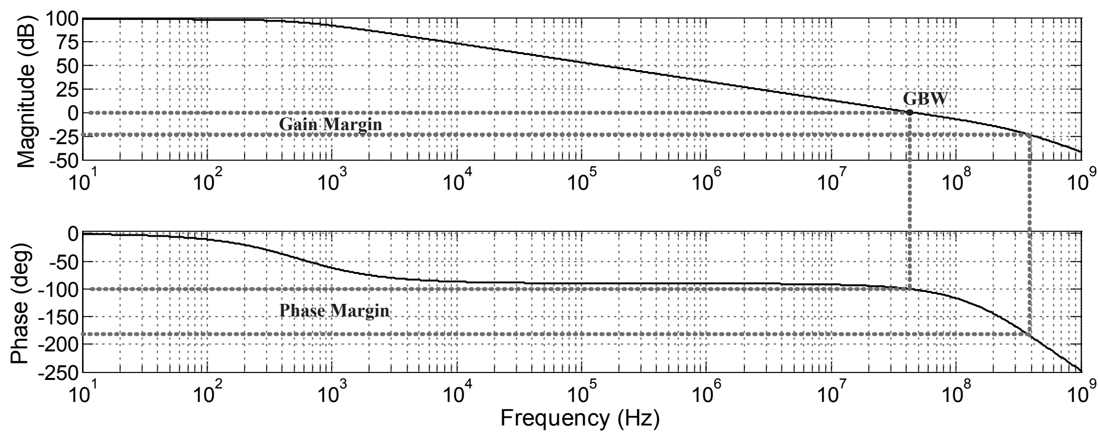


Figure 4.19: Bode diagram of the fully-differential amplifier.

Taking into account that the minimum input voltage amplitude used is $110mV$ and the operating frequency is 1MHz, aiming for the full output range, a 30dB gain is required (minimum GBW of 33MHz). The simulation results showed a 40MHz GBW, which satisfies the requirements, as well as a 78° phase margin that guarantees the amplifier stability.

With the intention of isolating the differential output of the CVC, two buffers were added to the output. Similarly to the excitation signal generation circuit,

a n-Channel and a p-Channel amplifiers were used, resulting in the circuit represented in figure 4.20. As the amplifiers used were already described, no further information is presented.

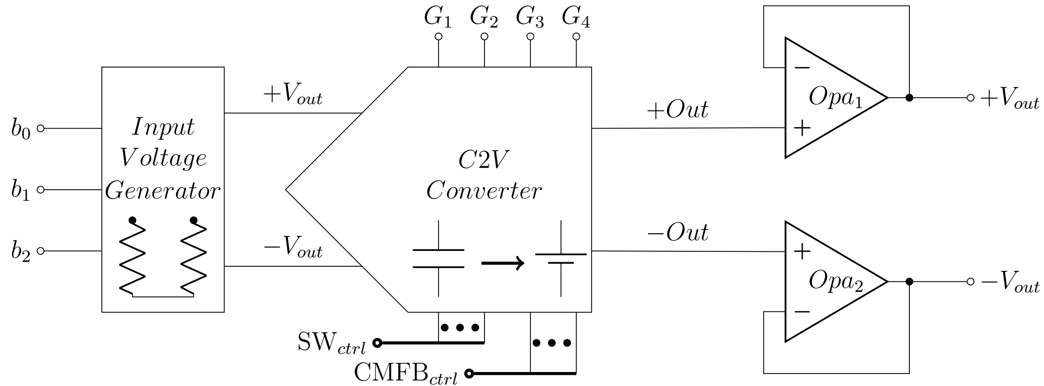


Figure 4.20: Overview of the capacitance-to-voltage (C2V) converter.

4.2.2 Control Signals Generation

Once the operating frequency of the switched capacitor capacitance-to-voltage converter is defined, a clock signal, at the desired frequency, needs to be generated. After generating the main clock, to guarantee that the charge is not inadvertently lost, the non-overlapping clock signals need to be produced, which are used to eliminate the clock feed-through influence [4.7, 4.8].

The full ASIC uses two different clock sources, one in the digital and another in the analog domain. The circuit has been designed in such a way that, the analog circuit, namely the CVC, is able to work without activating the digital control system (main state machine), i.e. the ASIC can operate as a purely analog circuit. Therefore, the default clock source, an analog ring oscillator that can be digitally disabled, while the 1MHz clock signal is switched to a digital source, as shown in figure 4.21.

Ring Oscillator

An oscillator is a circuit that produces a periodic output without requiring any input signal. This kind of circuit relies on the principle that, a system with a negative feedback may oscillate if the "Barkhausen criteria" is met ($|H(j\omega_0)| \geq 1$ and $\angle H(j\omega_0) = 180°$).

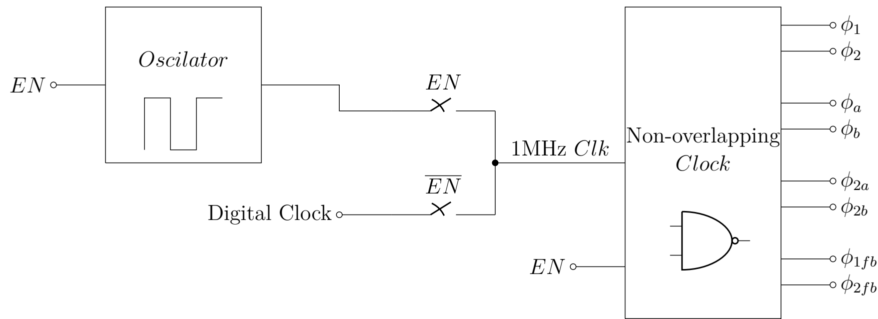


Figure 4.21: Overview of the control signals generation circuit.

A ring oscillator consists of several gain or delay stages in a loop. To meet the oscillation criteria, an odd number of inverting stages needs to be used, where the output of each stage is used as input for the next one. The last output is fed back to the first inverter. Due to the delay time of each stage, the whole circuit spontaneously starts oscillating at a certain frequency. The frequency f depends on the number of stages n and the delay contribution of each stage τ as follows:

$$f = \frac{1}{2n\tau}. \tag{4.8}$$

Given the stated conditions, a ring oscillator with 5 inverting stages and an enable signal was designed. The resulting schematic is depicted in figure 4.22. To increase the time constant of the oscillator, and therefore decrease the oscillation frequency, two capacitor stages have been added to the delay loop.

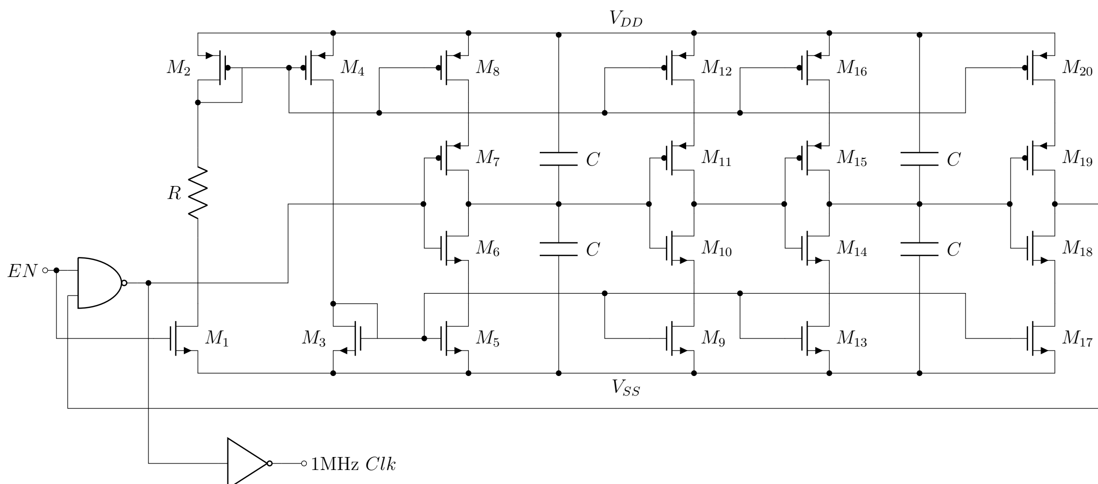


Figure 4.22: Ring oscillator schematic.

The proposed ring oscillator was simulated, and a 1MHz clock signal was achieved, as shown in the fft result on figure 4.23b.

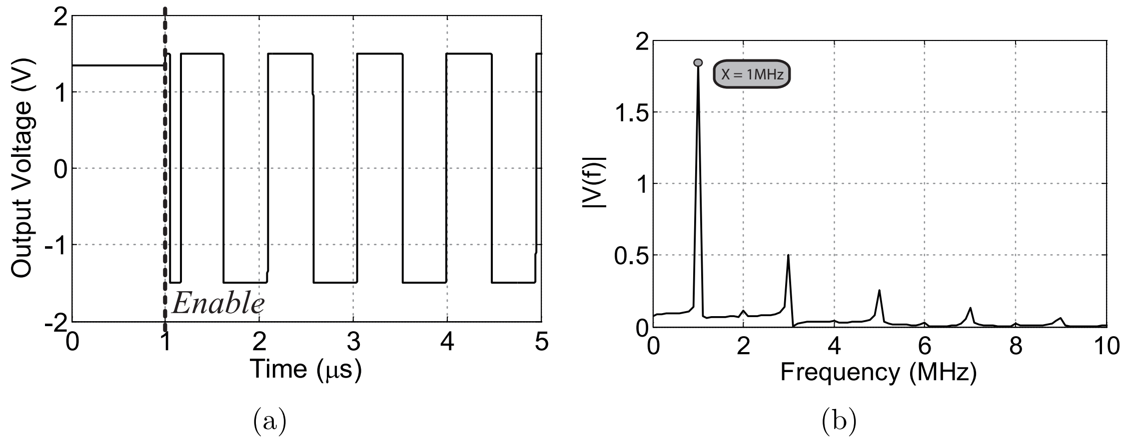


Figure 4.23: Simulation results of the ring oscillator. a) Output voltage. b) Output signal fft.

Non-Overlapping Clocks

A control circuit, based on CORELIB digital cells, was designed where two logic signals running at the same frequency, are delayed in such a way that at no time both signals are high. This circuit grounds it working principle on the delay that each digital cell adds to the signal (CORELIB cells are perfectly characterized [4.2]). Given the complexity of the circuit, the complete schematic is not presented here, but a simplified version, merely illustrative, of the adopted approach is depicted in figure 4.24.

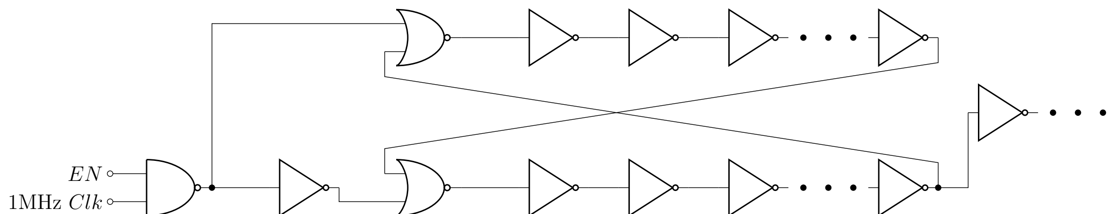


Figure 4.24: Non-overlapping clock generation circuit.

The control signals generation circuit was simulated, and the results are shown in figure 4.25.

The same 1MHz control signals are used for the common-mode feedback circuit of the fully differential amplifier, Φ_{1fb} and Φ_{2fb}, and for the CVC (Φ_1 and Φ_2). The signals named with number 1, are used to trigger the sample phase of the switched capacitor circuits, while the signal named as Φ_{2x} activate the amplifying phase. Each clock transition is performed $5ns$ before the other signal switches state.

The signals labeled with the letters a and b are 500kHz signals, used to select the

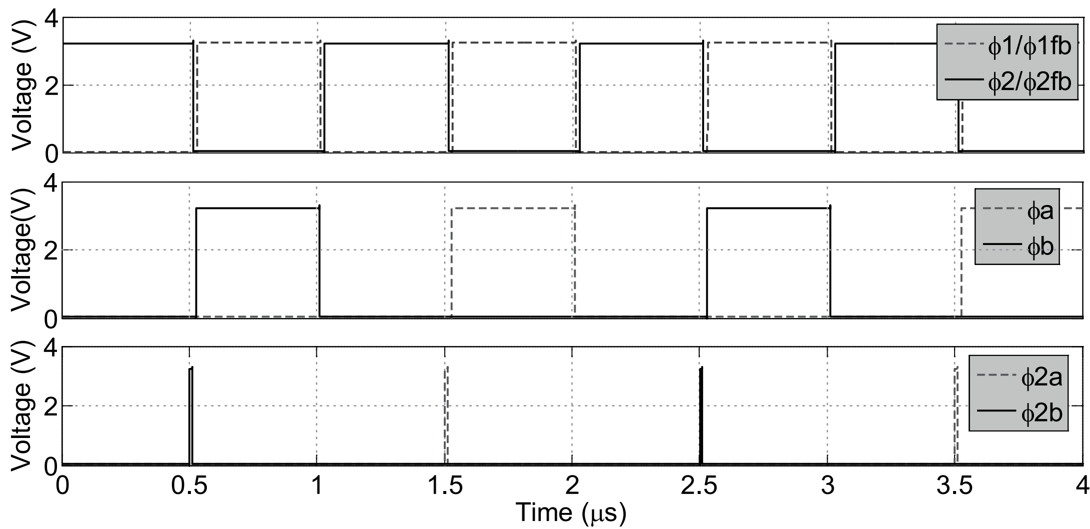


Figure 4.25: Simulation results of the non-overlapping clocks generation circuit.

input voltage, Φ_a and Φ_b, and to control the sample and hold circuit (Φ_{2a} and Φ_{2b}), as previously explained.

4.2.3 Pull-In Detection

Once the MEMS sensing capacitance is converted into a differential voltage signal, a mechanism capable of detecting the critical deflection needs to be implemented. This sub-circuit can be divided into three major blocks, namely the differential-to-single-ended converter, the analog comparators and the reference voltages generation circuit. A block diagram with the circuit overview is presented in figure 4.26.

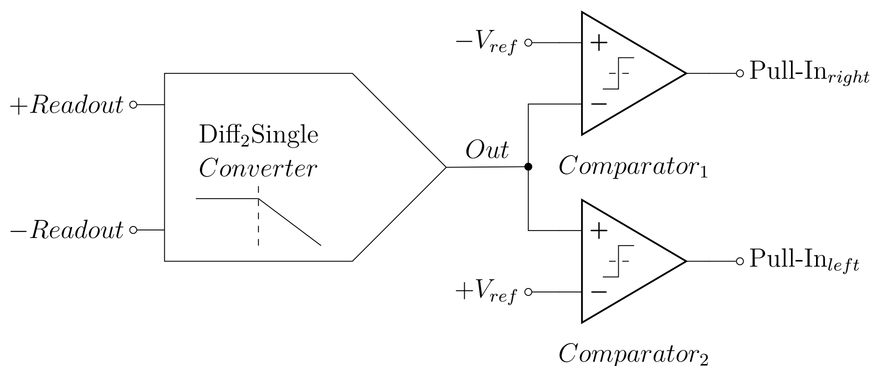


Figure 4.26: Overview of the pull-in detection mechanism.

Differential to single-ended converter

Considering that the switched capacitor CVC operating frequency can add out-of-band noise to the signal of interest, it is important to reduce that noise while removing common-mode errors. This can be achieved by designing an active low-pass filter with a cutoff frequency, at least, one decade lower than the CVC switching frequency.

This circuit, not only filters the required high frequency noise, but can also be used as a differential-to-single-ended converter. This is useful since single-ended analog comparators can be used to detect the pull-in, instead of using more complex differential comparators.

A 2-pole low-pass filter with differential input is used, as shown in figure 4.27. This type of circuit can be easily designed by applying the design equation for the well known multiple-feedback low-pass filter [4.9].

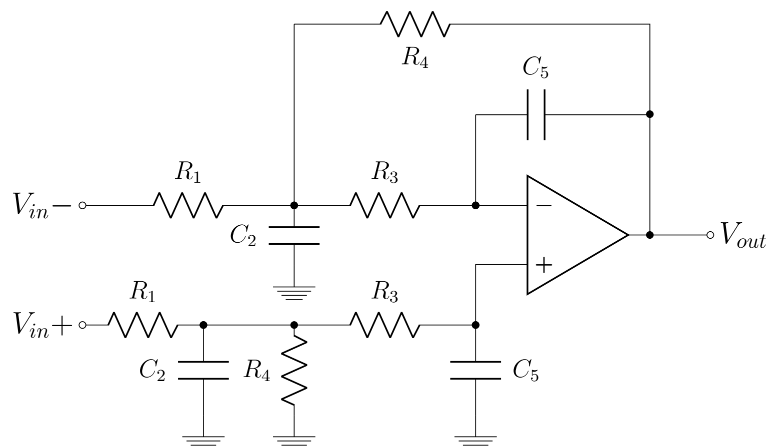


Figure 4.27: Two pole filter with differential input.

When converting the differential signal, it is imperative to recall that, in order to avoid signal saturation, the single-ended output needs to be half of the amplitude of the input signal, as the differential signal range is of $2 \times (V_{dd} - V_{ss})$. The AC response of the differential-input filter, using the previously designed operational amplifier with n-Channel input transistors, is presented in figure 4.28, where the -6dB pass band gain can be noticed. The filter was designed to have a corner frequency of 100kHz, since lowering much further this frequency would lead to larger chip area.

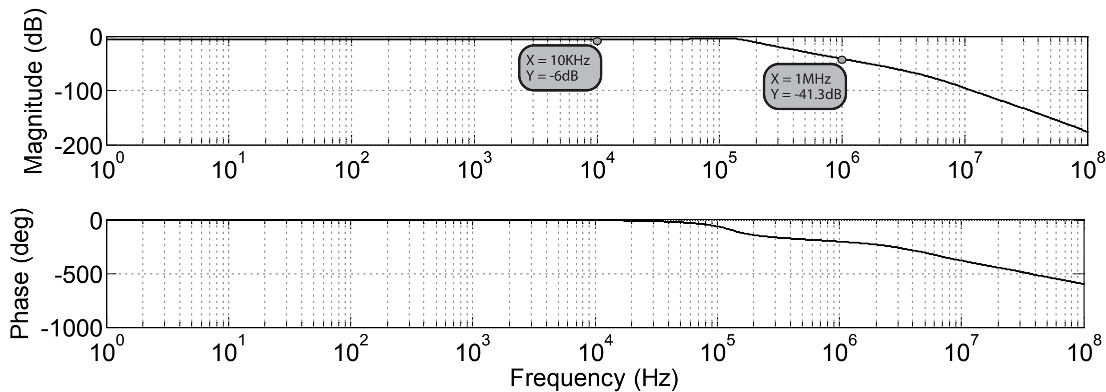


Figure 4.28: Bode diagram of the two pole low-pass filter.

Comparators

As shown in figure 4.26, the single-ended output of the low-pass filter is compared with two reference voltages that represent the pull-in critical deflection. Similarly to the excitation signal generation, a resistor-based voltage divider (figure 4.8) and a digital decoder, using CORELIB standard cells (figure 4.9) are used to select the comparison value.

In this case, the reference voltage can be selected from 16 different values, V_1-V_{16}, defined by the current flowing through the resistors, $I = \frac{V_{DD}-V_{SS}}{2\times30R}$. Considering $R = 6.67k\Omega$, a $8.25\mu A$ current is obtained. It means that the reference voltages ($+V_{ref}$ and $-V_{ref}$) range from $V_{cm} \pm 605mV$ to $V_{cm} \pm 1.43V$, with $55mV$ steps. A 4-16 decoder was designed to control both reference voltages with the same 4 control bits.

The generated references voltages are buffered using the same amplifier architectures as in the excitation signal generation circuit, resulting in the circuit represented in figure 4.29.

In what concerns the pull-in detection itself, since the reference voltages can go to values close to the power rails, two different comparator architectures were designed. For the lower reference voltage, $-V_{ref}$, a comparator with p-Channel transistors in the input stage is used ($Comparator_1$), while a n-Channel input comparator is used for the higher reference voltage, $+V_{ref}$ ($Comparator_2$).

Both comparators are based on a multi-stage comparator architecture (figure 4.30 and figure 4.31). The first stage, acts as a pre-amplifier that is used to obtain higher resolution. Even thought the output of this stage is larger than the comparator

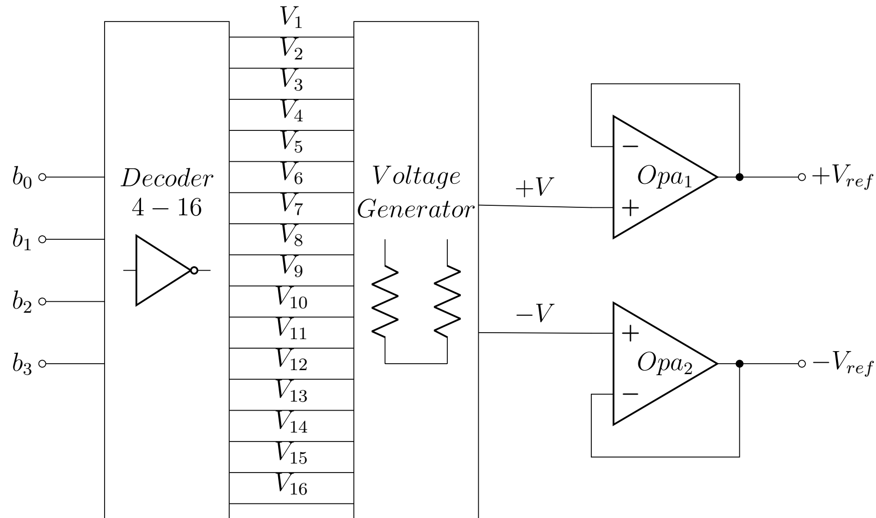


Figure 4.29: Reference voltage generation circuit.

input, it is still too small to trigger any digital circuitry. The output of this stage is then connected to a latched circuit, that works as the positive feedback for the last and main gain stage. Two digital inverters are added to the output, in order to increase the slew-rate of the output signal. As a summary, these comparators can be described as an unbalanced low-offset high-gain amplifier, that quickly switches between one of the power rails, depending on the input signals.

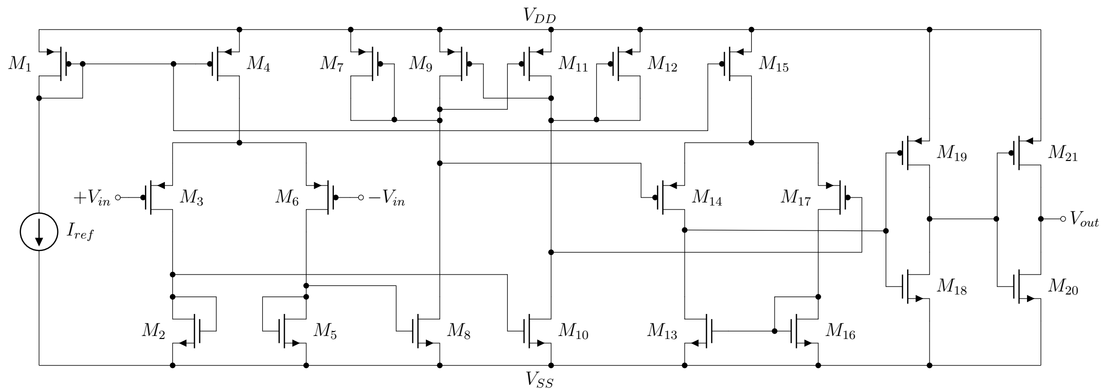


Figure 4.30: Comparator with p-Channel input stage.

Ideally, in a comparator with infinite open-loop gain, which corresponds to zero linear region, the output would switch from one saturation to the other, while crossing the reference voltage, $\pm V_{ref}$. In reality, the deviation from the comparison value is defined by the gain, as: $V_{out} = A(+V_{in} - V_{in})$. The voltage transfer characteristic of both comparators is shown in figure 4.32, where $+V_{ref} = 2V$ and $-V_{ref} = 1V$.

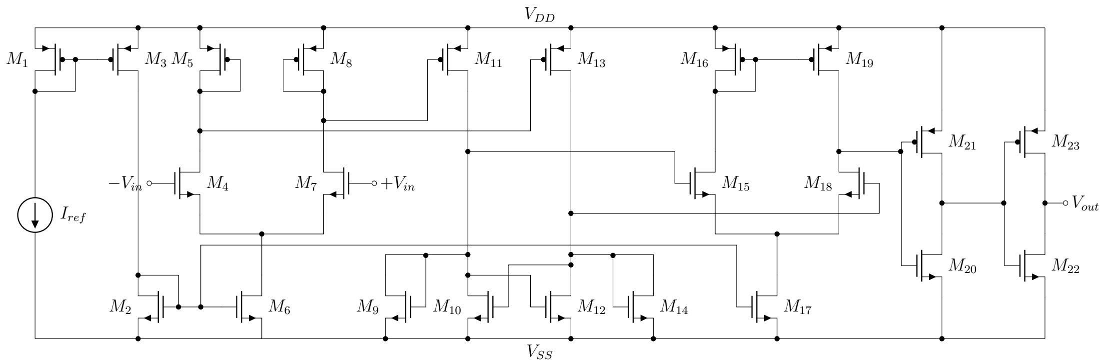


Figure 4.31: Comparator with n-Channel input stage.

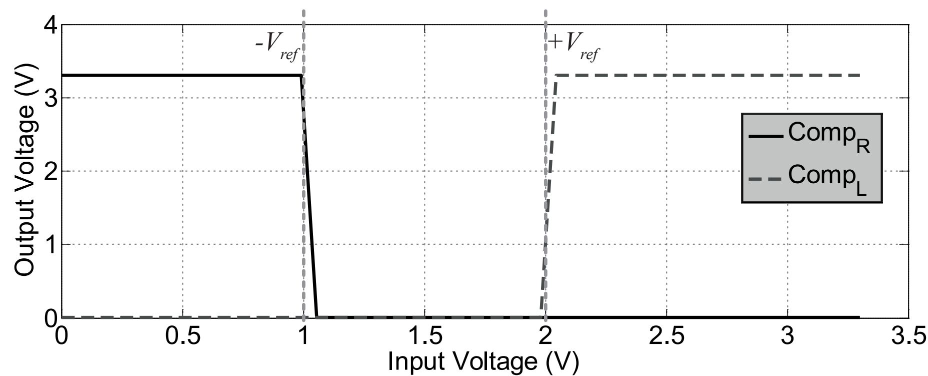


Figure 4.32: DC analysis of the designed comparators.

The high gain achieved on the comparators, reduces the voltage deviation to values smaller than $1mV$, as well as achieving high slew rate ($SR = 1V/100ps$, measured in the transient simulation). The complete pull-in detection mechanism was simulated using a triangular wave with $3.3V_{pp}$ as the differential input, and $-V_{ref} = 1V$ and $+V_{ref} = 2V$ as the reference voltages. The transient results are shown in figure 4.33.

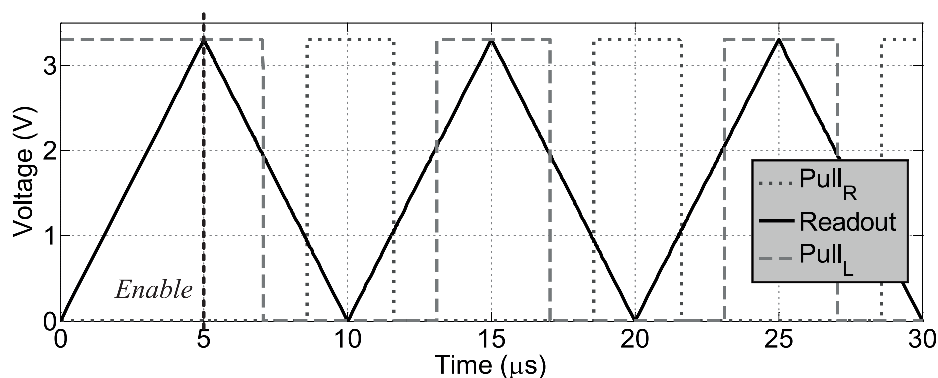


Figure 4.33: Transient analysis of the designed comparators with a triangular shape input signal.

4.2.4 Current Generator

Most of the above listed analog circuits incorporate a current reference signal. Such reference is a DC signal that should exhibit little dependence on power supply, process parameters and temperature, as it affects the voltage gain and noise of the biased circuits.

The design of these reference generation circuits usually faces two main problems: generating a supply-independent biasing circuit and the definition of the temperature variation. The first problem can easily be overcome by using a simple circuit that establishes a supply-independent current, such as the one of figure 4.34.

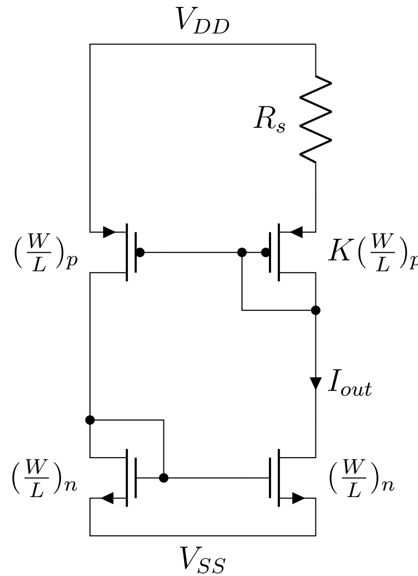


Figure 4.34: Circuit establishing supply-independent currents without body effect.

By neglecting the body effect, the resulting reference current can be expressed as:

$$I_{out} = \frac{2}{\mu_n C_{ox}(\frac{W}{L})_n} \times \frac{1}{{R_s}^2}\left(1 - \frac{1}{\sqrt{K}}\right)^2. \quad (4.9)$$

As expected, the output current is independent of the power supply, but still depends on the process and temperature. Usually, when this type of current generation circuits is made temperature-independent, since most process parameters fluctuate with temperature, it is process-independent as well.

The temperature-independent current generation circuits are based on the principle that, if two quantities with opposite temperature coefficients (TC) are added

with the correct weighting, a resulting TC equal to zero can be achieved. The fact that the bipolar transistors, available in semiconductor technologies, can provide well defined positive and negative TC, makes this kind of technology the core of temperature-independent reference circuits.

Considering a bipolar transistor, the base-emitter voltage exhibits a negative TC, as:

$$\frac{\partial V_{BE}}{\partial T} = \frac{V_{BE} - (4+m)V_T - \frac{E_g}{q}}{T}, \tag{4.10}$$

where $m \approx -\frac{3}{2}$, $E_g \approx 1.12eV$ (bandgap energy of silicon) and q is the charge of an electron.

A proportional to absolute temperature (PTAT) reference can be generated by using two bipolar transistors that operate at unequal current densities, figure 4.35, resulting in a base-emitter voltage difference proportional to the temperature.

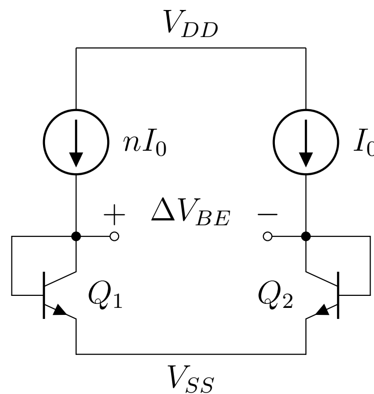


Figure 4.35: Generation of a PTAT voltage reference.

The V_{BE} difference temperature coefficient can be expressed as:

$$\frac{\partial \Delta V_{BE}}{\partial T} = \frac{k}{q} ln(n). \tag{4.11}$$

With the basic principles on generating positive and negative TC reference voltages listed above, a reference circuit with nominal zero TC can be developed. Different circuit architectures have been proposed as a way to generate a reference voltage, mostly based on the conceptual circuit present in figure 4.36.

The amplifier, A_1, senses V_X and V_Y while driving the top terminals of R_1 and R_2

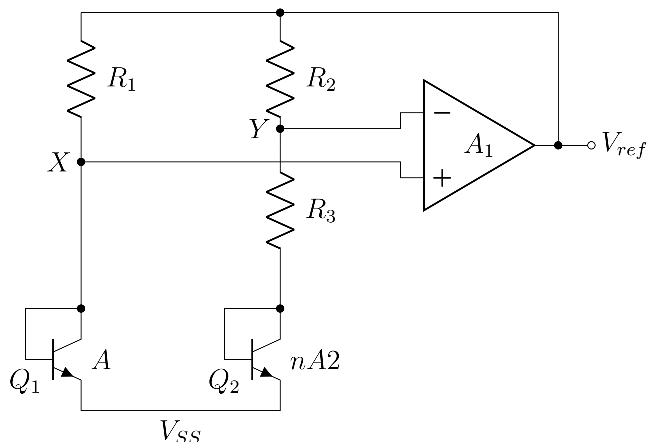


Figure 4.36: Conceptual generation of a temperature-independent reference voltage.

in a way that both voltages settle in equal values. The amplifier output is used as the reference voltage, which is equal to:

$$V_{ref} = V_{BE_2} + \Big(V_T ln(n)\Big)\Big(1 + \frac{R_2}{R_3}\Big). \tag{4.12}$$

For a zero TC, $1 + \frac{R_2}{R_3} ln(n) \approx 17.2$, which results in $V_{ref} \approx 1.25V$ [4.7].

Considering the compatibility with CMOS technology, *pnp* bipolar transistors can be formed in *n-well* processes. A p^+ region, inside the *n-well*, is used as the emitter, while the *n-well* itself is used as the base. The p-type substrate acts as the collector, which is connected to the most negative supply. For that reason, the presented conceptual circuits should be redrawn using *pnp* transistors.

Reference Generation

Based on the theory listed before, the term "bandgap reference" can be introduced. This type of nominally-zero TC reference voltage, is equal to the bandgap voltage of silicon ($V_{ref} = \frac{E_g}{q}$) when $T = 0$.

The architecture used for the reference voltage generation circuit is based on a low-voltage cascode current mirror that improves the supply rejection. The resulting bandgap circuit is shown in figure 4.37.

Since the designed bandgap is not a "self-biased" cascode, a biasing circuit needs to be used, in order to establish the voltages at nodes V_{b1} and V_{b2} (figure 4.38).

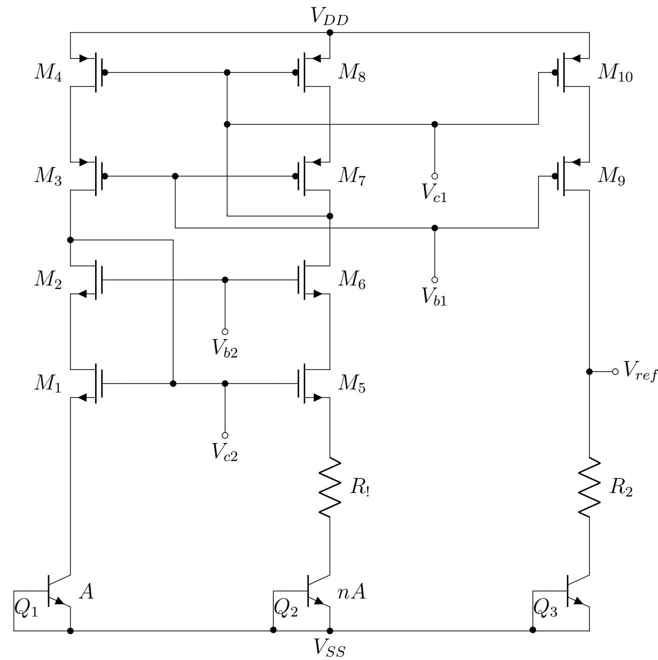


Figure 4.37: Schematic of the designed bandgap cirtuit.

The voltages at nodes V_{c1} and V_{c2} are secured by the cascode current mirror itself.

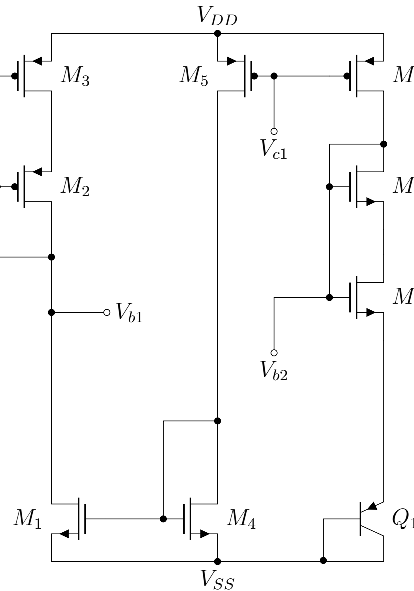


Figure 4.38: Bandgap biasing network.

Since during the start-up of the circuit, the state of the nodes in the bandgap are unknown, the circuit can remain in a meta-stable state without generating the required reference voltage. To avoid that, a start-up circuit can be used, figure 4.39, which will inject current on the critical nodes, until the bandgap output voltage, V_{ref}, reaches a minimum value ($V_{ref} > V_{th}[M_5]$).

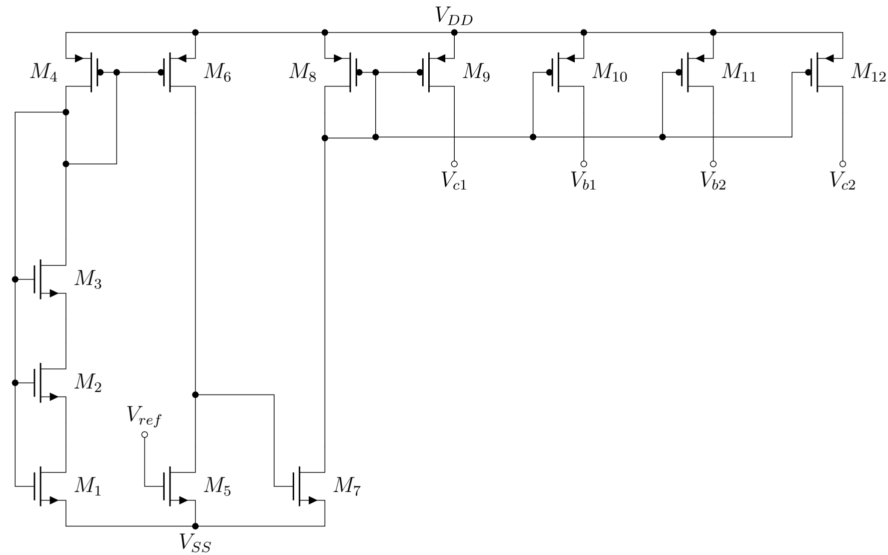


Figure 4.39: Bandgap start-up circuit.

The bandgap simulation results of figure 4.40, showes that in an operating temperature range of $150°C$ ($T = [-30°C; 120°C]$), a voltage drift smaller than 0.33% of the nominal value ($V_{ref} = 1.224V$) is achieved. The circuit was designed for a nominal operating temperature of $38°C$, which is expected to be close to the real conditions.

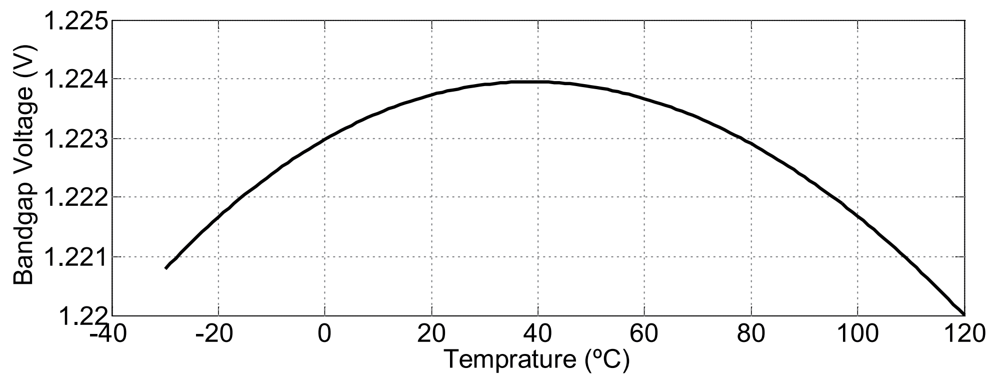


Figure 4.40: DC analysis of the bandgap for different temperatures ($T = -30°C$ to $120°C$).

Current Generation

The bandgap voltage reference needs to be converted into a current signal that will supply all the analog circuits. To isolate the bandgap, in order to avoid any overload on the bandgap output node, a self-biased buffer is used, before connection to a resistance load (figure 4.41).

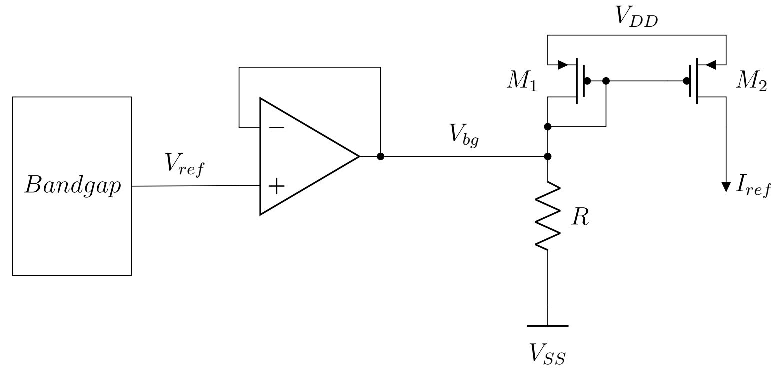


Figure 4.41: Current generation circuit.

The resultant current, I_{ref}, is defined by the resistor, R, and the aspect ratio of the current mirror, as:

$$I_{ref} = \left(\frac{V_{bg} - V_{SS}}{R}\right) \times \left(\frac{W_2/L_2}{W_1/L_1}\right). \tag{4.13}$$

Current Mirrors

The generated reference current is then mirrored to all the analog circuits. For added flexibility, there is the possibility of selecting the current value from four predefined values. To do so, as shown in figure 4.42, four current mirrors have been connected in parallel, using one control bit to enable each of the mirrors (b_0, b_1, b_2 and b_3).

The generated current is controlled by means of a logic circuit, based on digital cells, that generates the output signals according to table 4.3.

Table 4.3: Truth table of the control circuit.

Inputs			**Outputs**				
Enable	Select		Control Bits				Current
On	a_0	a_1	b_0	b_1	b_2	b_3	I_n
0	x	x	0	0	0	0	$0\mu A$
1	0	0	1	0	0	0	$5\mu A$
1	0	1	1	1	0	0	$10\mu A$
1	1	0	1	1	1	0	$12.5\mu A$
1	1	1	1	1	1	1	$15\mu A$

After designing and simulating each of the analog circuits, all the sub-circuits were interconnected and the circuit behavior was validated. An electrical model of the

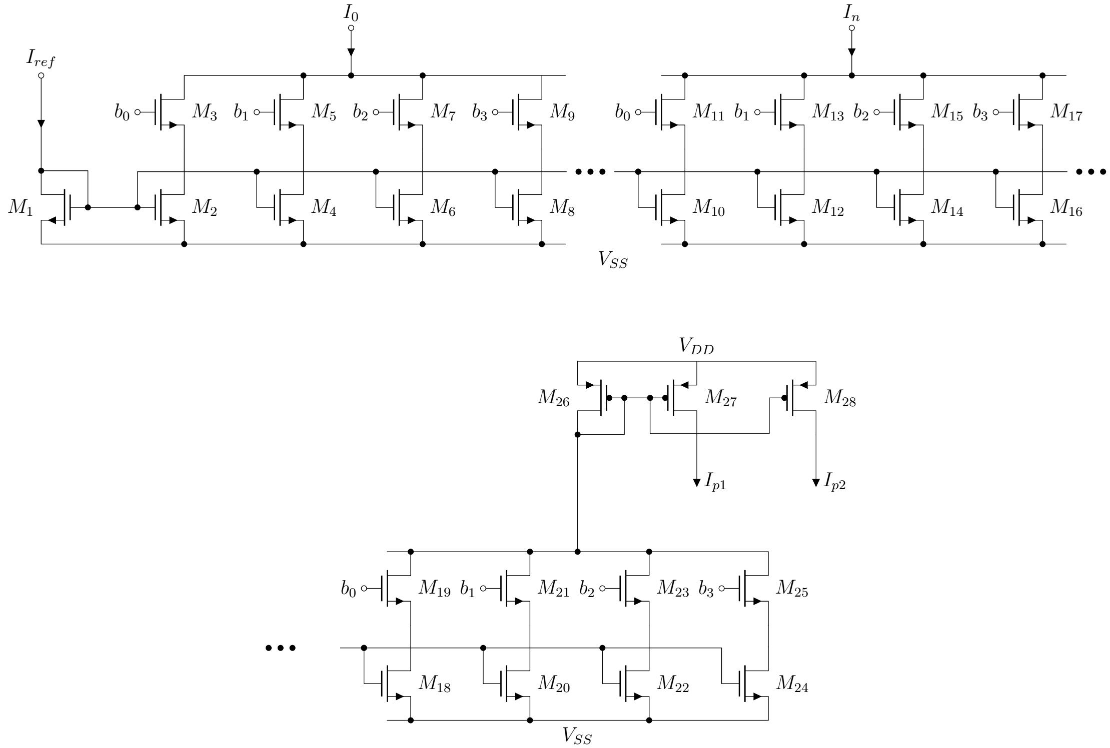


Figure 4.42: Current mirrors for the analog circuitry.

MEMS device was implemented (Lumped Model), as a way of correctly estimate the real behavior of the system.

In order to simplify the simulation process, two fixed capacitors were also used to simulate the MEMS sensing capacitance. One of these simulation results is shown in figure 4.43, where $1pF$ and $21pF$ were used as the right and left sensing capacitances. Theoretically, considering the input signal of $\pm 220mV$ and the feedback capacitor (defines the gain) of $2pF$, the output of the C2V is expected to be: $V = 220mV \times \frac{21pF - 1pf}{2pF} \times \frac{1}{2} = 1.1V + V_{cm}$.

The results of the transient simulation showed that, the theoretical output voltage is not achieved ($V_{simulation} = 2.43V < V_{theoretical} = 2.75V$). The difference is mainly due to the relation between the ON resistance of the switches and the sensing capacitances. Given the large capacitances to be measured, the time constant of the circuit can increase to values above the available charging time (500ns in each phase). In this case, the voltage at the capacitor may not charge completely to the input voltage, when the circuit switches to the next phase. Nevertheless, given the large capacitance change that characterizes the pull-in phenomenon, this is not critical for the application.

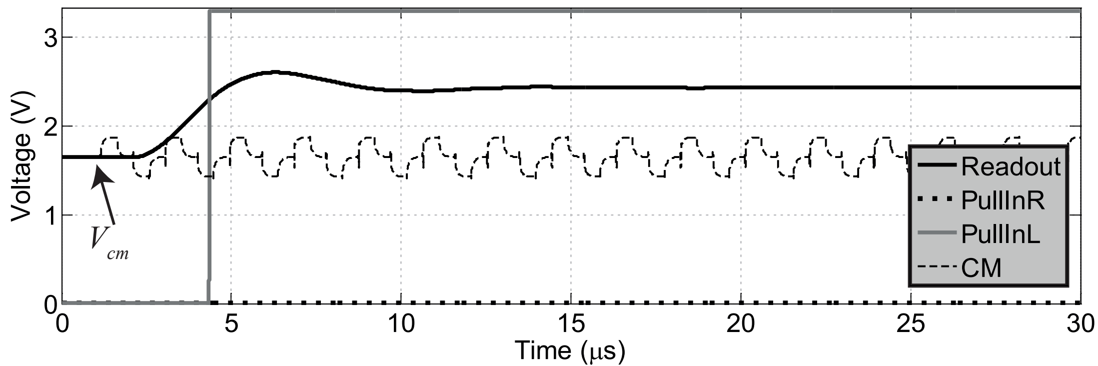


Figure 4.43: Transient simulation of the complete analog circuit (Supply current consumption of $2.2mA$ and $+V_{ref} = V_{cm} + 400mV$).

4.3 Digital Control

The sensor control system, performed in the digital domain, is responsible for setting the sensor working principle on the pull-in measurement. An overview on the ASIC digital circuit is presented in the block diagram of figure 4.44. As represented in the diagram, the system can be divided into five major subsystems: communications (I^{2}C (inter-integrated circuit) and SPI), actuation control (implements the actuation algorithm), the clock and reset unit, the register bank an the main finite state machine (FSM).

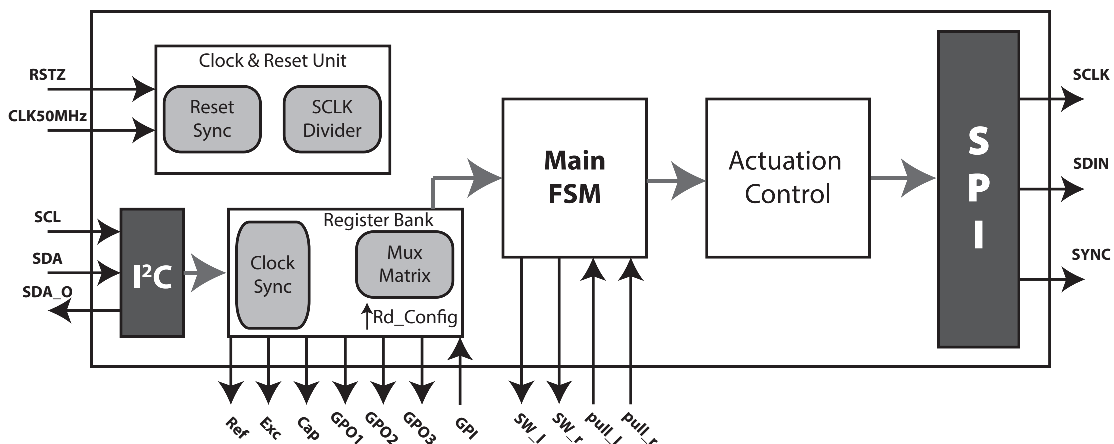


Figure 4.44: Digital architecture block diagram.

As a preparatory note, the system has been implemented using the digital standard cells from CORELIB and Verilog has been used as the hardware description language (HDL). A 50MHz clock signal was assumed.

4.3.1 Main FSM

The sensor operation is controlled by a main FSM. It is responsible for the control of the transition between left and right branches of the sensor (left and right pull-in measurements), as well as to control the inclinometer operation mode.

Taking in mind the working principle explained in chapter 2, different operation modes have been implemented. Since, in terms of electrostatic force, using positive or negative actuation voltages has the same effect ($F_{electrostatic} \propto V^2$), it is possible to use positive or negative ramp voltages, or even a combination of both. This is important as the sensor stability can be improved (section 2.3.2). The state machine is depicted in the diagram of figure 4.45.

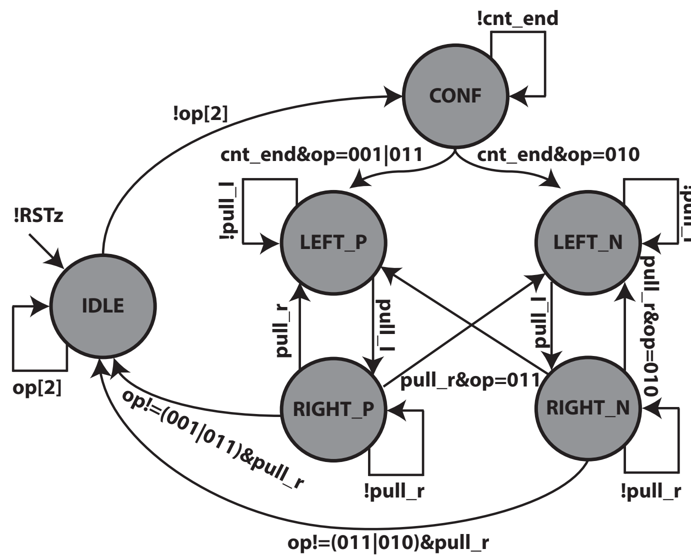


Figure 4.45: Diagram of the main finite state machine.

A summary of the main actions and possible transitions of each state is presented in table 4.4.

The sensor operation modes have been intuitively named as *Positive Ramps*, referring to pull-in measurement only using positive voltages, *Negative Ramps*, implying the use of only negative voltages. By *Positive and Negative Ramps*, it is suggested that both positive and negative voltages are alternately used for the pull-in measurement.

On the state name, the *Left* or *Right* words indicate on which branch of the sensor the pull-in voltage is being measured, while the letters *P* or *N* are used for positive

or negative ramp voltages. The signals from the analog comparators are refereed to as *pull_l* (left side comparator) and *pull_r* (right side comparator).

Table 4.4: Main FSM transitions and functions.

State Name	Next State	Condition	Action
IDLE	IDLE	!rstz|op[2]==1	This is the initial state. Right after the reset de-assertion, the FSM waits on this state until Start condition is configured. At any state, if reset is de-asserted, the FSM returns to IDLE immediately.
	CONF	op[2]==0	Once the Start configuration is detected and there is a valid configuration mode, the FSM transits to CONF state. This transition also triggers: **1-**An internal counter to start measuring the time spent in CONF state. **2-**Requests for the actuation block to send the DAC configuration command word and the conversion value stored in register Ext_DAC(1/2/3).
CONF	CONF	!cnt_end	FSM stays in this state until the counter reaches the configured time.
	LEFT_P	cnt_end&op[1:0] ==01|11	FSM transits to LEFT_P once the counter reaches the configuration time limit and if the operation mode is configured for Positive Ramps or Positive and Negative Ramps. This transition also triggers: **1-**Restarts the state counter value. **2-**Activates the left switch.
	LEFT_N	cnt_end&op[1:0] ==10	FSM transits to LEFT_N once the counter reaches the configuration time limit and if the operation mode is configured for Negative Ramps. This transition also triggers: **1-**Restarts the state counter value. **2-**Activates the left switch.
LEFT_P	LEFT_P	!pull_l&!timeout	FSM stays in this state while the left pull-in signal is not detected.[1]
	RIGHT_P	pull_l|timeout	Once the pull-in signal is detected, or state counter reaches the time out values, the FSM changes to the right branch state, RIGHT_P. This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**Activates the right switch, de-activates the left switch.
RIGHT_P	RIGHT_P	!pull_r&!timeout	FSM stays in this state while the right pull-in signal is not detected.[1]
	LEFT_P	(pull_r|timeout) &op==001	Once the pull-in signal is detected, or state counter reaches the time out values, and the operation mode is Positive Ramps, the FSM changes to the left branch state, LEFT_P . This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**Activates the left switch, de-activates the right switch.

	LEFT_N	(pull_r|timeout) &op==011	Once the pull-in signal is detected, or state counter reaches the time out values, and the operation mode is Positive and Negative Ramps, the FSM changes to the left branch state, LEFT_N. This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**Activates the left switch, de-activates the right switch.
	IDLE	pull_r|timeout	Once the pull-in signal is detected, or state counter reaches the time out values, the FSM changes to the IDLE state if there is no working operation mode. This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**De-activates the switches.
LEFT_N	LEFT_N	!pull_l&!timeout	FSM stays in this state while the left pull-in signal is not detected.[1]
	RIGHT_N	pull_l|timeout	Once the pull-in signal is detected, or state counter reaches the time out values, the FSM changes to the right branch state, RIGHT_N. This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**Activates the right switch, de-activates the left switch.
RIGHT_N	RIGHT_N	!pull_r&!timeout	FSM stays in this state while the right pull-in signal is not detected.[1]
	LEFT_N	(pull_r|timeout) &op==010	Once the pull-in signal is detected, or state counter reaches the time out values, and the operation mode is Negative Ramps, the FSM changes to the left branch state, LEFT_N. This transition also triggers: **1-**Stores the last DAC applied value in a specific register. **2-**Restarts the state counter value. **3-**Activates the left switch, de-activates the right switch.
	LEFT_P	(pull_r|timeout) &op==011	Once the pull-in signal is detected, or state counter reaches the time out values, and the operation mode is Positive and Negative Ramps, the FSM changes to the left branch state, LEFT_N. This transition also triggers: 1-Stores the last DAC applied value in a specific register. 2-Restarts the state counter value. 3-Activates the left switch, de-activates the right switch.
	IDLE	pull_r|timeout	Once the pull-in signal is detected, or state counter reaches the time out values, the FSM changes to the IDLE state if there is no working operation mode. This transition also triggers: 1-Stores the last DAC applied value in a specific register. 2-Restarts the state counter value. 3-De-activates the switches.

[1] **-**During this state, the state counter is being incremented as well. If the state counter reaches the timeout period, before the pull-signal is detected, the FSM leaves this state.

4.3.2 Actuation Control

This block is responsible for generating the DAC values that need to be transmitted to the device at a given time, according to the previously described actuation algorithm. The main function of the actuation control system is defined by the state machine of figure 4.46.

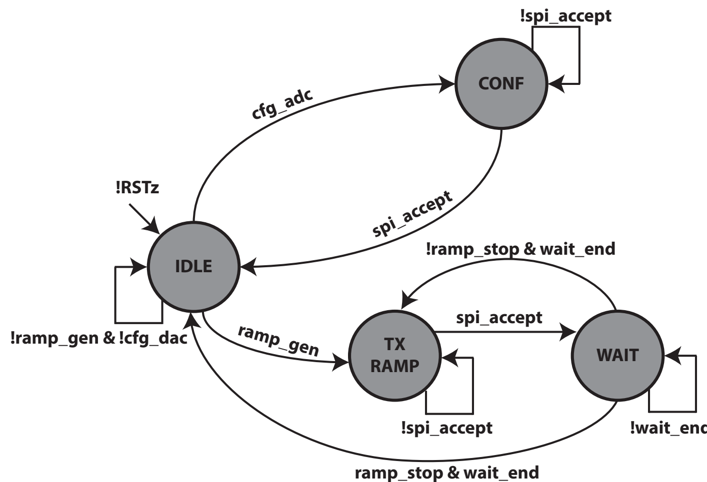


Figure 4.46: Diagram of the actuation system FSM.

An overview on the main actions in this FSM is presented in table 4.5.

Table 4.5: DAC actuation FSM transitions and functions.

State Name	Next State	Condition	Action
IDLE	IDLE	!rstz|!ramp_gen |!cfg_dac	This state is the initial state. Right after the reset de-assertion, the FSM waits on this state until it receives a request to configure the DAC, cfg_dac, or to generate a ramp, ramp_gen. At any state, if reset is de-asserted the FSM returns to IDLE immediately.
	CONF	cfg_dac	When a request to configure the DAC is made, the FSM transits to CONF state.
	TXRAMP	ramp_gen	When a request to generate a ramp voltage is made, the FSM transits to TXRAMP state.
CONF	CONF	!spi_accept	The FSM holds in this state while the SPI block does not informs that it accepted the transmission of the Command Word followed by the DAC initial value.
	IDLE	spi_accept	Once the SPI accepts transmission of the DAC value, the FSM returns to IDLE state.
TXRAMP	TXRAMP	!spi_accept	The FSM holds in this state while the SPI block does not informs that it accepted the transmission of the DAC value.
	WAIT	spi_accept	Once the SPI accepts transmission of the DAC value, the FSM transits to WAIT state.

WAIT	WAIT	!wait_end	FSM holds in this state until the Wait timeout counter does not expires.
	TXRAMP	!ramp_stop &wait_end	If there is no Ramp Stop request received and if the Wait timeout counter expired, the FSM transits to TXRAMP state, in order to transmit another DAC value.
	IDLE	ramp_stop &wait_end	If there is a request to Stop the Ramp generation and the Wait timeout counter expired, jump to IDLE state and wait for further requests.

The DAC configuration function, requests the SPI transmission of the DAC values stored in registers, Ext_DAC(1/2/3). This is used during the configuration state of the main FSM block. These values are pre-loaded to the DAC, so that it is stable before leaving the configuration state. Note that configuration state needs to have a timeout value specified, such that in the worst case scenario, for the SPI transmission lower speed clock, 5MHz, it is still possible to transmit the DAC value before the timer expires.

Ramp generation function, produces the values of a variable slope ramp that is requested to be transmitted to the DAC. The values are calculated according to the following algorithm:

1. Between 0 and 99,167% of the previous value ⇒ slope = 1000 LSB per transmission.

2. Between 99,168% and 99,833% of the previous value ⇒ slope = 600 LSB per transmission.

3. Between 99,834% and 99,983% of the previous value ⇒ slope = 100 LSB per transmission.

4. Between 99,984% and 99,997% of the previous value ⇒ slope = 10 LSB per transmission.

5. Between 99,998% and 100% of the previous value ⇒ slope = 1 LSB per transmission.

6. A ramp can be generated as a positive ramp or a negative ramp. Calculation of the ramp values are the same, with the exception that for the negative ramp, the increments are subtracted instead of added.

7. Every ramp generation starts from the previously determined value, sub-

tracted of value 0x199A. In case of a negative ramp the generation starts from the last value added of value 0x199A.

The actuation block imposes a latency between the transmission of a new value, through the SPI interface, and the actuation on the external switch. Such value is a parameter on the RTL code and cannot be configured. The parameter is set to wait 8 clock cycles (1MHz Clk) before the switch is activated. The reason for this delay is to guarantee that the output voltage, representative of the new value, is stabilized at the DAC output before the switch is activated. The diagram of figure 4.47 depicts the latency of the switch activation.

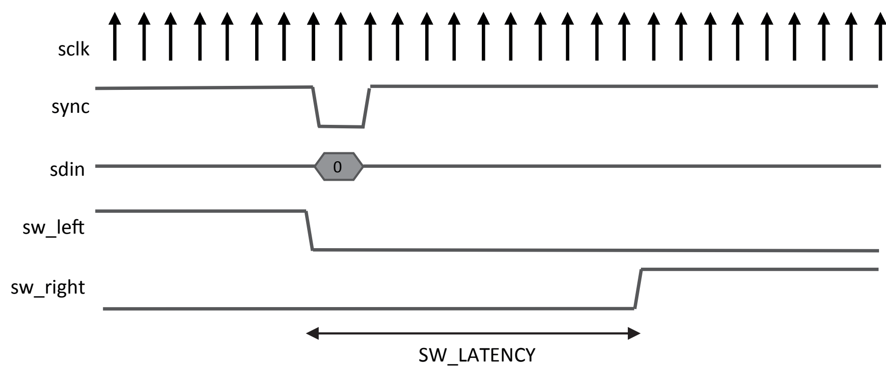


Figure 4.47: Switch latency, timing representation (SW_LATENCY represents around $8\mu s$).

4.3.3 Clock and Reset

A block is responsible for the generating internal divided clock signals inside the Controller. This block is also responsible for synchronizing the reset signal coming from the input port and synchronizing it to the clk50MHz domain.

The reset synchronization scheme is depicted in the diagram of figure 4.48.

The clock division is performed using a 6 bit counter that, cyclically counts until the value 50. The clock source is assumed to be a 50MHz clock signal. During the period of 50 clock cycles, four clock signals at different frequencies are generated (25MHz, 10MHz, 5MHz and 1MHz), as depicted in figure 4.49. The 1MHz clock is routed to the output port clk1mhz (used by the analog circuit), while the others are used as the SPI clock. The selection of which clock is routed, depends on the configuration held in register Ext_DAC_3[7:6].

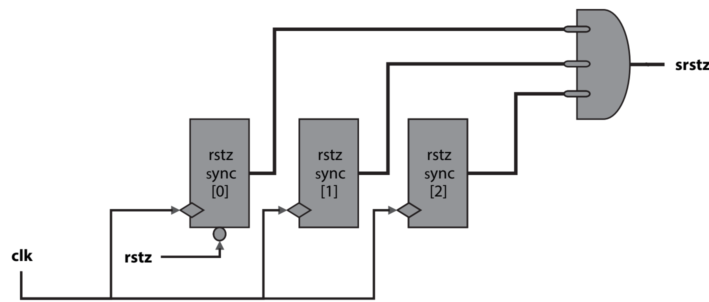


Figure 4.48: Reset synchronisation scheme.

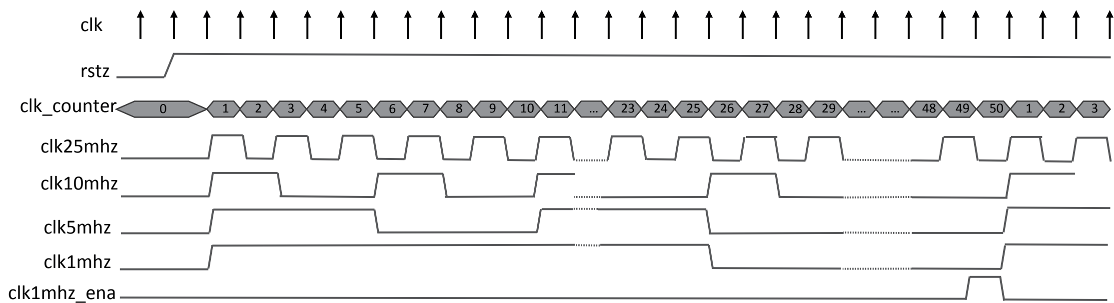


Figure 4.49: Timing representation od the devided clocks.

Additionally, an 1MHz pulse is generated, clk1mhz_ena, used internally to count waiting periods. Given that this is the lowest frequency being generated, it allows lower width counter registers to measure large periods of time.

4.3.4 Serial Communications

In the designed ASIC, both I^{2}C and SPI digital communications are available. In SPI communication the device operates as master to control the external DAC, while in the I^{2}C communication, the device operates as a slave.

SPI

The SPI communication is controlled by one hardware block, that implements a serial connection with two different write operations, write command and write data.

When write command is requested, the block uses the register bank information to build a 24-bit command word to be transmitted. Table 4.6 shows how the 24-bit command is build.

Table 4.6: SPI command word assignment.

Command Bits	**[23]**	**[22:20]**	**[19:6]**	**[5:3]**	**[2:1]**	**[0]**
Assigned value	1'b0	gpo3[7:5]	14'd0	gpo2[7:5]	gpo0[7:6]	1'b0

When "write data" is requested, the block receives the data to transmit and holds it at the input bus until the request is accepted. If the SPI block is not currently transmitting a value, it accepts the value by lowering the "sync" signal. At this point, it stores the value held at the input for transmission inside a 24-bit width shift register. Considering the 20-bit data length, the extra 4 bits will contain the address content (in accordance with the DAC specifications). Once the value is latched to the shift register, the 4 MSBits are filled with value 4'b0001 (this code represents a write operation on the DAC) [4.3]. Once the SPI block accepts the new value for transmission, the input request pin to send data can be lowered. At this point the SPI block will transmit the totality of the serial data autonomously.

I^{2}C

The I^{2}C serial protocol is used to communicate with the device, namely to configure and read the sensor output. This device conforms to the UM10204 I^{2}C-Bus Specification and User Manual, Rev. 06-4 April 2014, available from NXP Semiconductor, supporting (100 kHz) and fast (400 kHz) data transfer modes [4.10], therefore no further detail is given on this topic.

Due to communication speed constraints, the maximum output data rate when using 400 kHz I^{2}C is 10 kHz, and scales linearly with a change in the I^{2}C communication speed. For example, using I^{2}C at 100 kHz would limit the maximum output data rate (ODR) to 2500 Hz. Considering the low operating frequency of the sensor, this is not a limitation.

4.3.5 Register Bank

Basically, the register bank, is where the ASIC information is stored. As a safety measure, some of the registers can be modified during the controller normal operation, while others (quasi-static) can only be modified while the controller is not yet awake.

The only registers that are not considered to be quasi-static, are the ones were

the pull-in voltages are stored (updated upon a read request), the one that defines the operation mode and the wake-up one, that triggers the main FSM start condition. The general propose output and input registers (GPO and GPI), used to enable/disable the analog circuits, can also be modified anytime.

On the other hand, registers where the analog circuits configurations are stored, specifically the excitation signal amplitude, the comparators reference voltage, the CVC gain and the organization of the information to be read, can only be modified when the wake-up signal is not set.

Read Mux Mesh

The mux matrix block is responsible for organizing the DAC read data values (corresponding to the pull-in voltage values) in the disposed formats configured through register Rd_Config[2:0]. It re-organizes the data in such a way that, the I^2C slave mechanism does not need to do any additional function, besides reading sequentially the information on the register bank.

It is also responsible for detecting the I^2C request for reading the DAC data, at which point it will store the current values held by the controller, avoiding the scenario of changing values during the reading process. The registers holding the DAC measurements are stored in the controller, and only get updated on the register bank once the I^2C request to read them is once more triggered. It means, once this block detects that the I^2C master accessed register Left_1, 0x0F, for reading purposes, it triggers the storage of the DAC measurements.

4.4 MEMS & ASIC Integration

Due to its simplicity, in the overview of the readout circuit implementation presented here, there is no reference to the power-down additional circuitry on each analog block. Despite that, they have been implemented, as this kind of circuit can highly reduce the overall power consumption of the device, by disabling any unused analog circuit.

The readout circuit, both analog and digital, was fabricated in the AMS $0.35\mu m$ CMOS process [4.2]. A picture of the fabricated device is presented in figure 4.50, which has a die size of $2180\mu m \times 1780\mu m$. The supply current for analog circuits

was measured to be $2.5mA$. In power-down mode, the supply current is measured to be less than $20\mu A$.

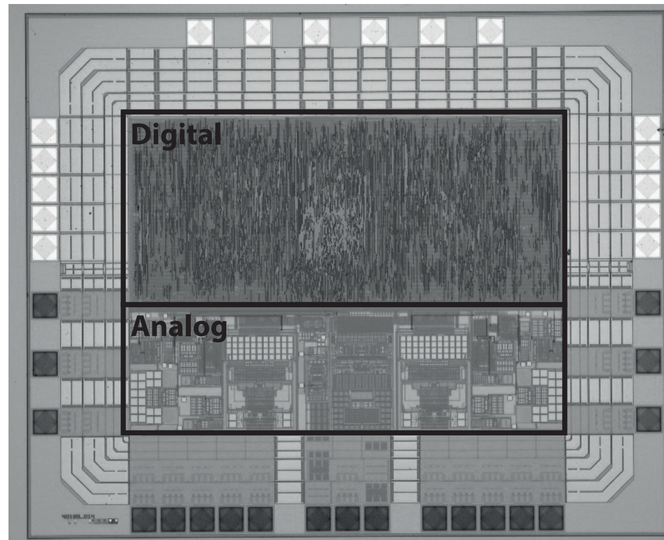


Figure 4.50: Microscopic image of the fabricated ASIC.

The concepts discussed in section 1.1.3 showed that, the integration of the MEMS sensing element with the fabricated ASIC can be performed at different levels, particularly at board level, chip level and wafer level. Since the MEMS device and the CMOS circuit were not fabricated on a monolithic process, neither any wafer bonding technique has been used, only board level and chip level integration remain as a possibility.

After all, achieving a high integration grade on the sensor has been pointed as a deeply desirable characteristic. Accordingly, wafer level integration has been used. A representation of the sensor integration is presented in figure 4.51.

The result of the integration process is shown in figure 4.52. Smaller size sensors can be accomplished by decreasing the carrier cavity area, as currently the carrier is clearely larger than required.

4.5 Conclusions

A synopsis on the sensor's implementation has been presented in this chapter. The description was divided in three main components, MEMS sensing element, analog circuit and digital control circuit.

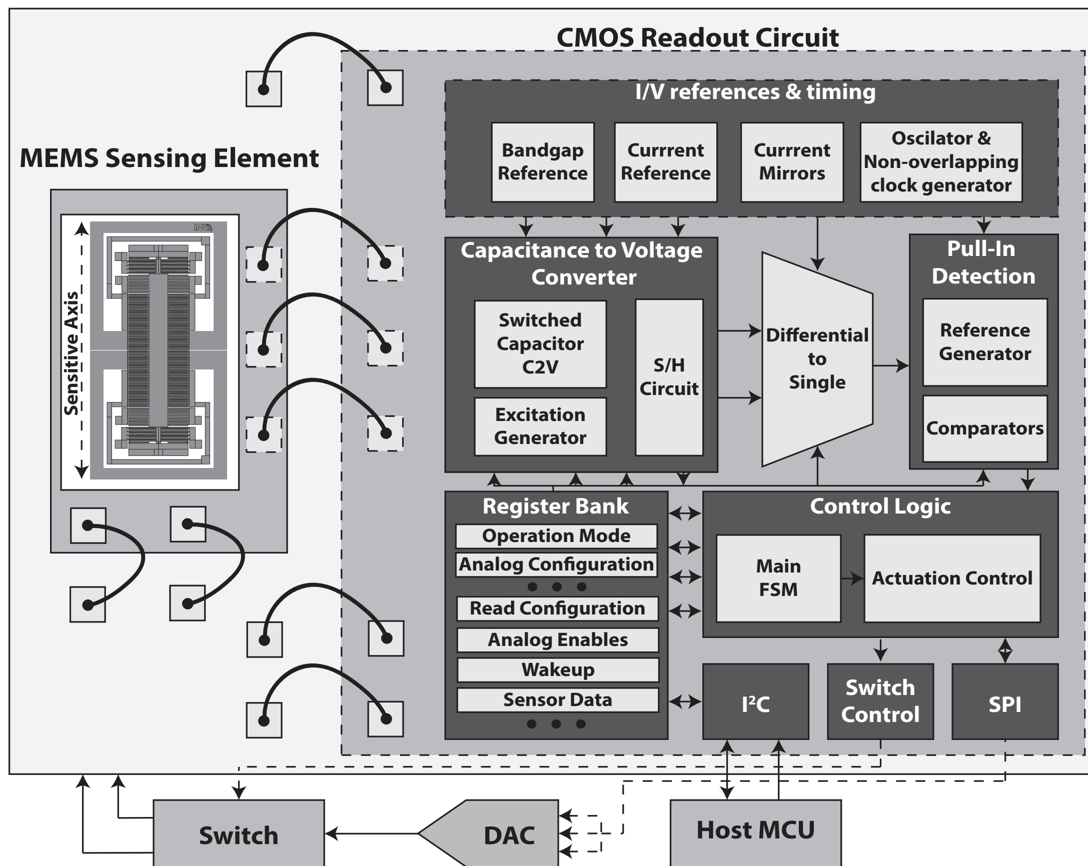


Figure 4.51: Block diagram of the sensor integration. MCU stands for the micro-controller unit.

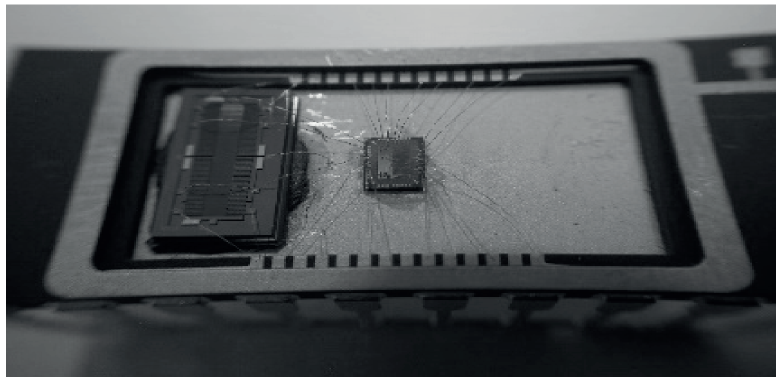


Figure 4.52: Picture of the final integrated sensor, using MEMS device #4.

The major design and fabrication challenges of the different parallel-plate MEMS device was presented in section 4.1. Each one of those devices, can contribute to the sensor with particular attributes. Devices #1 and #2 can be used to maximize the resolution, while with structure #3 higher dynamic range and bandwidth can be achieved. The simplicity of the device #4 fabrication process can be seen as a

major advantage. All the referred structures have been tested, and the fundamental results are going to be presented in the next chapter.

Section 4.2 gives the basic information on the analog circuit development. The main features of the ASIC, implemented in the digital domain, are presented in section 4.3.

During the whole chapter, the sensor has been referred to as a single-axis inclinometer. In reality, even though not used in this work, the ASIC has been designed in such a way that, a dual-axis configuration can be used. The digital control logic and the analog circuitry were duplicated, excluding the bandgap reference and the non-overlapping clock generation. The same I^{2}C serial communication and register bank are used for both axis.

A conceptual scheme of the 2-axis inclinometer configuration is depicted in figure 4.53.

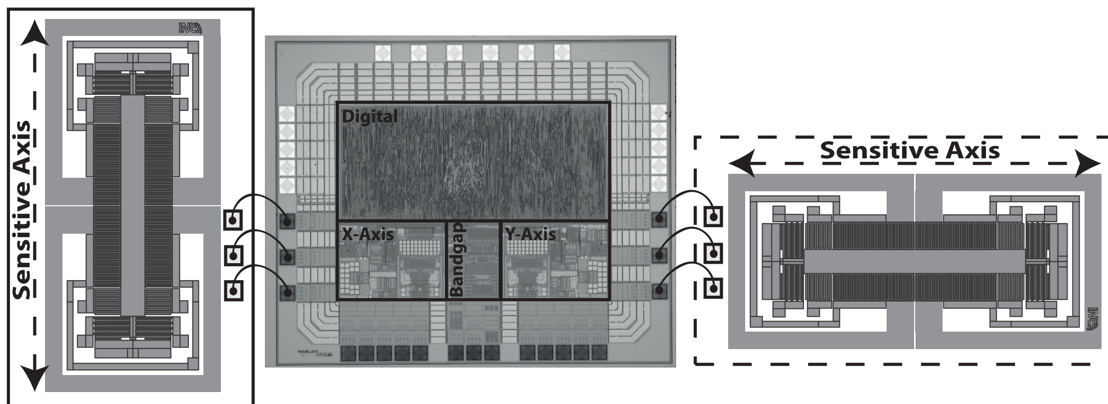


Figure 4.53: Diagram of the 2-axis sensor configuration, using the designed ASIC.

References

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5

Experimental Results

A promising approach for the realization of a high-resolution inclinometer is proposed here. By repeatedly bringing the microstructure to pull-in, while measuring the pull-in voltage (chapter 2), allows the measurement of the sensor tilt angle. As the pull-in point is characterized by a large change on the structure sensing capacitance, low requirements for the capacitive readout circuit are required. The non-mechanical noise is set primarily by the resolution of the actuation system (which can be made very high using a high-resolution DAC), and therefore, the main noise source is the structure mechanical-thermal noise [5.1].

In this chapter, the pull-in voltage based sensor prototypes are experimentally tested. The main focus is on the experimental validation of the proposed sensor architecture, using the different fabricated MEMS devices, but a performance evaluation of the designed ASIC, in terms of the differential input capacitance, is also presented.

The main experimental results include a long term analysis using data from almost 3 months. The sensor thermal stability is investigated and compensation mechanisms are tested [5.2]. An additional source of uncertainty is the charge accumulation on electrolytically actuated parallel-plate devices (section 2.3.2) [5.3,5.4].

The effect of consecutive measurements on the pull-in voltage is explored, including methodologies that can be used to minimize these charge effects. The previously presented performance comparison between differential capacitance direct transduction and the pull-in based approach is also experimentally supported here.

5.1 Measurement Setup

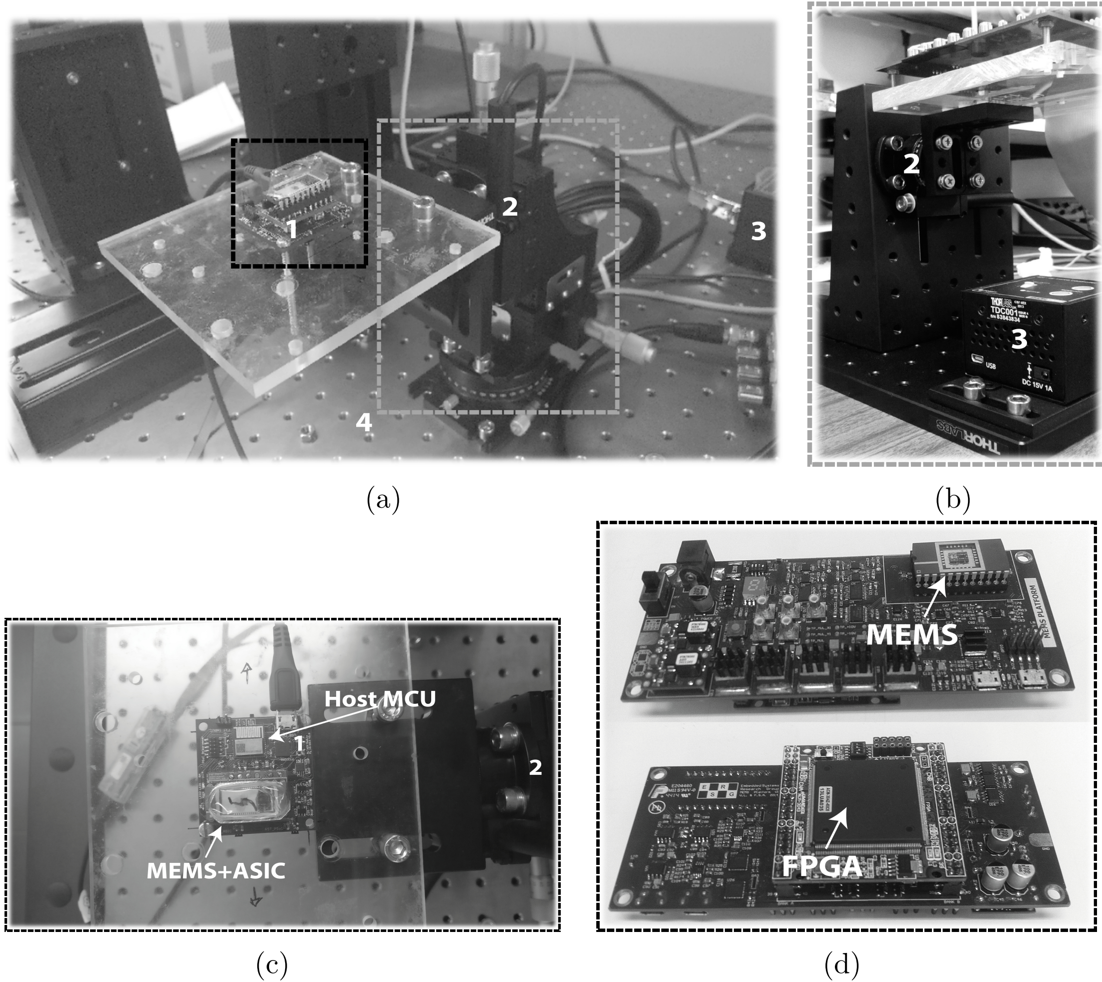
In order to evaluate the performance of the proposed inclinometer, the sensor was mounted on a platform attached to a motor shaft. The complete setup used for the measurements is depicted in figure 5.1a. The platform attached to the motor shaft is placed horizontally as shown in figure 5.1b) with a 90° angle relative to the gravitational force. Rotation of the motor changes the tilt of the sensor.

As shown in figure 5.1a, the sensor prototype, **1**, is placed in the rotation platform. The motor controller (TDC001), **3**, and the motor (CR1-Z7), **2**, both from THORLABS, are responsible for the rotations. The motor enables a 360° angle of continuous rotation with a $608\mu°$ precision. The measurement setup was assembled on a vibration isolating optical table (Nexus B90120A), **4**, also from THORLABS, in order to reduce the environmental noise during the measurements.

Two different sensor prototypes have been used in the experimental testes. An early version, based on a FPGA and COTS readout electronics, figure 5.1d, has been used to perform long term measurements, as well as to investigate the thermal dependence of the sensor. The latest prototype, employing the developed ASIC, figure 5.1c, has been used for the sensor working operation verification, the sensitivity analysis and the performance comparison with the differential capacitance direct transduction.

5.2 ASIC Characterization

Before evaluating the performance of the sensor, it is important to characterize the designed capacitive readout circuit for the different configurations available, namely feedback capacitors and input signal. Considering that the four different feedback capacitor available can be combined, the feedback capacitor can assume fifteen different values. Furthermore, eight voltage levels can be chosen as the excitation signal, resulting in one hundred and twenty different gain configurations.



(a) (b) (c) (d)

Figure 5.1: Experimental setup for the measurement system: a) Complete setup. b) Detail of the rotation motor. c) Detail of the prototype using the MEMS+ASIC integrated sensor. d) Detail of the sensor prototype using FPGA.

The circuit characterization has been performed using structure #4 as the reference capacitance. By tilting the device from $-90°$ to $+90°$ ($\pm 1g$), the movable mass has a well known displacement. Through the calculation of the differential sensing capacitance ($C = C_{left} - C_{right}$) at each tilt angle, it is possible to find the readout circuit sensitivity. The sensitivity results are depicted in figure 5.2.

As expected, the readout sensitivity is dominated by the input signal amplitude. On the other hand, even though its influence is surely noticed, the feedback capacitor has lower impact on the achieved sensitivity. This is due to the parasitic capacitances on the circuit, that can easily reach values of the same order of magnitude of the feedback capacitor. The measured sensitivity can be as high as $2.78V/pF$, for a $250fF$ feedback capacitor and an input signal with $800mV$ of amplitude. The non-linearity of the CVC circuit was also investigated, and the

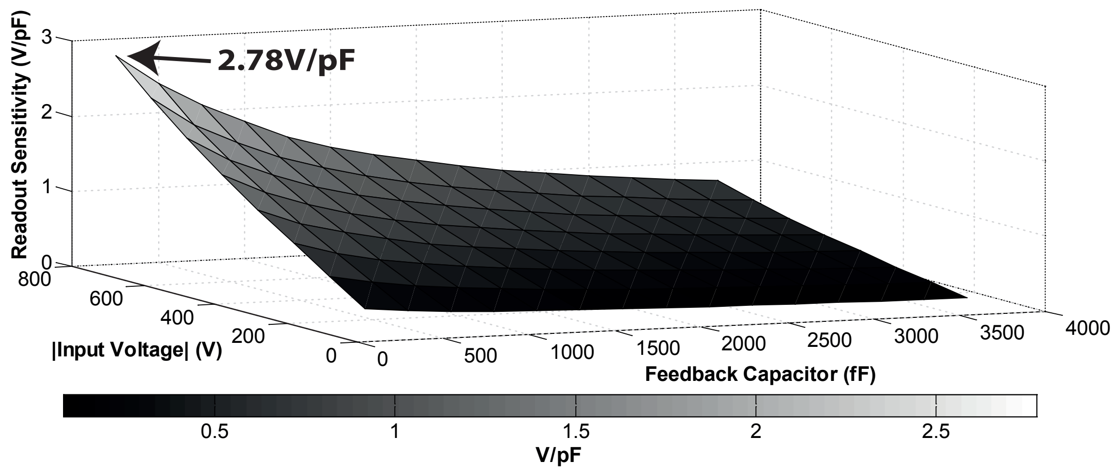


Figure 5.2: Readout circuit sensitivity for the different gain configurations.

results are shown in figure 5.3.

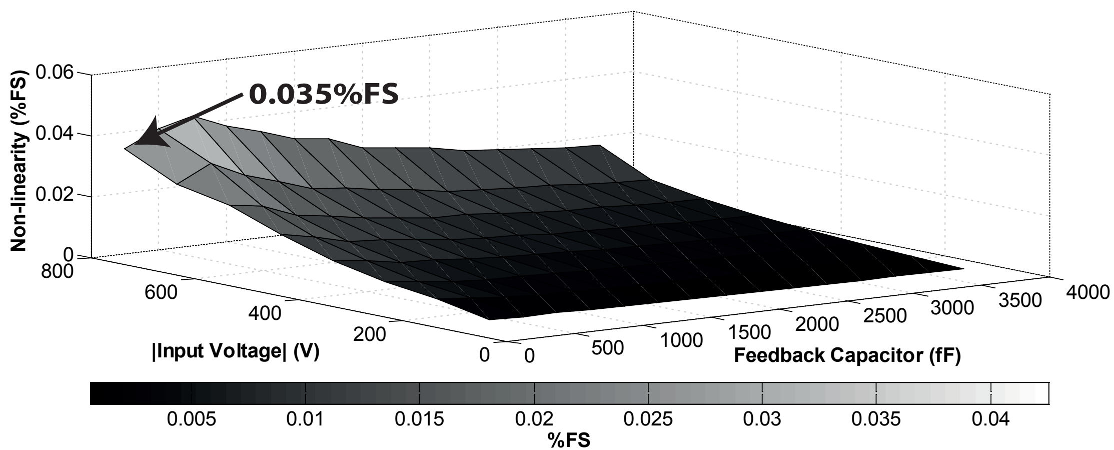


Figure 5.3: Readout circuit non-linearity for the different gain configurations.

In general, good linearity was obtained on the ASIC readout, since a non-linearity better than $0.042\%FS$ has been registered for all the configurations. As predictable, the higher the sensitivity, the higher the non-linearity.

The noise level using each configuration was experimentally measured. Based on those values, and considering the measured sensitivity, the minimum differential capacitance that the circuit is able to detect can be calculated (figure 5.4).

If the typical capacitance change at the pull-in point is taken into consideration ($\approx 40pF$), a signal to noise ratio (SNR) of $110dB$ is accomplished. It is also important to notice that, the high sensitivity achieved, can lead to a circuit saturation before the pull-in point.

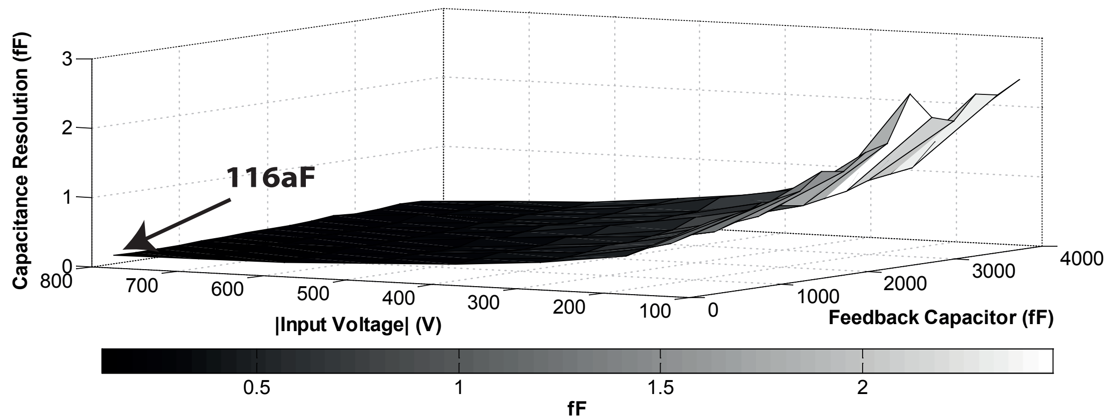


Figure 5.4: Minimum differential capacitance detectable with the readout circuit.

5.3 Performance Analysis

Following the assembly of the experimental setup, and the ASIC performance evaluation, the sensor operation was experimentally verified (figure 5.5). After the switch is turned on, the 20-bit DAC starts to generate the required actuation voltage ramp until the pull-in is detected. Once the pull-in is detected, both switches are connected to the ground allowing the structure to return to its natural position and the procedure is repeated to the other side of the structure. Pull-in voltages are sequentially measured and the inclination is proportional to the difference between the two pull-in voltages. This operation mode enables an inclination measurement each 610 milliseconds, corresponding to a sensor bandwidth of $\frac{1/0.61}{2} = \frac{1.64}{2} = 0.82Hz$.

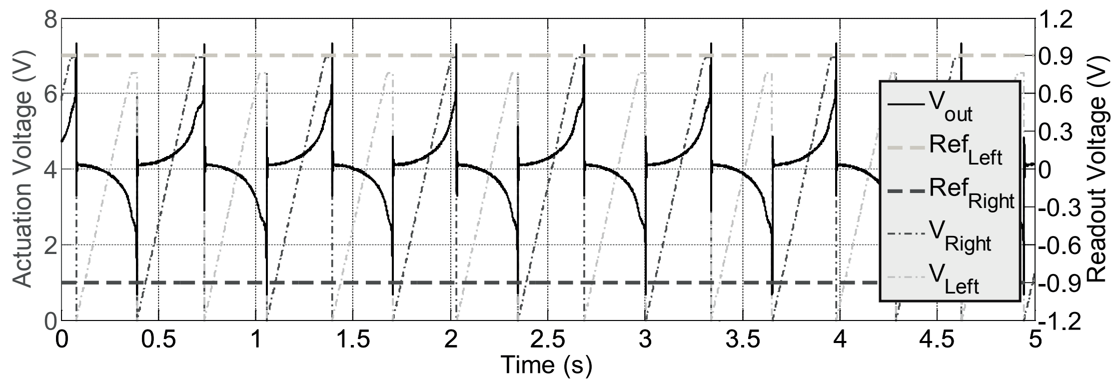


Figure 5.5: Continuous measured differential pull-in voltage.

5.3.1 Sensor Sensitivity

Next, the sensitivity of the pull-in based inclinometers was measured. Devices #1 and #2 results were measured with the COTS setup (using FPGA), while device #3 and #4 measurements used the fabricated ASIC. The results for the four different fabricated microstructures are shown in figure 5.6. The device with extra proof-mass, #2, shows the highest sensitivity ($290mV/°$), followed by the other extra-mass device, #1 ($269mV/°$). Structure #3 shows the lowest sensitivity ($41.4mV/°$), while device #4 displayed an intermediate sensitivity of ($112mV/°$). These results are consistent with the devices design parameters since #2 has the highest mechanical sensitivity ($\frac{m}{k}$). The non-linearity of the sensors was also calculated and found to be below 0.5%FS (Full Scale of ±23°) for both #1 and #2, below 0.9%FS (Full Scale of ±60°) for #3 and below 0.7%FS (Full Scale of ±18°) for device #4.

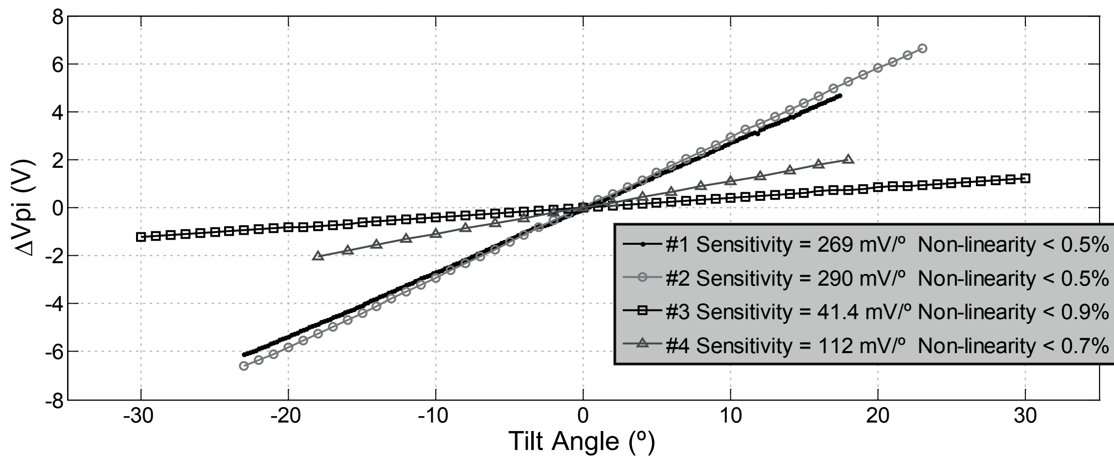


Figure 5.6: Sensitivity results with experimental pull-in voltages measurements.

5.3.2 Long Therm Analysis

The two best performance inclinometers (#1 and #2), were used for a long-term analysis. In an attempt to have constant temperature, the sensor prototype was placed in an oven (with very good thermal insulation) and the sensors were continuously operated for several days (after temperature stabilization), as shown in figure 5.7.

The $20\mu V$ resolution of #1, which corresponds to the DAC's resolution, is clearly visible. The performance of #1 is currently limited by the DAC's resolution and

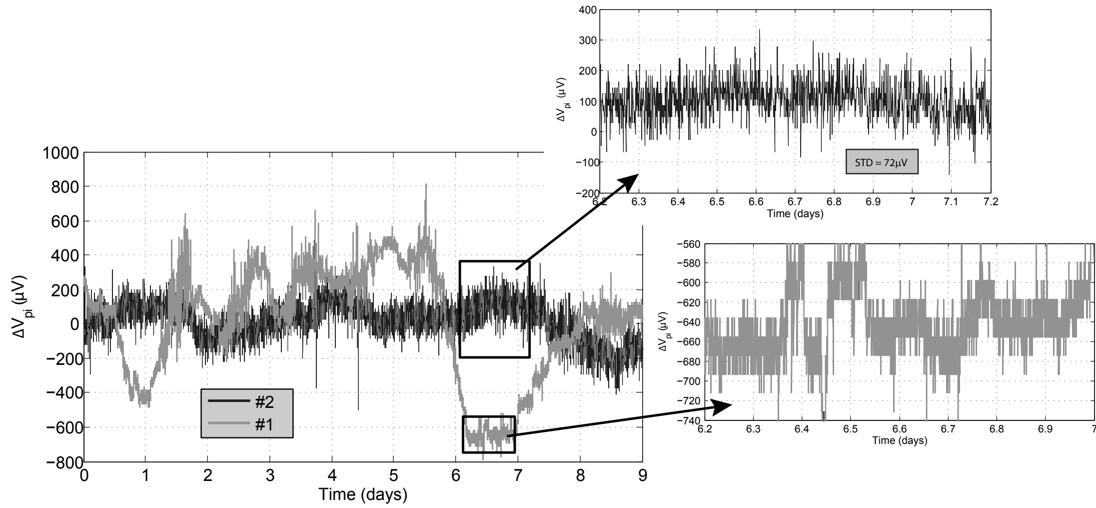


Figure 5.7: Long term noise level measurements using structures #1 and #2 at constant temperature (37°C).

not by other noise sources. Regarding device #2, a noise level higher than the DAC's resolution is observed. This is due to the high quality factor of the device (Q = 7.56) that causes mechanical oscillation of the device during actuation resulting in pull-in noise. Considering the measured noise-level of $72\mu V$, the resolution of #2 is $248\mu°$. The resolution of #1 is $75\mu°$ $(\frac{20\mu V}{269mV})$. This high-resolution sets the system dynamic range at $[20log(2 \times \frac{23°}{75\mu°})] = 116dB$.

Although no measures were taken to minimize external vibrations/oscillations in the oven, the long-term stability of the sensors is very good. Structure #2 presents stability better than $400\mu V(< 0.003\%$FS) while #1 presents a stability better than $1100\mu V(< 0.009\%$FS). The results obtained with #1 are consistent with weekdays day/night activity (between day 1 and 5) and weekend (days 6 and 7).

Since device #1 registered the highest performance, in terms of stability and resolution, it has been used to perform an extended long term measurement (80 days) in a low noise environment. The temperature was also monitored during these measurements, since a small temperature dependence has been observed in other experiments. The sensor output and the measured temperature over the 80 days are depicted in figure 5.8.

Even though large temperature variations were registered ($2.5°C$), the sensor prototype shows a stability better than $4m°$ (<0.009%FS) during almost 3 months. The larger deviations on the sensor output are clearly due to temperature changes, which can be compensated at different levels.

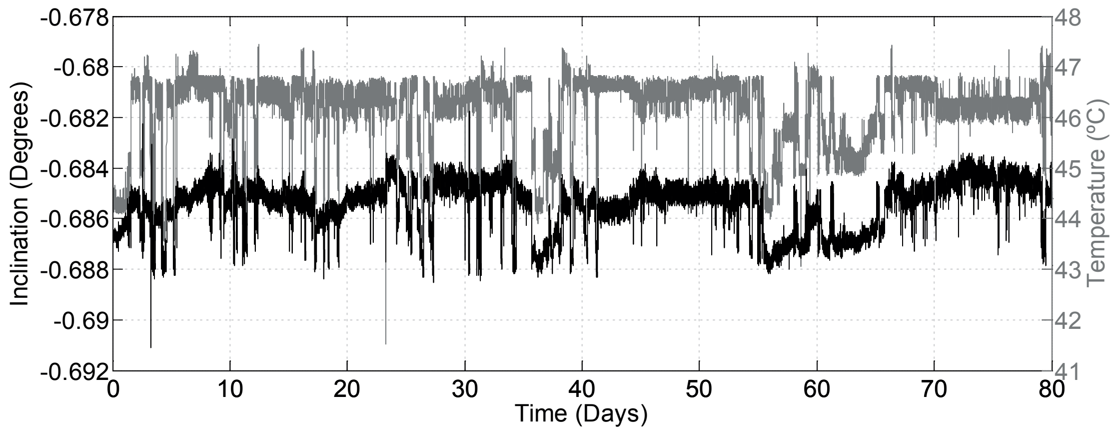


Figure 5.8: Long term noise level measurements using structure #1 with temperature monitoring.

The measured differential pull-in voltage variations are smaller than the left and right pull-in voltage variations. It means that the differential measurement, is already compensating part of the changes due to temperature. Additionally, the measured temperature can be used to compensate the sensor output, as:

$$Out_{compensated} = Out - \alpha \times \left(T - T_{initial}\right), \tag{5.1}$$

where Out is the sensor output without compensation, T and $T_{initial}$ are respectively the measured temperature and the initial temperature, α is the sensor thermal coefficient and $Out_{compensated}$ is the resultant sensor output.

A thermal coefficient, α, of $800\mu°/°C$ was experimentally obtained and used to compensate the long-term results. A detailed (2 days) outcome of the compensation mechanism is shown in figure 5.9.

The sensor thermal stability was increased to values better than $0.002\%FS$, using the compensation mechanism based on the measured temperature.

5.3.3 Thermal Stability

The thermal dependency registered during the long term analysis, even though reduced, demanded for a deeper analysis on the thermal behavior of the pull-in based inclinometer. Compensating any temperature variation by using the measured temperature, equation (5.1), proved to be efficient. Anyhow, it does not fulfill the auto-calibration characteristic intended for the sensor. Therefore, a

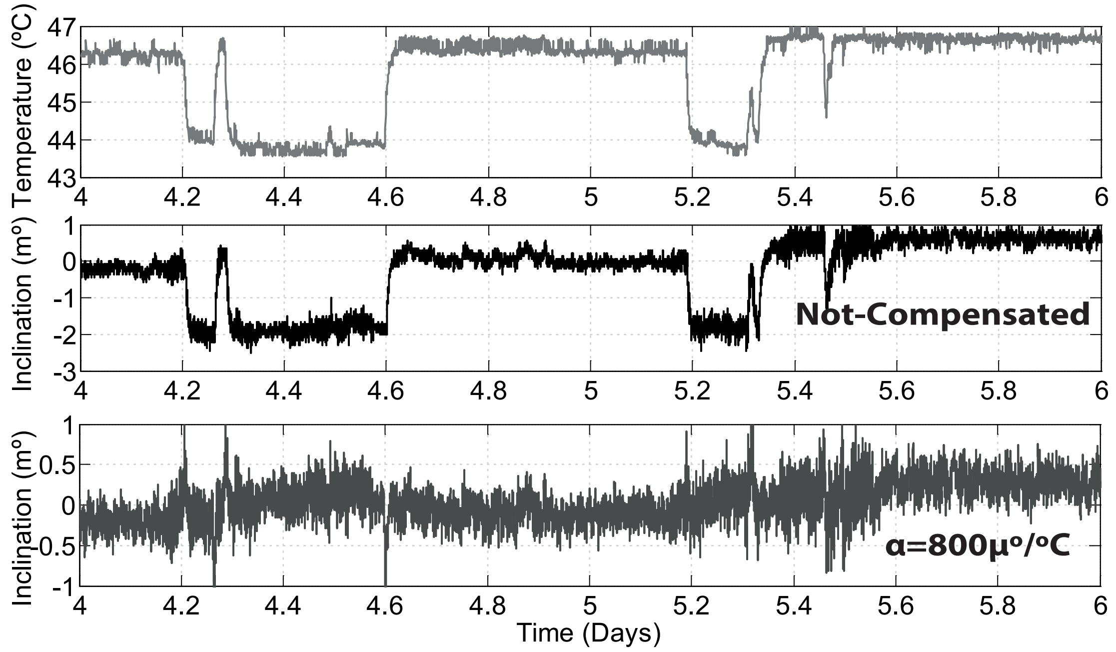


Figure 5.9: Compensated sensor output, using the measured temperature.

compensation mechanism that does not require the temperature measurement has been studied.

Differential measurements of left and right pull-in voltages should guarantee (in theory) that the sensor output is not affected by temperature variations since the two pull-in voltages depend on the same mechanical structure. In reality, accordingly to the theory presented in section 2.3.1, thermal cycles performed at different inclinations (figure 5.10) revealed that the two pull-in voltages have different temperature coefficients, CTE ($CTE_{Vpi_{left}} \neq CTE_{Vpi_{right}}$). Moreover, the CTE of the differential pull-in measurement (ΔV_{pi}) changes with inclination (between 240 and $330\mu V/°C$).

While the changes with inclination on differential pull-in thermal CTE are due to different left and right actuators gaps varying with temperature (due to thermal expansion), the different pull-in voltages CTE are attributed to process tolerances, mainly charge effects.

As presented in section 2.3.1, it is believed that the nominal pull-in voltage, $V_{pi_n} = \frac{V_{pleft}+V_{pright}}{2}$, of the microstructure can be used in a compensation mechanism. The CTE of the nominal pull-in voltage was then experimentally measured for different inclinations (figure 5.11a) with a mean value of $-330\mu V/°C$, which is in good agreement with simulations (figure 5.11b) [5.5].

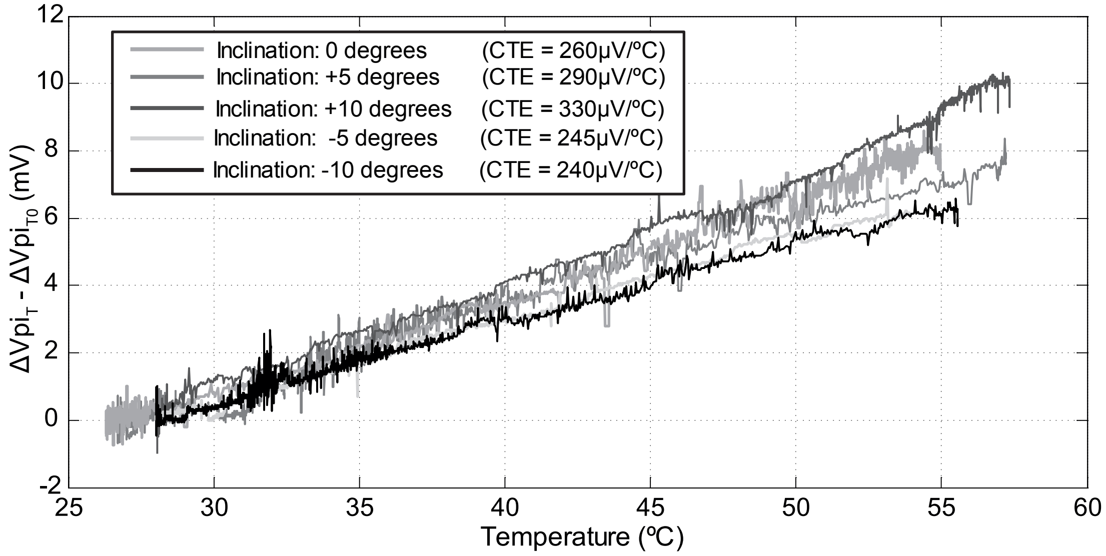


Figure 5.10: Experimental results of (ΔV_{pi} for different temperatures at different tilt angles. (The noise in the measurements is due to external perturbations during the test, and not related with the sensor noise level).

The similarity of the experimentally measured temperature CTE for V_{pi_n} and ΔV_{pi} suggest that the compensation mechanism proposed in equation (2.21) can be used. For the sake of convenience, it is rewritten below:

$$Compensated\ \Delta V_{pi} = \Delta V_{pi_T} + \delta(V_{pi_nT} - V_{pi_nT_0}), \tag{5.2}$$

where ΔV_{pi_T} is the measured differential pull-in voltage at a given temperature T, V_{pi_nT} is the nominal pull-in voltage at that temperature and $V_{pi_nT_0}$ is the same voltage at the calibration temperature T_0. The compensation factor is defined by $\delta = \frac{CTE_{\Delta V_{pi}}}{CTE_{V_{pi_n}}}$.

Experimental testes using the proposed compensation mechanism where performed with $\delta = 0.8$, resulting in a thermal compensated high resolution inclinometer, with a thermal stability better than $0.004\%FS$ as shown in figure 5.12.

The experimentally obtained thermal stability, proved the efficiency of using the nominal pull-in voltage in a compensation mechanism for temperature changes.

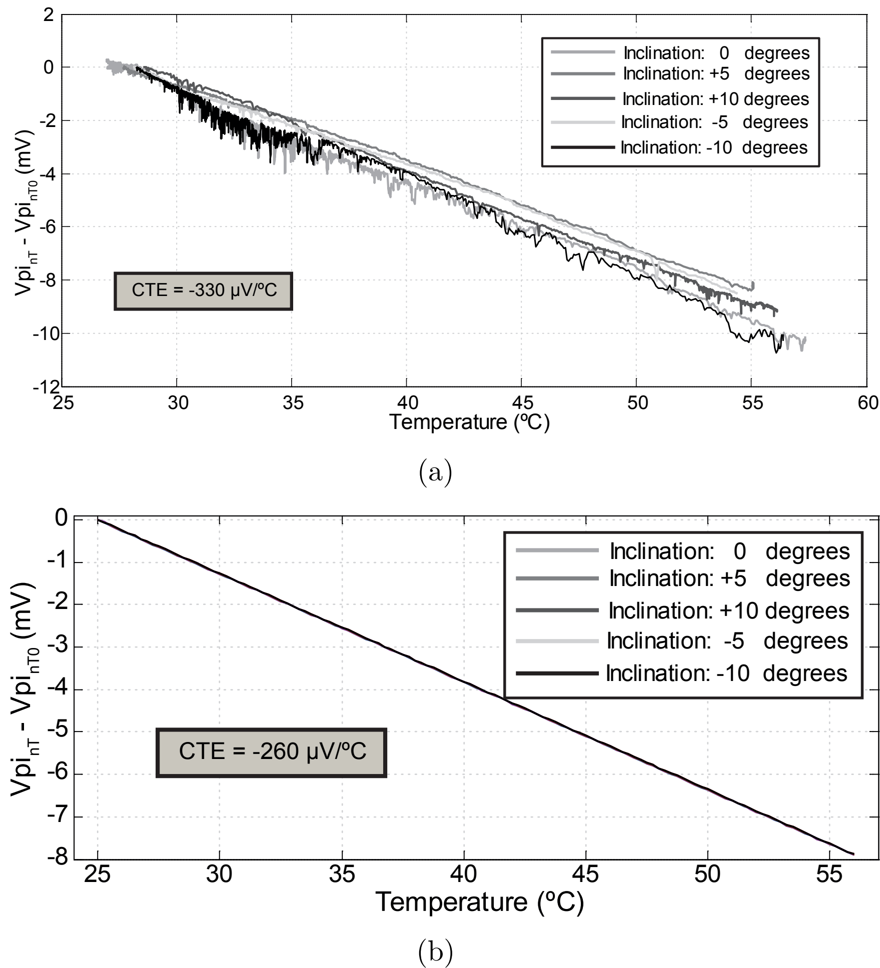


Figure 5.11: a) Experimental results of the measured nominal pull-in voltage at different temperatures and different inclinations. b) Simulated results of the nominal pull-in voltage at different temperatures.

5.3.4 Charge Effects

As discussed in the previous section, charge accumulation (section 2.3.2) on the parallel-plate actuator dielectric might originate a pull-in voltage deviation, and can also influence the sensor thermal behavior thermal behavior. Even if the differential measurements already cancels most of the effects, charge accumulation can be further minimized.

Using device #3, the pull-in variation, due to charge accumulation (equation (2.28)), was experimentally tested using consecutive measurements (consecutive ramps, up to the pull-in point). The results are presented in figure 5.13, showing a pull-in voltage drift of $5.2mV$ between the initial pull-in voltage (dielectric discharged) and the final voltage (dielectric completely charged).

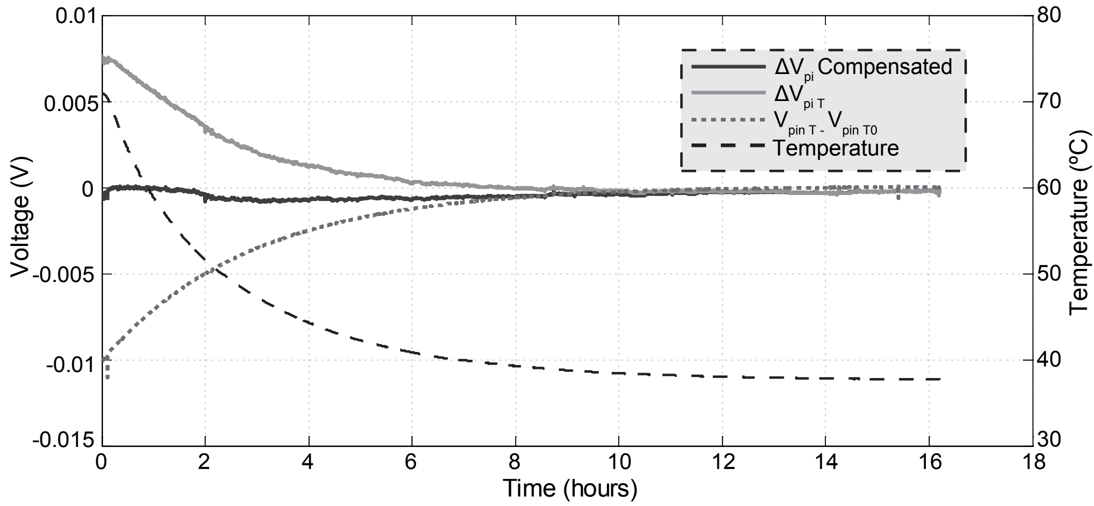


Figure 5.12: Measured results using the thermal compensation mechanism.

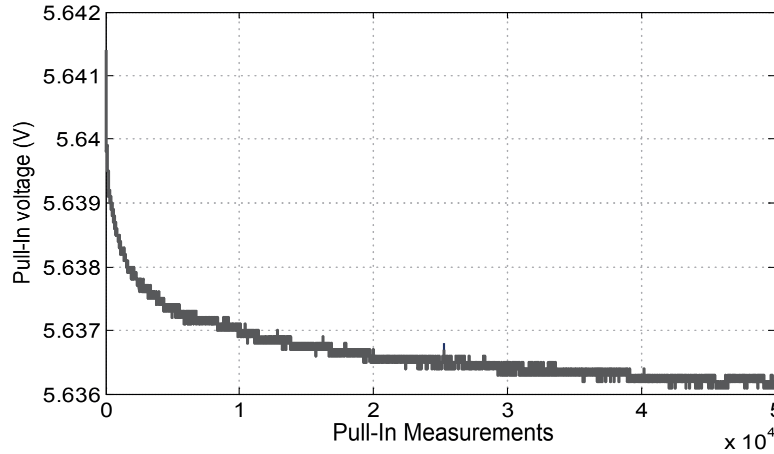


Figure 5.13: Pull-in voltage variation during consecutive measurements, due to charge effects.

From the theory presented in section 2.3.2, the amount of charge trapped in the dielectric can be reduced, and consequently minimize the pull-in voltage variation, by introducing an OFF time between each measurement (period without actuation), according to:

$$\Delta V_{pi} = \frac{V_0}{\tau} exp\left(\frac{-t_{off}}{\tau}\right), \tag{5.3}$$

where t_{off} is the time between measurements, and V_0 and τ are experimentally obtained parameters. The experimental results presented in figure 5.14, showed a relation between the OFF time and the pull-in variation in accordance with

equation (5.3).

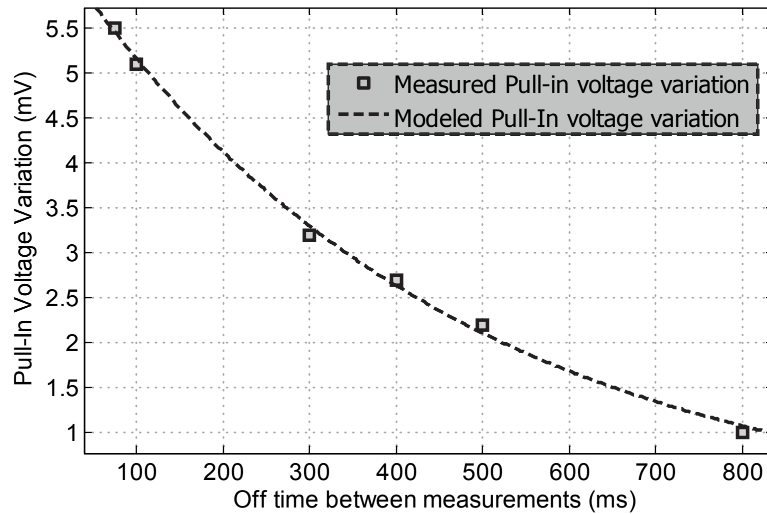


Figure 5.14: Pull-in voltage variation vs OFF time.

Another approach to get around the charge effects on capacitive actuators is the use of bipolar actuations, positive and negative voltages, instead of just positive actuation voltages [5.6].

This principle is based on the fact that, when a positive voltage is applied to the electrostatic actuator, positive charges will be injected in the dielectric, while negative charges are injected during a negative actuation. Assuming a symmetric actuation (same actuation time and amplitude for both voltages), the negative charges will counteract the positive ones, resulting in a charge density equal to zero. However, the charge injection is not exactly symmetric for positive and negative voltages, resulting in a residual charge density in the dielectric. This suggests that by using non-symmetric actuations, an equilibrium point might be found where the charge density is minimized.

Some experiments on the bipolar actuation technique have been performed using the FPGA based prototype. The sensor operating principle was changed to the one depicted in figure 5.15.

The preliminary results, using device #1, are presented in figure 5.16 where the single ramp and the bipolar ramp operations can be compared.

The $3mV$ drift registered using the single ramp operation, can be compensated to a less than $500\mu V$ variation, when using the positive and negative ramp working mode. The first results are very promising, but further investigation is required.

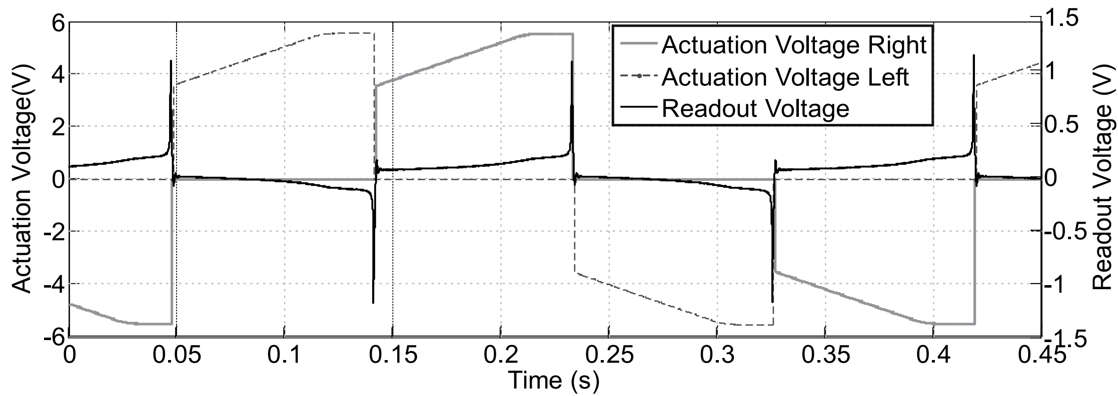


Figure 5.15: Sensor operating principle using positive and negative ramp voltages.

The developed ASIC can be used to investigate this approach, as it is configurable in terms of the sensor actuation mode (single or dual ramp operation can be used).

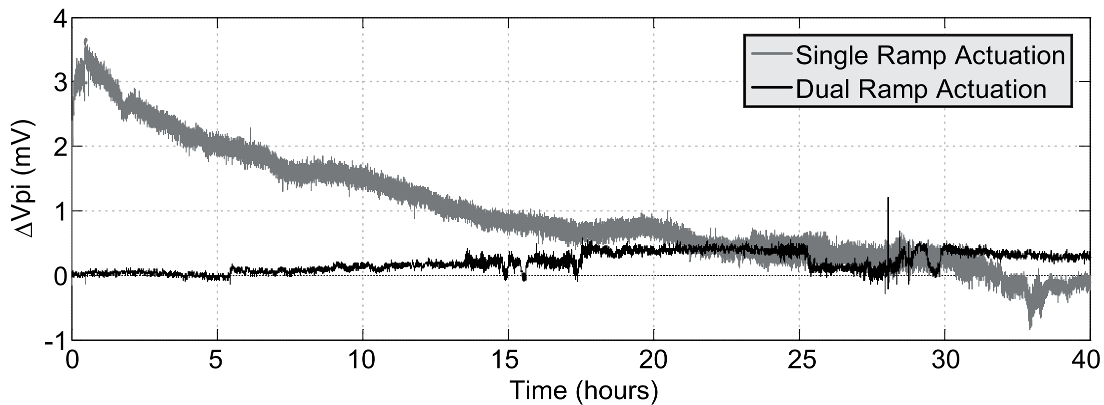


Figure 5.16: Differential pull-in voltage variation due to charge effects, using single and dual ramp actuations.

5.3.5 Differential Capacitive vs. Pull-In Based Detection

In order to experimentally verify the sensitivity difference between the pull-in based sensor and the more common direct capacitive transduction, stated in section 2.1.3, differential capacitance measurements were performed with device #4 using the voltage output from the ASIC readout circuit. Even though the highest gain configuration was used, the sensitivity results shown in figure 5.17, clearly show a huge sensitivity reduction.

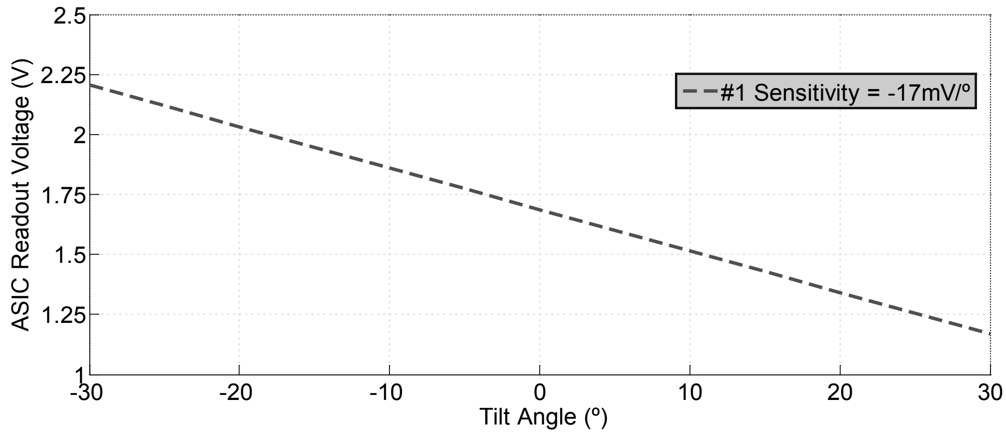


Figure 5.17: Sensitivity results with experimental differential capacitive measurements.

5.4 Conclusions

The sensitivity and noise level results from the integrated circuit capacitive readout clearely fulfill the application requirements, with a measured SNR of $110dB$.

In terms of the performance of the sensor itself, the different MEMS devices used in this experiment, as expected, showed different performances. Devices with extra-mass, #1 and #2, strongly increase sensitivity ($> 269mV/°$), when compared to the other devices ($< 112mV/°$) [5.7]. Even though, given the simplicity of the fabrication process of structure #4, the sensitivity results are very promising as different designs with good sensitivity can easily be fabricated and tested.

Long term results showed that he sensor resolution is currently limited by the actuation system (1 LSB - $20\mu V$), namely the DAC used. The pull-in based transduction mechanism proved to be more effective than traditional differential capacitive methods, with increased sensitivity and more relaxed requirements for the capacitive readout electronics.

Compensation mechanisms, implemented directly in the mechanical domain (differential pull-in measurement), can be complemented by more complex methodologies. It has been proven that the nominal pull-in voltage can be used as a way to compensate thermal drifts, without requiring temperature measurements.

A deeper analysis on the charge effects minimization needs to be performed, but the presented preliminary results are very promising. The results suggest that the already good stability of the sensor, can still be further improved.

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6

Conclusions and Future Work

The theoretical an experimental verification of pull-in based high resolution MEMS inclinometers has been presented in this thesis. The pull-in nonlinear behavior of microelectromechanical structures, when electrostatically actuated, has been analyzed from a static perspective, explaining how it can be used so sense tilt angles with high sensitivity and resolution. Significant characterisation and analysis on the ASIC readout circuit and sensor behavior have been made.

This chapter summarizes the goals, contributions and conclusions of this thesis. It also proposes possible directions for future research.

6.1 Conclusions

The main conclusions to be drawn from the developed work can be divided as follows:

1. **Nonlinear electromechanical coupling:** Exploiting the unique characteristics of nonlinear parallel-plate electrostatic MEMS devices, creates the

possibility of designing a whole range of new high-resolution sensors. The proper integration of optimised MEMS devices with the required microelectronics allows the minimization of the noise sources, which can lead to higher resolutions.

2. **Capacitive readout circuit:** The pull-in phenomenon, used here as transduction mechanism, is detected through a sudden change in the MEMS sensing capacitance. This capacitance change is sensed by a switched capacitor based readout circuit that showed a SNR of $110dB$. Although there are no tight requirements in therms of noise, a minimum differential capacitance change of $116aF$ can be detected with the fabricated circuit.

   The mixed signal ASIC has been designed with a high configuration level. Different gain configurations and comparison values (used to detect the pull-in point) can be selected, enabling the test of MEMS devices with different characteristics. The standard serial communication available on the ASIC, I^2C, enables an easy integration of the sensor in any electronic system.

3. **High resolution inclinometer performance:** The fabricated sensor prototypes have been experimentally verified, showing performances above current state-of-the-art MEMS devices.

   (a) **High sensitivity:** The different MEMS devices tested showed that sensitivities as high as $290mV/°$ can be achieved (structure #2). This is the result of combining the non-linear pull-in phenomenon with an extra proof-mass, attached to the MEMS movable part (portion of the handle wafer from the SOI-process). Lower sensitivities were achieved for devices with simpler fabrication processes (#4 - $112mV/°$), which can reduce the development time of new sensor designs and are much easier to integrate.

   (b) **Long term stability:** Extensive experiments have been performed to examine the long term stability of the proposed approach. In an eighty days experiment, a stability better than 0.009%FS was registered, on a not thermally isolated environment (thermal variation of $2.5°C$).

   (c) **High resolution:** It is expected that the resolution limitation of the sensor would be either the mechanical-thermal noise of the MEMS device, or the noise/resolution of the actuation system. The results of the fabricated prototypes showed that, the registered $20\mu V$ noise level, for

the best performing device, is limited by the resolution of the external DAC used. It corresponds to an $75\mu°$ resolution.

The differential capacitance direct transduction comparison showed that, to achieve similar resolutions, a readout circuit capable of measuring $6aF$ would be required. It means that, the current ASIC would need to be improved around 20 times.

(d) **Thermal compensation:** Even though the sensor showed a low thermal drift, two different compensation mechanisms have been proposed. If the operating temperature is measured, a sensor stability better than 0.002%FS can be achieved.

Without measuring the temperature, the nominal pull-in voltage can be used as a compensation method. This method improves the sensor stability to values better than 0.004%FS.

4. **State-of-the-art comparison:** The sensor's performance (considering device #1) is summarized and presented in table 6.1. It shows to be better than existing MEMS state-of-the-art devices and at par with other non-MEMS technologies.

Table 6.1: Comparison with state-of-art devices specifications

	MEMS Inclinometers				Not MEMS technology/Conventional inclinometers	
Specification	Pull-In Inclinometer	MEMSIC AXTLA01/02 [6.1]	RST Digital Tilt Logger [6.2]	Murata SCA103T D05 [6.3]	Jewell LSOC/LSOP [6.4]	Sherbone Sensors LSOC/LSOP [6.5]
Resolution ($\mu°$)	75	30000	600	1300	280	28
Sensitivity (mV/°)	269	100±10	NA	140	3183	5000
Operation Range (°)	±23	±20	±15	±30	±1	±1
Bandwidth (Hz)	0.82	6	0.1	28	0.5	10
Non-Linearity (%FS)	<0.5	<0.4	0.0125	0.11	0.03	0.05
Thermal Drift (%/°C)	0.002	0.01	NA	0.013	0.04	0.05
Stability/Repeatability (%FS)	<0.009	NA	±0.0125	0.028	NA	0.04
Output Signal	Digital	Analog Voltage	Digital	Digital	Analog Voltage	Analog Voltage
Technology	MEMS	MEMS	MEMS	MEMS	Closed-Loop (Servo)	Closed-Loop (Servo)

NA - Not Available

5. **Limitations:** The main limitations in the described work must be pointed out. These help to narrow the focus on the next development steps. How these limitations can be overcome in future work is described in the following section.

(a) **External Actuation system:** The need of an external actuation sys-

tem, namely DAC and digital switch can be indicated as the main limitation of the current prototype. This is the only impediment on having a fully-integrated sensor.

(b) **Bandwidth:** Although having a large bandwidth is not a requirement of inclinometers, the time per measurement of the current sensor can be further decreased by improving the ramp generation algorithm.

6.2 Future Work

Several research directions have been found, in order to tackle the limitations identified in the presented work.

6.2.1 System Full Integration

The main challenge on the complete integration of the sensor is the pull-in voltage of the currently used MEMS devices. The need for above-the-rail actuation voltages ($V_{pi} > 3.3V$), has been limiting the current approach and requires the use of an external actuation system.

Designing the MEMS sensing element to have lower pull-in voltages would decrease the sensor sensitivity, compromising the overall performance. It is then visible the need for the investigation of analog CMOS design techniques, that allow the generation of the required voltages.

The use of a high voltage CMOS fabrication processes [6.6], allied with voltage boosting circuits (charge pumps) [6.7], seems like the next step on the sensor improvement towards full-integration and is currently under investigation.

6.2.2 Time-Based Pull-In Inclinometer

A slightly modified operation mode is believed to be capable of simplifying the sensor system, without compromising the performance.

Considering that the full-integration is one of the goals for the next generations of the sensor, the current operation mode requires the design of a low-noise high

resolution DAC to generate the actuation voltage. This can be a very challenging task, considering the $20\mu V$ resolution of the current prototype.

As an alternative, it is believed that, if a well defined analog circuit is used to generate a sawtooth like voltage signal, the tilt angle of the sensor can be measured by digitally counting the elapsed time until the pull-in detection. A block diagram of the proposed approach is depicted in figure 6.1.

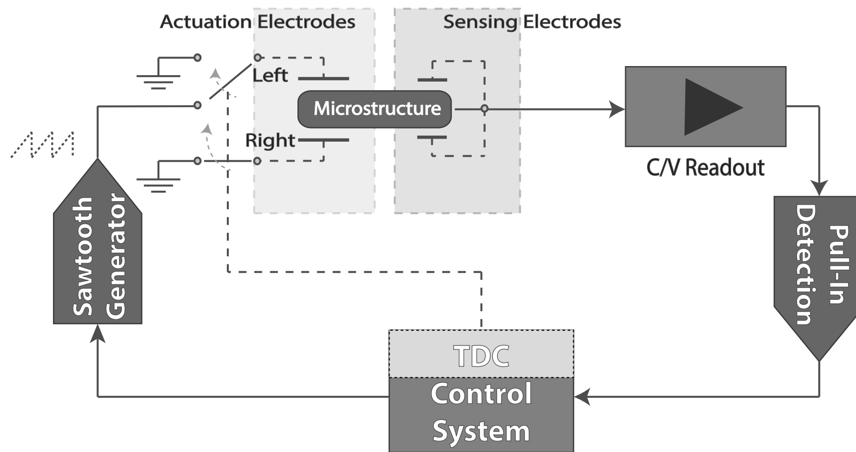

Figure 6.1: Block diagram of the proposed time-based pull-in inclinometer.

If the slope of the generated voltage signal is stable enough, the pull-in time variation will be due to the tilt of the sensor (figure 6.2). It basically consists of measuring the pull-in voltage using a time counter. As several high frequency time-counting mechanisms can be easily implemented, such as CMOS TDCs [6.8], high resolutions can be achieved using this approach.

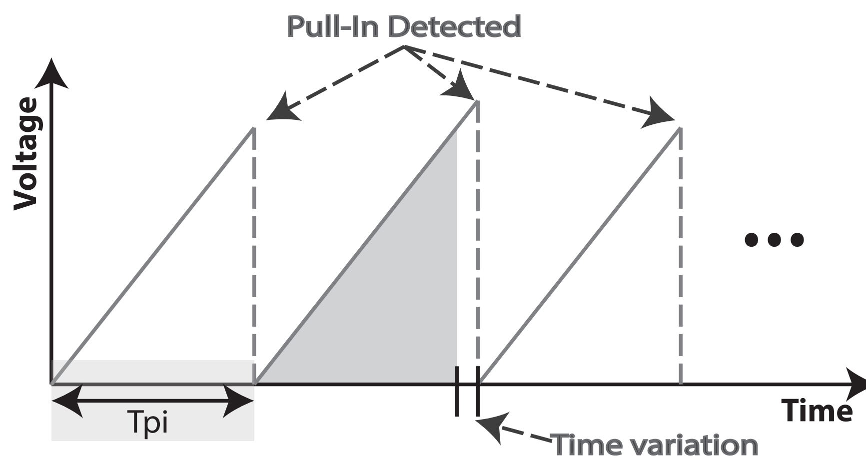

Figure 6.2: Representation of the new approach working principle.

6.2.3 Tuning Resolution vs Operating Range

The performance of the sensor is mainly defined by the mechanical properties of the MEMS sensing element. Depending on the application, a completely new design might be needed, in order to meet the specifications.

Pull-in based sensors, besides the advantages highlighted in the course of this thesis, have the possibility of employing techniques to enhance the device sensitivity. Considering the differential set of actuators available in the MEMS structures proposed in this work, a compensation voltage can be applied on the counter electrode at the same time that the pull-in voltage is being measured (figure 6.3).

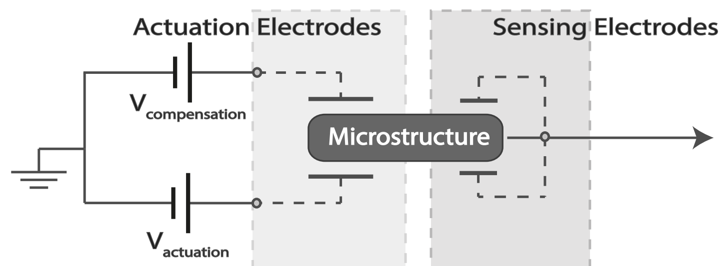

Figure 6.3: Representation of the sensitivity increase technique.

The applied voltage, generates an electrostatic force in the direction opposite to pull-in. It means that, higher voltages will be required to reach the pull-in point. As a matter of fact, the pull-in voltage increase is directly translated to a sensitivity increase on the sensor. Some preliminary simulations have been made, considering the details of device #3, and the results are shown in figure 6.4.

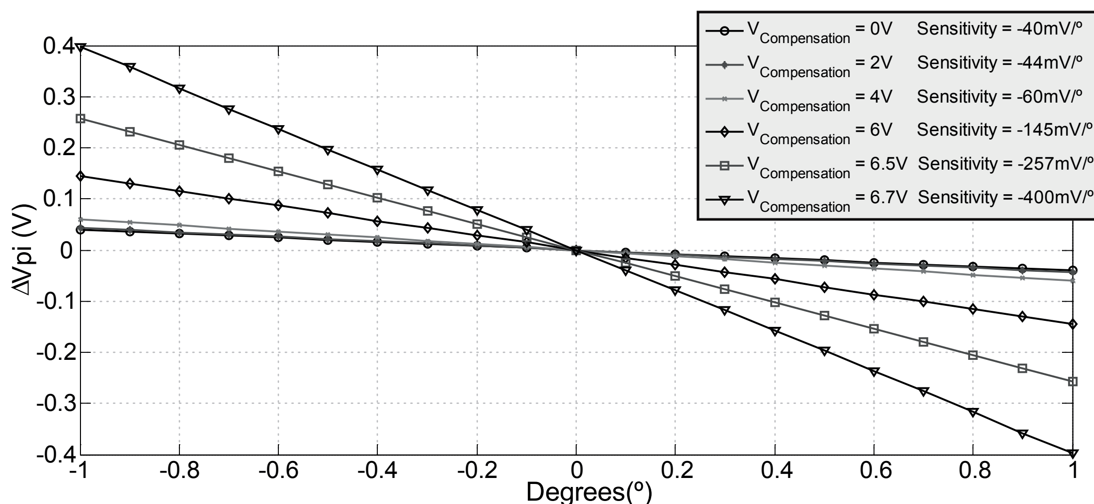

Figure 6.4: Simulation results of the proposed sensitivity increase technique.

In the simulation results, a sensitivity improvement of 10 times ($40mV/°$ to $400mV/°$) was obtained by applying a compensation voltage of $6.7V$. Since the mechanical properties of the sensing element were not modified during simulations, no changes are expected, regarding the sensor noise level, usually limited by the structure mechanical-thermal noise. Therefore, the sensitivity gain will lead to a resolution improvement in the same order, at the expense of lower dynamic range (full-scale).

The limitation of this approach would be the high pull-in voltages, that might limit the operating range of the sensor (high tilt angles would require voltages not supported by the actuation system). The most interesting point of this method is the trade-off between resolution and operating range, easily controlled by the compensation voltage.

A highly versatile sensor can then be achieved and easily tuned for different target applications.

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List of Publications

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Filipe Alves was born in Valença, Portugal in 1989. He received the M.Sc. degree in Electronic Engineering at the University of Minho, Portugal, in 2012. In 2013 he started pursuing the Ph.D degree at the Industrial Electronics Department of the same university. In the past few years he has been a Ph.D visitor at different institutions, Electronic and Instrumentation Laboratory at the Delft University of Technology, The Netherlands, and International Iberian Nanotechnology Laboratory, Braga, Portugal. His research focused on the study and design of pull-in based MEMS sensors and mixed-signal CMOS IC design.

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