Universidade do Minho
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Rui Miguel Tinoco da Luz

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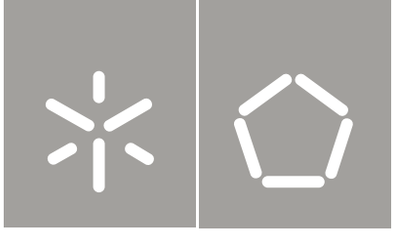

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Organic Electronics – Implementation of Some Components and Organic Logic Simulation

Tese de Mestrado
Ciclo de Estudos Integrados Conducentes ao Grau de
Mestre em Engenharia Eletrónica Industrial e Computadores

Trabalho efetuado sob a orientação do
Professor Doutor José Gerardo Rocha

e co-orientação do
Professor Doutor Senentxu Lanceros-Mendez

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DECLARAÇÃO

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Rui Luz

Abstract

Organic and printed electronics are promising technologies due to their versatility and expected future applications. Using commonly available laboratory tools and organic materials, three electronic components have been implemented and analyzed – a schottky, an OFET and a capacitor. Simulations of digital logic have been carried out based on the OFET characteristics. It was observed that PEDOT:PSS did not display a schottky barrier, contrary to Tips-Pentacene, with the used materials. The fact that no barrier formed in any of the three schottky devices using PEDOT:PSS, seems to indicate that both gold and aluminum are possible candidates for hole injection into the polymer. The gate to the channel current proportion, in the created OFET device, generated difficulties in the analysis, which were overcome with a physical simulation. Considering the behavior of the OFET, some production steps should be revised, such as the curing time for both dielectric and semiconductor. Additionally, the adequacy of the deposition masks to the deposition process should be previously evaluated, using masks with sample apertures with the intended substrate. Using PMMA as the dielectric, the capacitors presented a stable capacity for the range of tested frequencies, although their parasitic did not. The parasitic behavior in capacitors formed with Au/PMMA/Au and Al/PMMA/Au show some disparities that might require further research to be clarified. The fact that these devices have been made without any special atmospheric condition, with common tools – even using hand-made masks – reinforce the market potential of printed and organic electronics.

Key-words: OFET; Schottky; PMMA capacitor; Organic electronics; Printed electronics; Organic logic

Resumo

Tanto a eletrónica orgânica como a impressa têm-se revelado tecnologias promissoras devido à sua versatilidade e aplicações futuramente esperadas. Com recurso a instrumentos de laboratório comuns e materiais orgânicos, foram implementados e analisados três componentes eletrónicos – um schottky, um OFET e um condensador. Foram também realizadas simulações de lógica digital, com base nas características do OFET. Verificou-se com a caracterização dos díodos que o PEDOT:PSS não apresentou uma barreira schottky, contrariamente ao Tips-Pentacene. O facto de não ter sido formada uma barreira em qualquer dos três dispositivose shottky desenvolvidos com PEDOT:PSS, parece indiciar que quer o ouro quer o alumínio são candidatos possíveis para injeção de lacunas no polímero. A proporção entre a corrente parasita da gate e a corrente que atravessa o canal, no OFET construído, criou dificuldades de análise que foram ultrapassadas com a sua simulação física. Tendo em consideração o comportamento do OFET, conclui-se ser necessária a revisão de algumas das fases de fabrico, tal como o tempo de cura para o dielétrico e semicondutor. Adicionalmente, deve existir uma avaliação prévia quanto à adequação das máscaras de deposição aos processos de deposição, usando para tal máscaras com diferentes aberturas amostrais juntamente com o substrato desejado. Utilizando o PMMA como dielétrico, os condensadores apresentaram uma capacidade estável para o leque de frequências testadas, embora o mesmo não tenha sucedido com as suas componentes parasíticas. O comportamento parasítico nos condensadores formado com as combinações Au/PMMA/Au e Al/PMMA/Au demonstra algumas disparidades, cuja clarificação exige investigação adicional. O facto destes dispositivos terem sido construídos em condições ambientais sem exigências especiais, recorrendo a materiais comuns – incluindo máscaras construídas manualmente – sustentam o potencial de mercado da eletrónica orgânica e impressa.

Palavras-chave: OFET; Schottky; Condensador com PMMA; Eletrónica orgânica; Eletrónica impressa; Lógica orgânica;

“A parte que ignoramos é muito maior que tudo quanto sabemos”

Platão

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Nomenclature

a-Si	amorphous silicon
CAD	Computer Aided Desing
CNTs	carbon nanotubes
DOS	Density of States
DW	Direct Writing
FET	Field Effect Transistor
FP7	Seventh Framework Programme
HOMO	Highest Occupied Molecular Orbital
IPS	Instructions per Second
K	Kelvin
LUMO	Lowest Unoccupied Molecular Orbital
MWCNTs	Multi walled carbon nanotubes
OE-A	Organic and Printed Electronics Association
OFET	Organic Field Effect Transistor
OLAE	Organic and large area electronics
OLED	Organic Light Emiting Diode
OPERA	Organic/Plastic Electronics Research Alliance
OSC	Organic semiconductor
PANi	polyaniline

PE	Printed electronics
PEDOT	poly(3,4-ethylenedioxythiophene)
PEDOT:PSS	poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)
PET	polyethylene therephthalate
PolyMap	Technology Roadmap of Processes and Mmaterials for Organic Electronics
PolyNet	Network of Excellence for the Exploitation of Organic and Large Area Electronics
PPy	polypyrroles
PRODI	Manufacturing and Production Equipment and Systems for Polymer and Printed Electronics
RF	Radio frequency
SPICE	Simulation Program with Integrated Circuit Emphasis
TIPS-pentacene	6,13-Bis(triisopropylsilylethynyl)pentacene

1 Introduction

It was not before 1947 when John Bardeen, William Shockley and Walter Brattain invented and demonstrated the first point contact transistor [7], that the era of electronics started to profoundly affect our lives. Acknowledging the relevance of the invention, they were awarded in 1956 with the Nobel prize in Physics [8]. Two years before they have been nominated, the "first commercial transistor pocket radio" from Texas Instruments was on the market. It was among the first applications that pronouncedly begun to spread and trivialize the inorganic electronic technology [9].

Years later, in 1977, three men, Alan J. Heeger, Alan G. MacDiarmid and Hideki Shirakawa published the research that they have been doing on acetylene [10], and showed a process that could increase, in few minutes, the conductivity of trans-polyacetilene (a derivative of acetylene) by approximately seven orders of magnitude. This was one of the works that helped to lay the foundations of organic electronics. Although some transistors that could be considered polymeric indeed appeared in the literature before this period, as argued elsewhere by Dimitrakopoulos, et al. (pp. 100) [11], it was only after the research of Alan, et al. that the field grew. In recognition of their work, the Nobel committee awarded them in 2000, with the Nobel prize in chemistry “for the discovery and development of conductive polymers” [12].

The purpose of this work was to validate the adequacy of organic and printed electronics to be processed with non-specialized common laboratory tools. To fulfill this objective, it was proposed to create three devices - a schottky, an organic field effect transistor and a capacitor - and additionally, to show that simple logic gates based on the profile of this transistor could be simulated.

In the second chapter, the general aspects on the area of printed and organic electronics will be covered and it will be attempted to show the potential of the field and its economical significance. In addition, some of the most recent innovations alongside with research tendencies will be highlighted. Finally, a comparison between those which are considered the first microprocessors both in organic and

inorganic electronics will be made.

Printed electronics are a set of methods and materials with the promise to unleash new possibilities and applications. This third chapter will detail what processes, methods and materials are being tested, their strengths and weaknesses and - for some of the detailed materials - relevant properties and characteristics will be presented.

The forth chapter attempts to present and confront, for organic semiconductors, the major drawbacks affecting them. Organic semiconductors are prominent players in the area of printed and organic electronics, but unfortunately they display several short and long term problems (specially when applied in transistors), which derive from several agents, such as charge carrier trapping, deterioration, imperfections, parameter variation, among others. In this chapter, only the first two areas will be covered, as they are the ones presenting major constrains.

The fifth chapter will present the materials, methods and description of procedures used. The textual construction of the chapter is intended to allow the reader to jump over the materials and methods, directly to the description of the procedures. The reader is referenced to subjects which he may or may not chose to read, without disturbing the flow of the description.

Finally, In the sixth chapter, the results from the implementation and characterization of each component will be given. Additionally, for the organic field effect transistor, some simulations will be presented. Alongside, discussions concerning the results will be made and, when possible, shortcomings will be scrutinized.

2 New Opportunities, New Markets

In this chapter, a general definition of organic electronics, underlining what the field is and is not, will be given. Following this definition, an economical perspective of the market of organic and large area electronics (OLAE) will be presented, as well as some achievements of the industry and advances that have been happening in research. The interest that the field has been creating on political and industrial organizations will also be evidenced.

In the second part of the chapter, some achievements and advances in the field, more related to research, are finally synthesized.

2.1 Overview of Organic Electronics

Organic electronics, is a relatively new and multidisciplinary area, dealing with the research, development, optimization and implementation of functional materials - which can have relevant electrical, chemical or optical properties - and also dealing with the topology and geometry of these compounds as well as the interactions among them, generating new fields of application. The main disciplines comprising this area, are materials science, chemistry, physics and electronics. The term organic, refers to the characteristic of the active areas in the created devices. Contrary to inorganic electronics, which use inorganic semiconductors such as silicon and germanium, organic electronics use carbon based functional materials, such as polymers and small molecules. As the philosophies inherited by the field proclaim the creation of products that are flexible, inexpensive, disposable, thin, large-area compatible (displays, solar cells, e-skin, etc.), environmentally friendly and lightweight, the field is also known as plastic electronics, polymer electronics, flexible electronics, printed electronics and disposable electronics, although these expressions have their own proper meaning. These functional materials can be solution processed (dispensing vacuum and high temperature) and deposited in a variety of substrates, from plastics to paper (discarding silicon wafers), using much common

deposition processes such as inkjet printing, "newspaper-like" roll-to-roll/reel-to-reel or web processing (flexography, gravure, offset and rotary screen), spin-coating, drop-casting, among others (avoiding soft lithography). The main disadvantages refer to the relatively high resistance of conductors, low mobility of semiconductors, high voltages needed, difficulties in achieving high repeatability of characteristics in devices and shorter lifetime of the materials than in inorganic electronics. The current and future main applications comprise, large-area organic light emitting diode displays, solar cells, lightning, logic, memory, transistors, battery and smart integrated systems. (pp. 18[13]), (pp. 15 [14]), (pp. 4 [15]), (pp. 1-2 [16]), (pp. 3 [17]), (*preface* [18]), (pp. 1 [19]), (pp. 4 [20]).

Figure 2.1: The first commercial OLED TV from Sony Corporation

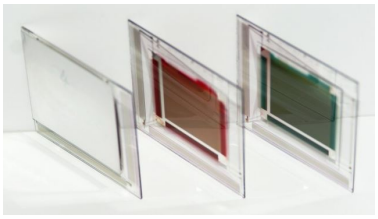


Figure 2.2: NikkoIA Semi-Organic Image Sensor

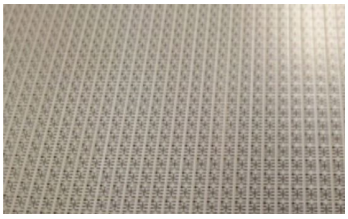


Figure 2.3: One of PragmatIC organic and flexible products

In the last years, it has been possible to see many examples of how the industry begun to give use to the innovations in the field. It was possible for Sony to release in 2007 the first full Organic Light Emitting Diode (OLED) TV, as thin as 3 millimeters Fig. 2.1. One of the characteristics that this new market has been showing, relates to its openness to small-medium size companies. The start-up NikkoIA, is currently commercializing visible and infra-red image sensors based on the combination of quantum dots and organic materials [21] Fig. 2.2.

Low temperature, flexible and solution processed logic circuitry, cannot compete with current inorganic products in terms of performance, however when the focus is cost per area and flexibility, organic and printed electronics can indeed be competitive. PragmatIC Printing Ltd, plans to produce 10 million flexible, solution processed logic circuits until the end of the current year [22] Fig. 2.3, addressing the needs of its customers, such as De La Rue - the largest producer in the world, of high-security paper and printing technology, covering around 150 national currencies

[23].

The potential that this new market exhibits (estimated to be worth almost 10 times more in 2025 that in 2005), as referred in the preface of [16], has been attracting the attention of many industrial and political organizations.

The European union has been aware both of the forecasted possibilities for this market and the foreign threat of losing future market share for EUA and Asia. The Seventh Framework Programme (FP7), a founding mechanism in Europe (2007-2013) has created 4 specific programs/instruments to address funding issues on organic and large area electronics, namely:

PolyNet - Network of Excellence for the Exploitation of Organic and Large Area Electronics;

OPERA - Organic/Plastic Electronics Research Alliance;

PRODI - Manufacturing and Production Equipment and Systems for Polymer and Printed Electronics;

PolyMap - Technology Roadmap of Processes and Materials for Organic Electronics;

In the period of 2007-2011, the investment that these programs have provided to specific projects, reached 120 million euros[20].

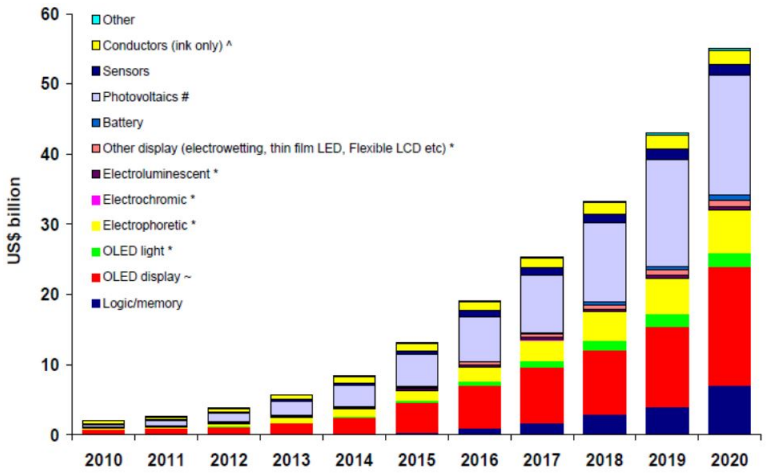


Figure 2.4: IDTechEx projected market growth, as appears in [1]

Acknowledging the opportunities predicted for this market, many companies are gathering information and knowledge as well as exchanging experiences in various associations. One of such examples is the Organic and Printed Electronics

Association (OE-A), founded in December 2004, that claims to be "the leading international industry association for organic and printed electronics", which has now more than 200 members in 31 countries [24].

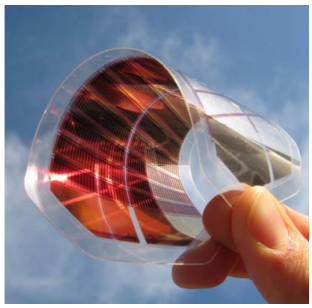


Figure 2.5: Fraunhofer's flexible photovoltaic module

Figure 2.6: Enfucell's thin, flexible and ecofriendly "SoftBattery"

Figure 2.7: Varta's fully printed, thin and flexible battery

As also mentioned in a third party study (by IDTechEx) used in [1]Fig. 2.4, the field promises a pronounced growth, wherein organic photovoltaic and OLED displays share the majority of the market.

Although organic solar cells still have lower efficiencies than their inorganic counterparts, there are currently many research efforts to change this fact. Many of these research efforts are meaningful enough to be mediatized as in [25], where an efficiency of 18,5% has been achieved, also in [26],[27],[28], all from 2013, are exposed different approaches that led to improvements in performance. In[29] (also from 2013) are given some strategies that may help to reduce the production costs of organic solar cells.

Working prototypes of printed batteries (Fig. 2.6 and Fig. 2.7) and solar cells (Fig. 2.5) have also been presented by OE-A partner companies [17].

Released in 1971, the Intel 4004 was a co-development of Intel and a Japanese calculator manufacturer, Busicon. It was the first microprocessor to be released on the market. It had a 4-bit architecture, 2300 P-MOS transistors and ran at a frequency of 740kHz. This microchip project started as an industry request, to be the core of the calculator "Busicon 141-pf". At an inflated price, it would cost today around 70US$, or roughly 50€ [30]. Today, the fastest microprocessors, as Intel Core i7-3970x Extreme, have faster clock frequencies, higher number of transistors, lower power consumption per transistor and a cost per transistor that is many

orders of magnitude lower when compared with the 4004 microprocessor. In 2012, Kris Myny [31] presented the first organic microprocessor constructed in a plastic foil, using pentacene as an organic P-type semiconductor. The average mobility difference between pentacene (<1 cm^2/V. s) and P-type (<400cm^2/V. s) silicon is considerably high and, the device that was created reflects these differences. A short comparison between these three examples is shown in Tab. 2.1, where some general characteristics can be compared, as VDS, Transistor Count and Instructions Per Second (IPS). Also of relevance, is the topology of the transistors used in the organic microprocessor - the authors decided to implement a dual gate configuration - which is described as the best method to fine-tune the threshold voltage, at the cost of increased circuit complexity.

	Intel 4004	**Ref.**	**Intel i7-3970**	**Ref.**	**Kris, 8-bit Proc.**	**Ref.**
$VDS_{typical}$	30V	[32]	0,6V -1,35V	[33](7. 5. 1)	20V	[31]
Current	30mA (med.)	[32]	135A (max)		—	–
Power	0,9W (med)	Calc.	130W (max.)		100μW@10VDD	[31]
Architecture	4-bit	[32]	64-bit	[34]	8-bit	[31]
Transistor Count	2300	[32]	$2{,}27\times10^9$	[35]	3381	[31]
Process	10μm P-MOS	[31]	32 nm CMOS	[34]	5μm	[31]
Clock	740 kHz	[32]	3,5 GHz	[34]	40Hz	[31]
Instructions/s (theoretical)	$9{,}26\times10^4$ IPS	[32]	$>2\times10^{10}$ IPS (6core*3,5G)	Calc.	40 IPS	[31]
Chip Area (die size)	12 mm^2	[32]	434 mm^2	[35]	[1,96×1,22]cm^2	[31]
Cost Today **(Consumer)**	70 USD	[30]	1000 UDS	[34]	—	–
Cost/Transistor (Consumer)	0,03 USD	Calc.	0,000 000 44 USD	Calc.	—	–
Chip Cost/cm^2	583,3 USD	Calc.	232,56 USD	Calc.	—	–
Power/transistor (average)	196 μW	Calc.	77,4 nW	Calc.	30nW	Calc.

Table 2.1: Short comparison between silicon and pentacene microprocessors

3 Printed Electronics

In this chapter, the most common processes and materials that are being used in printed electronics (PE) will be evaluated: firstly, each process will be described as well as some of its advantages and disadvantages; secondly, the materials that are most commonly used in printed electronics will be reviewed and their main advantages and disadvantages highlighted; finally the last section of this chapter will resume the main ideas. In Fig. 3.1 a schematic representation of the processes and materials in printed electronics is given. This is not the only possible representation, and less common processes could be added. In the branch of materials, a topic that will not be covered is the one relating to "Special Function". This topic aggregate materials with piezoelectric properties, chemical sensing properties, materials capable of deformations (acting as actuators), among others.

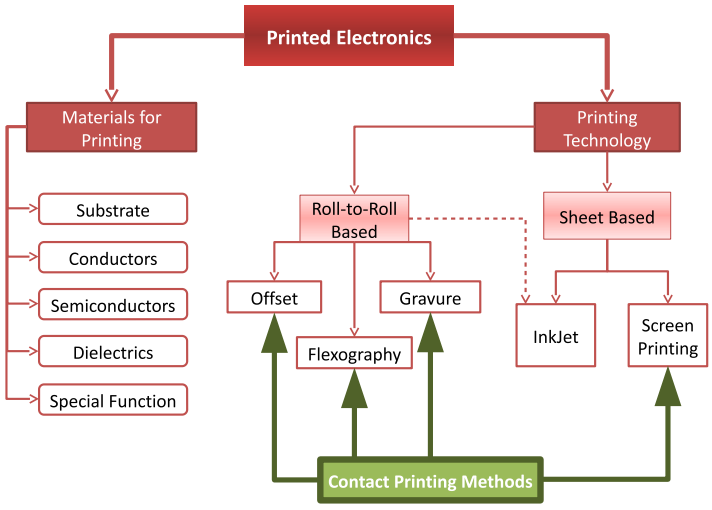


Figure 3.1: Common hierarchical representation of the PE processes

3.1 Processes and Techniques

Although printed and organic electronics are generally used interchangeably, these two terms are not quiet the same. In general, PE refers to a set of processes, meth-

ods and techniques that have been used (and still are) in the graphics industry - generally to print books, newspapers, food packaging, etc. - and that are now allowing electronics to be created in diverse substrates. Organic electronics is regarded as an area in which organic materials are used, whether or not deposited by PE, and the frontier between organic and hybrid devices is not entirely clear. Inorganic electronics can also be achieved using PE, as reported by Harting, et al. [36], where silicon nanoparticles (in suspension) were processed in solution with screen printing, producing transistors with mobilities between 0,3 and 0,7 cm^2/vs.

One of the main advantages of PE, is the low temperature and usually no vacuum [19] (pp. 6) required by the process, including the sintering and annealing stages. In terms of cost, printed electronics is expected to become a relevant player in large area/low-medium performance, where the cost per area can compete directly with silicon, even amorphous silicon (a-Si). The following, are the most relevant set of processes and related techniques that are expected to lead PE to mass production of low cost electronics, whether or not fully organic, flexible, green and disposable.

3.1.1 Offset Printing

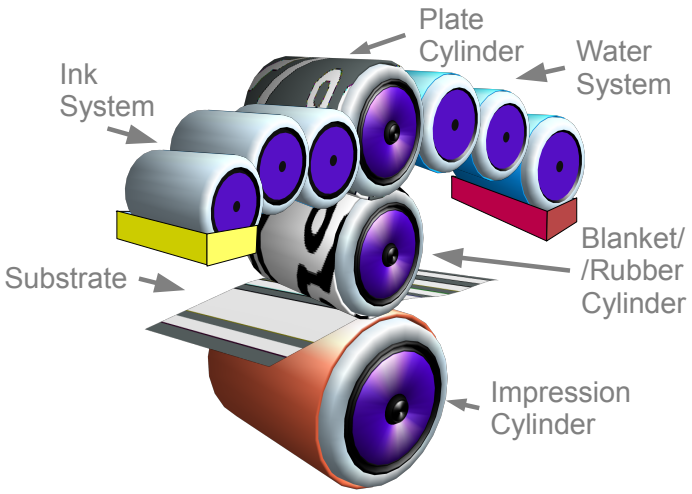


Figure 3.2: Schematic representation of the offset printing process

This process is based on hydrophilic and hydrophobic properties.

Although the image is formed in the plate cylinder, an intermediate roll (rubber/blanket cylinder) is used to transfer it to the substrate, with the support of the impression cylinder.

As argued by [37], the process itself is very complex, as the image to be formed in the plate cylinder requires a sensitive calibration of various parameters.

The plate cylinder has a pattern in its surface of different surface energies, which creates areas that are hydrophobic and lipophilic and others that are hydrophilic and lipophobic[1].

Connected to the cylinder are two independent systems providing, by means of roll-to-roll distribution, a thin, smooth and uniform layer of water and oil-based ink. Each area of the plate cylinder surface attracts only to itself water or oil based-ink, depending on its surface energy.

In [38] is underlined that the term "offset" comes from the offsetting of the printed image from the plate cylinder to the rubber/blanket cylinder and only then to the substrate. All the usual elements in this system are represented in Fig. 3.2.

3.1.2 Flexography Printing

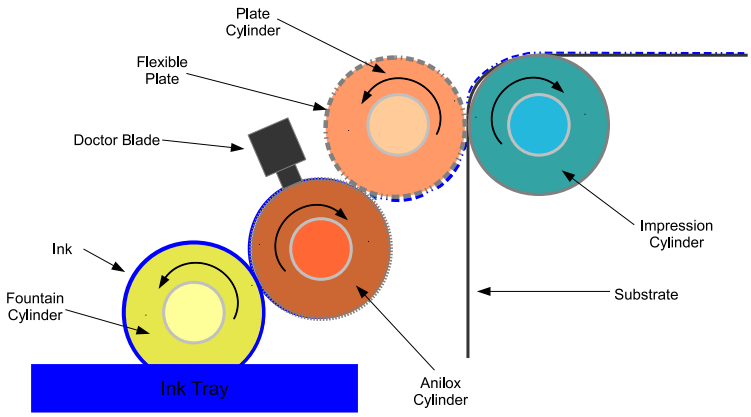


Figure 3.3: Flexography Printing process scheme

The flexographic process has several rollers with distinct functions, and other auxiliary components. The plate cylinder, is the last roll to come into contact with the ink. In order to ensure that the needed amount of ink reaches the outer surface of the plate cylinder, its previous cylinders must supply it - just the needed quantity and in the right manner. Wrapped around this cylinder, is the flexible plate or image plate, which is made of rubber or other similar material. The Image plate

[1]Rejection of "fats" and "oils"

is a 3D surface responsible for the pattern to be printed and, in fact, this is the surface receiving the ink in its higher relief parts. Preceding this cylinder, and in contact with it, is the "Anilox roller". This is the roller responsible for conducting the ink to the flexible plate of the plate cylinder, following the previous demands of ink control. This anilox cylinder, has an engraved texture, consisting of thousands of small holes. The anilox works together with the "doctor blade", which is simply a tool to wipe off the excess of ink in the anilox roller, leaving only ink in the holes. Capillary forces[2] keep the ink stable in the holes of the anilox. Between the anilox cylinder and the "ink tray", it is located the "fountain cylinder" which is responsible for continuously soaking ink from the ink tray. All this process is schematically represented in the diagram Fig. 3.3.

3.1.3 Gravure Printing

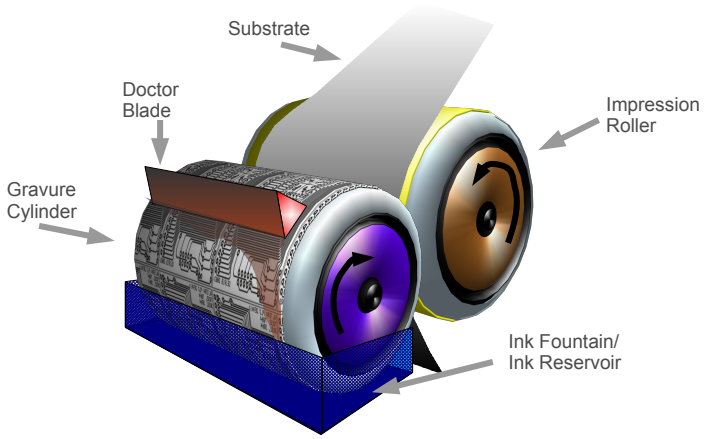


Figure 3.4: Gravure Printing process representation in perspective

The fundamental key unit in the gravure printing process is the rotogravure cylinder. The image patterns are engraved into its surface directly, but some rules apply to this engravement. The image elements that are engraved and lay bellow the original level will form small ink deposits that are transferred to the substrate. The ink deposits – image elements – are periodically spaced and, always between two consecutive image elements, a higher triangular non image area splits them.

Although this non image area is always present – so that small ink deposits can exist – a continuous tone is possible, as this non image elements can be reduced

[2]Capillary forces manifest themselves in some liquids. Water, for example, is capable of climbing up porous materials such as paper, against gravity, soaking them.

to a minimum height, or equivalently, the image elements can have a larger area percentage reserved. To make the continuous tone possible, the ink has to spread a little, as it is dot-deposited in the substrate. This print cylinder rotates partially immersed in the ink fountain and picks up the ink that fills its engraved cells.

As the image elements lay bellow the surface level of the cylinder, a doctor blade that is in contact with the cylinder wipes of the excess ink from its surface. The image cylinder comes into contact with the substrate and, with the help of the impression roller, a pressure is created that facilitates the ink transfer[39]. Additionally, an auxiliary technique is referred for non-metal, non-conductive inks where an electric field is created between the two rollers, lifting the ink in the image elements reseeds - thus helping ink transfer process.

An illustrative representation of the common elements in this process are pictured in Fig. 3.4.

3.1.4 Screen, Stencil and Rotary Printing

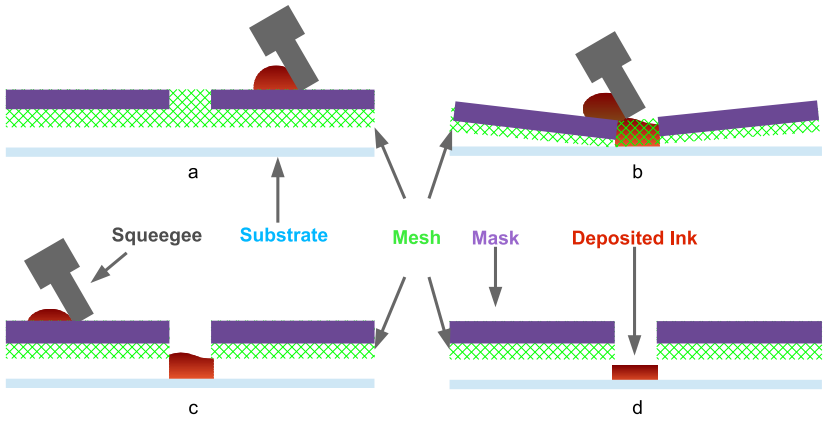


Figure 3.5: Screen Printing process representation. a) ink deposited; b) mesh-bending and ink deposition c) ink stabilization d) deposited ink

Screen and stencil printing have both the same working principle. Fixed by a frame, a mesh that is only permeable in the areas where a mask does not exist, lays above the substrate.

In the case of screen printing, both the mask and mesh (that usually are a single component) are flexible and separated from the substrate.

In case of the stencil, the mask does not bend and the structure is in direct contact with the substrate [38].

The rotary screen uses the same principle but the mask is wrapped around a cylinder that contains inside the ink to be transferred to the substrate [39].

Screen and stencil use a squeegee to force the ink through the mask openings. A blade is the equivalent to the rotary screen. For screen printing process, a schematic representation is shown in Fig. 3.5.

3.1.5 InkJet Printing Process

The main objective when using inkjet printers, is to pattern the subtract according to some digital design. The majority of the knowledge related to fluid behavior in the inkjet printing field, has been accumulated due to general printer development and commercialization[3]. At this level, the aim is to be able to generate textual and/or photographic documents. When transiting from these traditional fields to others, where the objective is no longer to create visible images or text, but precise designs of very small dimensions, more control over independent variables, higher resolution and precision, is needed.

According to B. Derby, 2010 [40], the versatility of inkjet printing reflects "the accurate placement of picoliter volumes of fluid on an arbitrary substrate". To be able to use a printer to create thin films with functional materials (e. g. insulators, semiconductors, conductors, piezoelectric), it is important to understand the way these fluids behave just before leaving the printer nozzle until reaching and stabilizing on the substrate. Nowadays, printers specially designed to these tasks begin to be available, with capabilities to deal with the particularities of functional inks. These printers differ from the traditional ones by allowing the user to access individual parameters, such as applied pulse shape (to drop formation), ejected drops per second, print head velocity, substrate temperature, print head distance from the substrate, etc.

In order to achieve the desired designed pattern, several topics must be taken into account. Derby divides them in 3 (quoting):

1. Generation of droplets;

2. Positioning of and interaction between the droplets on a substrate;

3. Drying or other solidification mechanisms to produce a solid deposit;

[3]Much of this knowledge has been acquired by trial and error

For general interest in the process, only the first item will be concisely reviewed. The last 2 items can be ascribed to the general dynamics of the flight, settle and curing of the droplets in the substrate.

3.1.5.1 Drop Formation

Two main inkjet printer systems are available today. Drop on Demand (DOD) and Continuous Ink Jet (CIJ). According to G. Cummins et al, 2012 [3], CIJ is less frequently used. One of the reasons that lead the preference of DOD systems in detriment of CIJ, is the particularity that the latter exposes ink to air, as the unused droplets are recollected during the flight. As many inks start to degrade once exposed to air, this type of system is less suitable for jetting functional inks.

For DOD systems, two methods for generating the droplet are common and, again, one of them is less recommended. Driving from the main ink reservoir to the print head, the ink stands still behind the printing nozzle. For the ejection to occur, an internal and brusque variation of pressure must happen. Commonly, thermal or piezoelectric actuators are installed. Thermal actuators, upon receiving the necessary energy pulse, heat up and boil a small amount of ink near them. This heated ink expands in a gas bubble. This fast volume variation, leads to a pressure increase in the region near the nozzle and, consequently, the ink near the nozzle is expelled, offsetting the pressure difference between the interior and exterior of the chamber. Afterwards, the actuator cools down and the bubble disappears, creating a negative pressure that helps the chamber to refill, and the process can star over.

Piezoelectric actuators have a similar operation but, instead of indirectly creating a pressure gradient, they act directly on the ink. These actuators deform themselves upon receiving the necessary energy pulse and, in this manner, provide similar transient pressure consequences to the ink.

In the same manner some inks degrade once exposed to air, others change their properties once exposed to certain temperatures. Inkjet printers with thermal actuators are not suitable for all types of inks, and are thus usually used with inks supporting these thermal particularities.

3.2 Materials for Printed Electronics

Printed processes may be designed to allow certain devices to be attainable, but not less important, is to understand that not all materials in solution can be safely

processed atop of each other, for example in thin-film devices. The study of the available materials and which solvents better dissolve them or yield most favorable results is also a key element. Although the importance of this subject cannot be underestimated, in this section the main focus will be on materials and not its solvents - which are not in the scope of this section, nevertheless this remains an issue deserving to be further explored.

Organic materials have been enabling numerous demonstration concepts of organic electronics to emerge in the market, either with printed electronics, or other deposition methods, as evaporation. This section will be mainly addressed to solution processable materials, which are required by printed electronics, and it is also intended to highlight the main applications, inconvenients and solutions within the materials. It will be also referred those considered across the literature as the most relevant and prominent materials in each section. In Fig. 3.6, a suggested hierarchy of materials for printed and organic electronics is schematically expressed - the following sub-sections will be based on this segmentation.

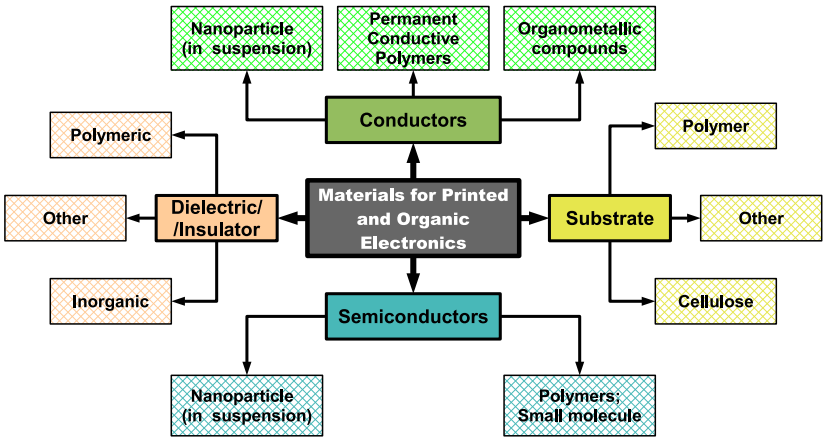


Figure 3.6: Suggested hierarchy of printed and organic electronic materials, based on [2] and [3]

3.2.1 Conductors for PE

Parallel to the field of PE, Direct Writing (DW) or Digital Writing technology has been receiving increasing attention. DW technology as referred by [41] is a set of additive on-demand processes for material deposition, within which InkJet printing and other Jet processes play an important role. Gerard Cummins et al. [3] have reviewed the main classes of materials for inkjet printing process, as well as the process itself. According to Cummins, the conductor materials can be divided into colloidal suspension of nanoparticles, organometallic compounds in solution and conductive polymers. This subdivision will be kept for simplicity, and the inks will be described in the usage perspective of the InkJet printing - nevertheless it is coherent to assume that the adaptation of the viscosity, surface tension and other tunable parameters of the solution, would validate it to other processes.

3.2.1.1 Nanoparticle Inks

Nanoparticle inks can be produced in high quantities and prepared to be dispersed in high concentrations. In order to form a conductive track - which is the final objective of many nanoparticle inks - these inks must be sintered after deposition. The objective of the sintering process is to melt the particles together, while releasing them from the additives in which they have been suspended. These additives such as dispersants, adhesion promoters, surfactants, stabilizing agents and so on, were firstly used to allow the ink to be properly jetted (assuming the InkJet printing case) and allow the particles not to interfere negatively with the process. These particles possess a favorable property of having a large superficial area and a very small size ($<$ 100th the size of the nozzle). This allows them to sinter at much lower temperatures than the bulk material.

Some of these nanoparticles are difficult to stabilize, and as a secondary effect, they will tend to agglomerate together. This is especially critic for the ink inside the deposition chamber in case of inkjet printing. These agglomeration can lead to the block of the nozzle, or a defective jetting, as the ink becomes more viscous. One way to address this issue consists of applying a polymer coating that will prevent agglomeration. These polymers have the unfavorable characteristic of requiring high temperatures to be removed (300^{o}C), which in many cases are incompatible with plastic/ flexible substrates. Cummins advocates that a combination of photonic or microwave flash sintering as an intermediate stage, could lower the temperature

requirements by the final thermal sintering process.

Another advantage related to nanoparticles is their superior electrical conductivity and air stability when compared with polymer conducting coatings. These particles only show, however, a small fraction of their bulk conductivity values.

Among the most commonly used conductive nanoparticles, there are those from the periodic groupe 11: Cu, Ag, Au, and Nickel, from group 10.

Gold and silver nanoparticles are the ones presenting higher chemical stability, lower chemical reactivity and electrical conductivity, although these are somewhat expensive materials.

Copper and Nickel nanoparticles demand extra care to be used. Again, according to Cummins, these inks have already been prepared for inkjet printing. Their disadvantage is the air instability, which can lead to a reduction of their lifespan unless they are blend with specialized coatings or processed in inert atmospheres.

Cummins considers graphene and carbon nanotubes (CNTs) in suspension as special inks, and not nanoparticle inks. For simplicity and assuming their sizes to be comparable to metal nanoparticles, they will be listed in this section. Schwierz (2013) [42] states that graphene can be regarded from various perspectives. It is a gapless[4] ambipolar semiconductor consisting of carbon atoms connected in a single layer hexagonal pattern. Although it is a semiconductor, its special nature allows it to be used in suspension (in water for example) as a conductive ink. Cummins advocates that after deposition, conductivities can be partially restored by chemical or thermal reduction, although the needed temperatures far exceed 500^{o}C, limiting the available strategies to raise its conductivities for flexible electronics.

CNTs are, as graphene, graphite and diamond, composed of carbon atoms - these are arranged in a tubular disposition. They can be composed of a single or more than one sheet of rolled up graphene to a cylindrical form. Multi walled carbon nanotubes (MWCNTs) always have metallic properties and single walled carbon nanotubes (SWCNTs) can have metallic or semiconducting properties. Whether or not semiconducting SWCNTs are among conductive ones, if the CNTs are to be used as a conductive ink, those with semiconductor properties will not reduce significantly the conductivity[5]. CNTs possess high current density and thermal conductivity, which makes them a possible alternative to other conductive flexible

[4]Large area graphene does not possesses a bangap and behaves as a semimetal. The valence and conduction band touch in a single point, the Dirac point.

[5]If the target was to use them as semiconductors, it would be necessary to eliminate those among them which were conductors

solutions.

3.2.1.2 Organometallic inks

Organometallic compounds are characterized by the existence of bounds between carbon and metals. According to Bojun Xu[43], pp. 30-31, organometallic inks can be achieved by the dissolution of "(...) an appropriate organometallic salt into a volatile organic solvent to provide the essential rheological properties (...)". The objective at this point is to evaporate the solvent, decompose the ink in such a manner that the metal bonded with carbon may be released, compact these metal particles with each other for an aggregation and melt them together. Organometallic, graphene and CNTs are not always regarded as PE materials due to the required temperature for them to achieve an acceptable performance (150ºC-500ºC). They are, nevertheless included in DW technology because an inkjet can print on a great variety of substrates, including rigid/inflexible substrates. Bojun (pp. 30-31) and Cummins refer whatsoever that there are some sintering techniques capable of using these inks without significant damage to the substrate. Among these, microwave sintering, laser sintering, chemical conversion, UV radiation and plasma treatment are mostly referred. Aziz Shaikh [44] has released a patent filled in 1997 and approved in 1999 that describes a process of achieving, with organometallic inks a thin film with a layer thickness of 1,5 micrometers.

In case these inks are used for inkjet printing, an advantage is that these inks are on solution rather than on suspension form, thus reducing the probability of nozzle blocking (as may happens with many nanoparticles that tend to stick together).

The main disadvantages pinpointed to the needed sintering step - when processing these inks - are the emitted gases, the high temperatures and, many times, the necessity to heat up the whole structure.

3.2.1.3 Polymer Inks

Since the discovery in 1977 that specially doped polyacetylene could have its internal conductivities improved by several orders of magnitude, the research in the field produced other polymers and derivations.

Nowadays, and accordingly to [2] three main conducting polymer groups are of special interest, namely, polythiophenes and its polypyrroles (PPy) derivatives, polyaniline (PANi) and polymers mixed with nanoparticles such as gold, platinum,

transition metal oxides or carbon nanotubes. In this last group, the polymer with which the nanoparticles will be mixed can be insulating or conductive, depending on the desired properties. An important derivative of the polythiophene group is the conjugated polymer poly(3,4-ethylenedioxythiophene) or simply PEDOT, which has conductivities in the order of 170 S/cm. Heraeus as an example, commercializes a formulation based in PEDOT that is of greater convenience for solution processes - poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) or PEDOT:PSS, by the name Clevios^{TM}. They claim that their various formulations - with changes in viscosity - have a correspondent conductivity ranging from 30 to 1000 S/cm. In Tab. 3.1, a set of materials is given along with their typical conductivities for comparison.

Material	**Conductivity**		**Resistivity**
	$[(\Omega.cm)^{-1}]$ or$[S/cm]$	$[(\Omega.m)^{-1}]$ or $[S/m]$	$[\Omega.m]$
Silver	$6{,}3\times10^{5}$	$6{,}3\times10^{7}$	$1{,}59\times10^{-8}$
Copper	$5{,}85\times10^{5}$	$5{,}85\times10^{7}$	$1{,}7\times10^{-8}$
Gold	$4{,}25\times10^{5}$	$4{,}25\times10^{7}$	$2{,}35\times10^{-8}$
Graphite	1000	10^{5}	1×10^{-6}
Germanium	$2{,}2\times10^{-2}$	2,2	$4{,}55\times10^{-1}$
Silicon (intrinsic)	$4{,}3\times10^{-6}$	$4{,}3\times10^{-4}$	$2{,}33\times10^{3}$
Polymethylmethacrylate (PMMA)	$<10^{-14}$	$<10^{-12}$	$1{,}00\times10^{11}$
Polyester	10^{-16}	10^{-14}	$1{,}00\times10^{13}$
Diamond	$<10^{-16}$	$<10^{-14}$	$1{,}00\times10^{13}$
Glass (silica)	$<10^{-18}$	$<10^{-16}$	$1{,}00\times10^{15}$

Table 3.1: Comparison between the conductivity of different materials based on [5]

According to B. Weng et. al. [45], PANi, PPy, and PEDOT are known to be insoluble. This has led various investigation groups to various approaches, trying to reach a possible solution. A usual solution to the problem has been to deposit these polymers by electrodeposition, but for applications in PE, the desired form is in solution (either in water or an organic solvent). This was achieved with PEDOT by the polymer mixture of PEDOT and PSS. As for the other polymers, sometimes chemical alterations and organic solvent-based inks are possible but when that is not the case, an alternative approach has been to create nanoparticles of that polymer, which are then dispersed in aqueous solutions, and this approach, again according to [45], was already used with polyaniline.

In a work published in the PNAS by Joung Yoo, et. al. [46], they experimented

with a technique called "solvent annealing". As the dispersions of polymer nanoparticles (as polyaniline), do not provide the "bulk" conductivities of the material - nor other mechanisms that render water dispersibility such as polymer acids - the use of these polymers in solution has been cautious. Regarding this issue, the authors report a conductivity increase of 835-fold for PEDOT:PSS deposited from solution after an annealing process in which vapors of dichloroacetic acid were present.

3.2.2 Dielectrics for PE

There are many non-conductive polymers that can be processed in solution and, among them, various are compatible with PE. According to [2], the most common are "(...) poly(methyl methacrylate), poly(vinil phenol) and other polyesters, polyvinil alcohol, polymides, silicone network polymers and parylene". Usually, poly(methyl methacrylate) is also referred as PMMA. In organic electronics, their main applications are as dielectric layers in thin-film transistors and in this particular field, it is common to use two polymer layers in which one grants high capacitance and the other present a more favorable interface for the growth of organic semiconductors (OSCs). Another relevant use for these polymers is in capacitors. The insulating layer tends to be chosen according to designed capacitance and break down voltage. Also in the view of Ming Yu Shi [38] and Bartzsch et. al. [47], the double layer interface in organic semiconductors has two main objectives, each one relating to the respective layer. The first is to provide a low-k layer material that favors the growth of larger OSC crystals and, the second, is intended to provide a higher capacitance and insulation, with a high-k material. In this last layer, a barium titanate oxide has been reported in [47]. This last layer allowed the transistor to reduce its threshold voltage.

3.2.3 Semiconductors for PE

Research in the area of polymer and small molecule semiconductors has grown to such an extent that at the present time it is possible to find hundreds of P-type OSCs[6]. Two figure of merit for comparison that have been used within the area of PE are the mobility of amorphous silicon ($10cm^2/V.s$) and amorphous silicon hidrogenated (a-Si:H), applied to field effect transistors (FET)[7] that rounds $1cm^2/V.s$

[6]Contrary to P-type, there are much less availabele N-type organic semiconductors

[7]The mobility can be a somewhat ambiguous figure if not clarified. The two main tests for the mobility of a material are the "time of flight" which is measured in a small sample of the

[48]. Although improvements to OSCs mobility is regularly reported, either by improvements in the fabrication process or by the development of new materials, its reported values when processed on solution round 0,2 to 1 $cm^2/V.$ s according to [49], pp. 74. A-Si has a relatively low electrical performance due to its atomic disposition - for the same area, the material presents larger amounts of much smaller crystals when compared to nanocrystalline, polycrystalline or single crystal silicon. Due to the lower temperatures required for deposition[8] and its lower price, a-Si has been used in the display sector, as it is also compatible with large area.

When using inorganic semiconductors, the practice to achieve N or P type conduction is by doping. It is known that only small amounts of doping agents are necessary thus clean rooms are needed to prevent - among other events - the accidental and uncontrolled doping with impurities in the air. The doping process in organic semiconductors does not render good results according to [50], and these materials usually become conductors with the increment of the doping agents as they are (naturally) "intrinsically degeneratively doped with large amounts of impurities"[9]. The purification of these materials, has been performed to some extent but again according to [50], it is purposeless as PE does not have to operate in clean rooms, and to some extent, contamination does happen.

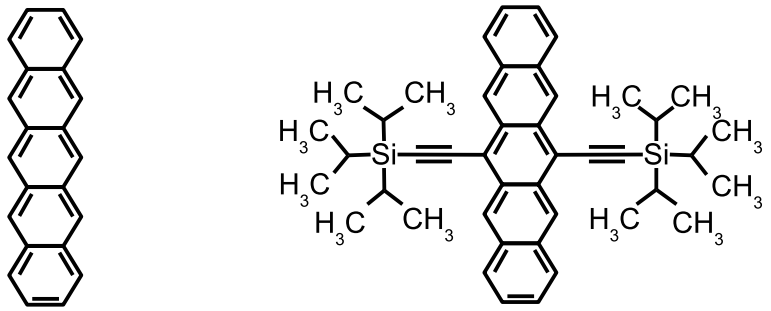


Figure 3.7: Comparison between small molecules of insoluble pentacene (left) and soluble TIPS-pentacene (right)

With the focus in PE, solubility is of great importance but regarding semiconducting materials, the problem is that most part of them are naturally insoluble.

semiconductor molecule only, and the mobility of a device that uses that material. The last is always slower.

[8]The deposition process does still need a low pressure inert atmosphere and clean rooms, thus creating some barriers to its use in flexible or PE approaches, although some applications start to appear [48]

[9]Organic semiconductors are chemically created as P or N type

Chemists have been working on this issue and currently, there are two main strategies to grant solubility to small molecules according to [51], adding either side chains to the core molecule or, thermally removable groups to the same core molecule. Pentacene is one of the most widely used P-type small molecule organic semiconductor and, as many others, its core molecule (formed by 5 benzene rings) is insoluble. In Fig. 3.7 two forms of pentacene (insoluble and soluble) are shown. The difference between the two molecules is in the side chains, which grant solubility to the second molecule 6,13-Bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene). Polymers can also be engineered with side chains - in [2] is stated that "thiophene copolymerized with single and fused-ring comonomers (...) side chains, promote self-assembly (...) and thereby charge carrier mobility".

Although polymer semiconductors usually have lower mobilities than small molecule semiconductors (such as pentacene), they possess some advantages as well. Zhang and co-workers [51] pointed three main advantages that polymers offer when compared to small molecule in practical applications (citing):

> (1) uniform thin film fabricated from solution and the small variation of device performance for the different devices;
> (2) excellent rheology properties. Viscosity and surface tension of polymer solutions are more suitable for printing techniques;
> (3) good mechanical strength;

As happens with conductive polymers, the "post solvent annealing" or "solvent-assisted annealing" technique is also used with some OSCs in FETs, as reported in [52] and [51]. Both report on works done with TES-ADT, where post deposition annealing helped to improve crystallization and consequently the mobility. It was equally found that the solvent in which the OSCs are diluted has an important role in the mobility of the thin-films created. Dimitrakopoulos et. al. , reported[11] on works in which regioregular P3HT has been found to vary its mobility by two orders of magnitude, depending on the solvent used, and the best results were observed with chloroform.

To date, most of the higher performance and more stable semiconductors are P-type. N-type semiconductors have been showing considerable instability when exposed to air and/or moisture, and Dimitrakopoulos links this fact to some instability that anions present when exposed to air. P-type OSCs also exhibit this behavior

but generally, not so pronouncedly. According to U. Zschieschang et. al. [53], even pentacene that is regarded as one of the most stable OSCs slowly degrades when exposed to air. In Fig. 3.7 - previously referenced - each one of the 5 aromatic benzene rings has some unlinked terminations, and these are originally connected to one Hydrogen atom each. Once exposed to air, some of these Hydrogen atoms begin to be replaced by Oxygen atoms and again according to Zschieschang, the substance changes to 6,13-pentacenequinone. The problem is that Hydrogen used to link itself by single bonds and Oxygen links with double bonds, thus changing the molecular balance, including its Highest Occupied Molecular Orbital (HOMO) energy and the Lowest Unoccupied Molecular Orbital (LUMO) energy, which in practice creates trap-sites[10].

3.2.4 Substrate Materials for PE

One of the main requirements concerning the traditional industry of inorganic electronics, is that the substrate is capable of standing high temperatures. This is due to the use of processes that generate a considerably high temperature, exceeding the allowed limits of common plastic materials, as an example.

One important characteristic that polymers present, is the maximum temperature they can be subjected to without experiencing deformations or degrading. Adapted from [6], the following table, Tab. 3.2, expresses this critical and other characteristics for some of the most used plastic substrates in printed electronics . Moisture absorption, is also another relevant characteristic of the substrate material. Many OSCs, for example, tend to degrade when exposed - over days to weeks - to oxygen and moisture. Even if a device containing an OSC is created and encapsulated, the wrong choice of the substrate can nevertheless condemn its functionality.

[10] Trap-sites in the material with different energies, have to be filled up first before a stable conduction can happen. The gradual appearance of traps (in addition to those initially present), usually leads to changes in the threshold voltage of FETs, as well as a decrease in its mobility - its worth noting that the number of molecules carrying charges in the material decreases, as some molecules change to other substances.

Material	Max. Temp. [ºC]	Color	Chemical Resistance	Thermal Expansion Coef.	Cost	Moisture Absorption
(Kapton) Polyimide	250	Orange	Good	High	High	High
(PEEK) Polyether-etherketone	240	Amber	Good	-	High	Low
(PES) Polyethersulfone	190	Clear/ Limpid	Poor solvent resistance	-	High	Moderate
(PEI) Polyetherimide	180	Hazy/ Turbid	-	-	High	-
(PEN) Polyethylene Naphthalate	160	Clear/ Limpid	Good	Moderate	Low	Moderate
(PET) Polyethylene terephthalate	120	Clear/ Limpid	Good	Moderate	Low	Moderate

Table 3.2: Maximum process temperature for some organic substrate materials, based on [6]

3.3 Chapter Highlights

In a growing area as PE, many challenges have to be overcome and requirements met. In regard to the printing processes and associated materials, it would be desirable to approach several idealizations. Some of these would be: small feature size; high precision/confinement of the ink; perfect registration between consecutive layers of material; high throughput; controllable material thickness; high material homogeneity; predictability of the process with simulation; real-time analysis of the printing process; real-time optical and electrical test and rejection of defective parts; controllable sintering and annealing - preventing undesirable effects as “coffe-fing effect” [54], perfect jetting (in case of inkjet) without satellites and optimized drop spacing; high semiconductor mobility, low threshold voltage, high Ion/Ioff ratio, ambipolarity, high air stability and flexibility; low surface roughness of the substrate and applied layers of ink; high material flexibility and durability; availability of substrates capable of yielding the previous requirements and be safely biodegradable;

a wide range of dielectric materials with high-k, favorable to the growth of OSCs, with low leakage current and high dielectric strength;

This is a wish-list to what would be desirable to converge, and where many improvements are constantly being made. Fig. 3.8 is extracted from [55] a report conceived by OE-A, and summarizes the actual reality in terms of throughput and feature size.

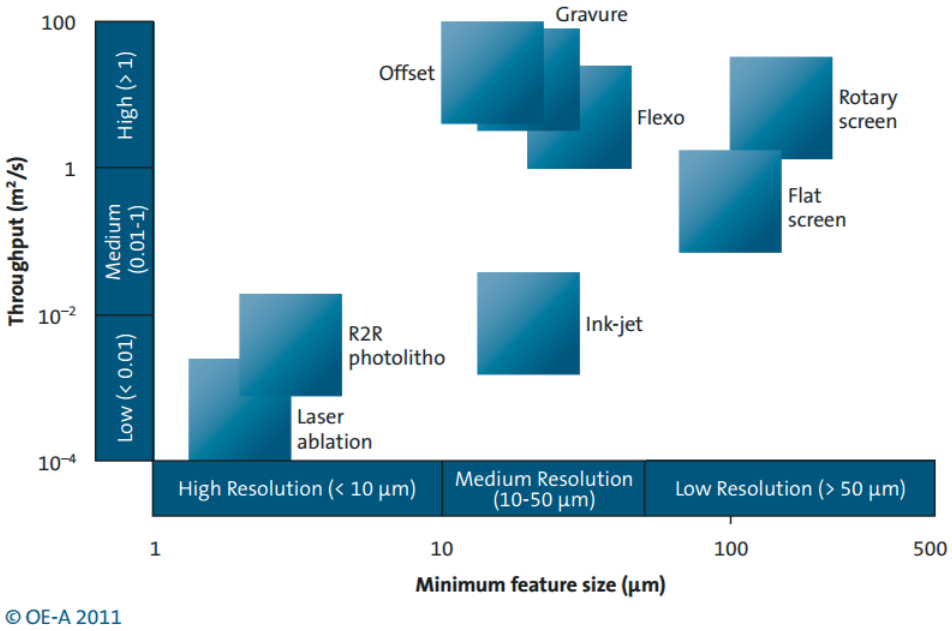


Figure 3.8: Throughput vs. feature size for some typical processes

4 Short & Long Term Problems in Printed Materials

4.1 Charge Carrier Trapping

Apart from memory devices, on which trapping effects are desired, when a semiconductor-dielectric interface is generated - either by using inkjet or other deposition methods - there exist the risk that defects have also been generated. These defects, known as charge traps, can become relevant once the device starts to operate.

According to Madison et al.[56], these could be divided into "chemical impurities, geometric disorder and, if both holes and electrons are present, Coulomb traps".

Sangeeth at al.[57] point the possible trapping sites in OFET. They divide them into the following regions:

1. Metal/Semiconductor Interface;
2. Semiconductor Itself;
3. Semiconductor/Dielectric(Gate) Interface;

They further describe a path to estimate the AC and DC OFET parameters, using a technique in which various light intensities on different wave lengths are used while operating the device and analyzing its response. This technique further allows to quantify the charge traps at several different regions on the OFET structure. The number of traps present in the semiconductor-dielectric interface are, among all the others trap types, those that mostly affect the OFET mobility and Ion/Ioff current. It is further stated that hysteresis is linked to charge traps present on the semiconductor-dielectric interface.

Another OFET parameter that is affected by traps is the threshold voltage. Pasquale et al.[58] discuss the physical origin of the threshold voltage shift. These

"large" value shifts, occur due to the presence of traps, which create punctual electric fields. In order to be compensated, these punctual electric fields demand a gate voltage increase, so that the accumulation layer can still be built on the semiconductor-dielectric interface. Pasquale attempts to clarify the relation between hysteresis and charge traps. The clarification on this matter, according to Pasquale, is meant to provide a faster and less degrading way to quantify the charge traps when compared to the "bias stress method". They conclude that it is possible to estimate the number of traps and to qualify their distribution based on the turning point of the hysteresis plot, which they obtain by applying triangular waves to the gate of the device, while altering the S/D voltage.

Madison, in the previously introduced work, attempts to show the influence of defect sites[1] and trap sites[2] in the behavior of OFETs. Their approach lies on the so called "Monte Carlo" simulations. The authors begin by explaining the initial assumptions, and established conditions for the simulations they performed. This was done in order to establish a comparative overview of the simulated devices, based on their defects. To further enlighten their study, they found it was necessary to create variations in site trap dispersions, generating simulations for heterogeneous and Gaussian dispersions. The energy associated with site traps was yet another parameter which they choose to control over simulations. Both for Gaussian and heterogeneous[3] dispersions, the authors vary the number of traps accordingly, to allow comparisons. The simulated structure was based on a monolayer FET, with a channel of 256 x 1024 sites and, according to the authors, corresponding to a device with W/L=0.25um/1.02um. The considered semiconductor was based on the molecular dimensions of phthalocyanine or pentacene size (which are approximate). It is reinforced that most of the charge transport occurs at the 2D layer closest to the gate of the device, justifying their option for also using a monolayer structure, contrasting to most of the simulations on the area. Madison has found in this work that for heterogeneous trap concentrations, ranging from 0 to 100% of the total structure, charge transport decreases for lower concentrations, reaching its minimum still further away from 100% trap concentrations, contradicting possible expectations. After the minimum charge transport is reached, it then starts to

[1]Defect sites: are unable to accept a charge carrier but instead act as "a wall" to charge transport (structural Impurities)

[2]trap sites: are able to accept a charge but have a different orbital energy (chemical impuries; intentional dopping; mixtures)

[3]Heterogeneous dispersions of traps in the semiconductors, generate geoagglomerations also known as "Islands".

increase as trap concentrations get closer to 100%. It was further shown that there is an increased charge mobility for heterogeneous than homogeneous trap dispersions. It is convenient to notice that the control over trap distributions is hard, and only few groups have had some success partially controlling it.

4.2 Deterioration

N-type semiconductors present several constraints. Their air stability is poor, along with theirs efficiency.

These type of semiconductors have been presenting several difficulties related to its application and usage. Many of them present instability when exposed to water and oxygen. Another of their unfortunate characteristic, lies on their less capable performance, when compared to P-type semiconductors. Pietro et al. [59] presented in their work a new optical spectroscopy technique, which they named Charge Accumulation Spectroscopy (CAS) intended to characterize the degradation of OFETs. According to the authors, their approach lies on the analysis of the different signatures observable on the device, in various operation modes: [Before device stress, during device stress, after device stress] (in vacuum, exposed to air). Comparing the signatures of various operation modes and conditions, they are able to identify polarons[4] that were not previously there and to check if their signature is preserved or not hours after storage of the device. In order to validate their technique, a N-type semiconductor P(NDI2OD-T2)[5] - one of the few that was believed to potentially be air stable - was tested. Pietro constructed an OFET, spin coating the N-type semiconductor to a 50nm thickness. After the application of their technique, they concluded that this N-type semiconductor was unstable for three reasons: firstly, the trapped polarons signature changed to negatively charged HO^- groups after 15 hours of air exposure; secondly, the thickness of the device changed during that period; thirdly, the performance of the device decreased in an irreversible manner when its operation was made in contact to air. On the contrary, the vacuum tested device preserved its initial characteristics with minor alterations.

[4] A charge moving in the lattice creates an accompanying polarization field. This field deforms along the passing charge. In case the charge is an electron, it is accompanied by a cloud of phonons

[5] poly{[N,N´-bis(2-octyldodecyl)-1,4,5,8-naphthalene diimide-2,6-diyl]-alt-5,5´-(2,2´-bithiophene)}

5 Material and Methods

Whether or not the capacitor, the schottky diode and the organic field effect transistor (OFET) are the most relevant components for digital electronics, they undoubtedly are among the most relevant. For organic digital systems, the criteria should also apply. These were the chosen components to be conceived within the field of organic/hybrid electronics. The original planning for each component and the materials that were supposed to be used will be presented as well as the alternative paths that were chosen. The alternative routes will be discussed in this dissertation, but not entirely in this chapter. Intentionally, this chapter has fragmented topics before the "capacitor" sec. 5.9, "schottky" sec. 5.10 and "OFET" sec. 5.11. The purpose is to make possible to jump over the first topics and return to them later if necessary.

5.1 Shadow Mask

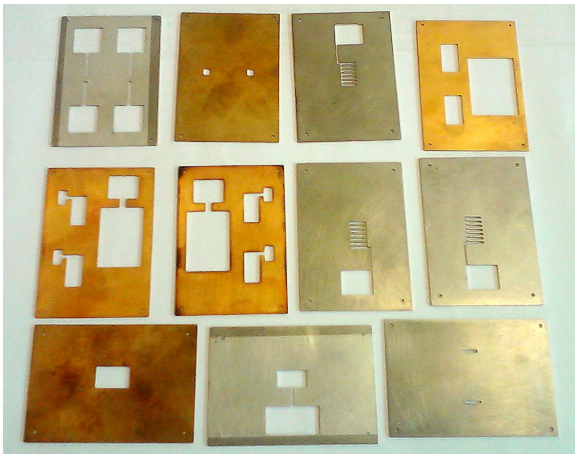


Figure 5.1: Some of the originally created Shadow Masks

It was chosen to use a shadow mask to pattern metallic and contact parts of each component, using a sputtering system (sec. 5.2). To this end, a commercial computer aided design (CAD) system named Rhinoceros® (sec. 5.8.1) was used.

Considering the limited workspace in the sputtering machine, the masks were designed with dimensions of 5cm×3,5cm Fig. 5.1. For each component, the number of masks corresponded to the number of implemented metallic layers, which were two for the capacitor and schottky, and tree in case of the interdigitated OFET.

5.2 Sputtering System

Figure 5.2: Polaron SC502 Sputter Coater

In order to deposit the needed metal layers with the shadow masks, a gold deposition system from Fisons Instruments: Polaron SC502 Sputter Coater Fig. 5.2 has been used. For each layer deposited - regardless of the component - this sputtering system was manipulated to achieve a low pressure between 10-20 pascal[1] while simultaneously, an inert gas (argon) [2] was continuously fed into the low pressure sputtering chamber. The deposition time has been kept with a value rounding 50 seconds. According to the user manual, the formula 5.1 expresses the final film thickness (d) in angstroms[3] as a function of K, I, V and t.

$$d = K \times I \times V \times t \tag{5.1}$$

[1] The pressure at the ocean level in Earth rounds 101 325 Pa

[2] An inert gas or noble has in its outermost electron shell 8 electrons. From this atomic configuration results that the material will not combine with other atoms. As a contrast, Oxygen only has 6 atoms in its outermost shell, and constitutes nearly 21% of the atmosphere, thus invalidating the use of ambient atmosphere at low pressures deposition chambers.

[3] 1Å=10^{-10}m

Here, I is the plasma current in mA, V is the applied voltage in kV (used 1kV), and K is a constant dependent on material being sputtered and the gas used - which is 0,17 in case of the argon/gold combination - and t is the sputtering time in seconds.

5.3 Spin-coater

A common spin-coating system has been used for some thin-film formations. This system could be programmed to vary its rotation speed, the acceleration between different rotational speeds and the time associated with each of the previous steps. The system has three main elements. In order to keep the sample closely attached to the rotational disk, a vacuum/low pressure system is externally connected to the spin-coating system; to power the spin system, an external air compressed system is equally necessary; finally to control the speed, acceleration and time, the system possesses - from origin - a digital console. The system spreads deposited material in solution - atop of the intended sample. The liquid/solution can be deposited before the beginning of the spin process, or just after its start, depending on the particularities of the solution and the sample to be coated. Depending on the previously presented variables (acceleration, speed and time), the resulting film can achieve different thicknesses.

5.4 Paint-Gun

A common air-pressure paint-gun was used to vaporize the PMMA solution creating a thin film in the contact surface. The functional parts of the used air-pressure paint-gun are presented schematically in Fig. 5.3.

5.5 Substrate, Solutes, Solvents and Solutions

In this section, the organic materials used are listed and briefly described.

5.5.1 Substrate

The used substrate for the major part of the implemented work consisted of soft sheets of polyethylene therephthalate from GoodFellow. This polymeric material is

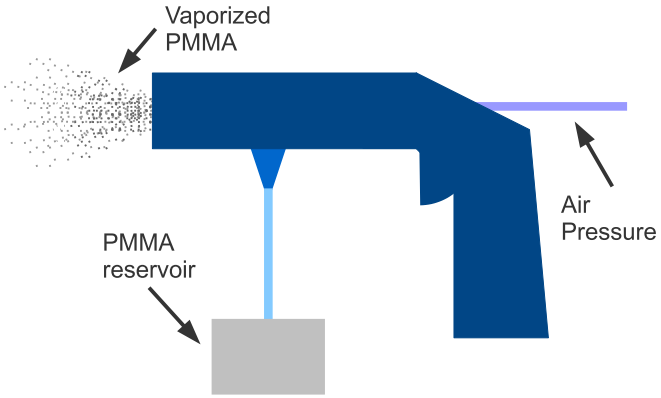


Figure 5.3: Air-preasure paint-gun

also known as PET or polyester, and its properties can be consulted in Tab. 3.2. The used PET sheets had a thickness of $50\mu m$.

For the capacitor only, a commercial and inexpensive aluminum foil - whose main purpose is to pack aliments - was also used. Its thickness is in the range[4] of $10\mu m$.

5.5.2 Solutes

- Tips-Pentacene → This is a soluble organic semiconductor and its characteristics have been previously explored in sec. 3.2.3.

- PMMA → This polar[5] polymer is commonly known as acrylic. It has insulating properties that grant it low current losses Tab. 3.1 (7) and a relative permittivity rounding 3 at 1Mhz. It is soluble in various organic solvents, including Toluene, Chloroform and Acetone.

5.5.3 Solvents

- Chloroform → This non-polar organic solvent has a melting point of -63,5ºC and a boiling point of 61,2ºC. It is one of the most dense organic semiconduc-

[4]This was determined measuring the mass of a sheet with 0,44 m X 0,29 m and evaluating $m[kg] = \rho[kg/m^3].V[m^3]$ for a the density of the aluminum (2800kg/m^3).

[5]Polymers can be polar or non-polar. Polar polymers possess dipoles that align with the electric field thus, displaying after the alignment, a certain dielectric constant. For low frequencies, the dipoles can accompany the electric field changes, but for higher frequencies they begin not to fully align, and the dielectric constant drops. Non-polar materials do not display this property pp. 7 [60].

tors with a density[6] of 1,48 kg/m^3.

- Toluene → With a melting point of -93ºC and a boiling point of 110,3ºC, this non-polar organic solvent has a density of 0,865 kg/m^3.
- 1,2 Dichlorobenzene → Displaying its melting and boiling point at -17ºC and 180,5ºC respectively, this non-polar organic solvent exhibits a density of 1,3 kg/m^3.

5.5.4 Solutions

- PEDOT:PSS → Is one of the most used organic conductors in organic electronics. Additional information can be found on sec. 3.2.1.3. In this work, the used product was Orgacon PEDOT:PSS IJ-1005, with a fabric date from 1/07/2010.

5.6 Mathematical Methods

5.6.1 A-Si:H TFT AIM-SPICE level 15 model and parameter extraction

To allow the simulation of electronic devices, a model capable of representing their behavior is needed. Here, the main elements of the procedure proposed by Cerdeira, A. and coworkers [61] to derive important parameters from the transfer and output curves of an OFET are described. The extracted parameters are intended to be used with the a-Si:H model in SPICE[7].

The parameters that the authors extract and find sufficient to describe the OFET model are listed in Tab. 5.1.

For the above-threshold region, the a-Si:H model is expressed in 5.2.

$$I_{DS} = \frac{\frac{K}{V_{AA}^{\gamma}}.(V_{GS}-V_T)^{1+\gamma}V_{DS}(1+\lambda.V_{DS})}{(1+R\frac{K}{V_{AA}^{\gamma}}(V_{GS}-V_T)^{1+\gamma}\left[1+\left[\frac{V_{DS}}{V_{DSsat}}\right]^m\right]^{1/m}} \tag{5.2}$$

Here, $K = (W/L).C_i.\mu_0$, and:

[6]The referenced densities occur at 25ºC
[7]Simulation Program with Integrated Circuit Emphasis

W Chanel width;

L Chanel length;

C_i Gate capacitance;

The remaining parameters are listed in Tab. 5.1.

Parameter	SPICE name	Symbol used	Units
Saturation modulation parameter	ALPHASAT	α_{sat}	–
Power law mobility parameter	GAMMA	γ	–
Output conductance parameter	LAMBDA	λ	1/V
Knee shape parameter	M	m	–
Conduction band mobility	MUDAND	μ_0	m^2/V.s
Source/Drain resistance	RS+RD	R	Ω
Characteristic voltage for field effect mobility	VAA	V_{AA}	V
Zero-bias threshold voltage	VTO	V_T	V

Table 5.1: Parameters that can be extracted using the method presented by Cerdeira and coworkers

Cerdeira noted that 5.2 ignores leakage currents, but it has the advantage of considering the increase in field effect mobility with the increase of the gate voltage.

The first parameters to be extracted are V_T and γ. In order to obtain them, Cerdeira and also Yaghmazadeh, O. [62] propose to use a function that - for the linear part of the transfer characteristic - relates the original values with their integration as expressed in 5.3.

$$H(V_{GS}) = \frac{1}{2+\gamma}(V_{GS} - V_T) = \frac{\int_0^{V_{GS}} I_{DS}(x)dx}{I_{DS}(V_{GS})} \tag{5.3}$$

Here, the authors point that V_T and γ can be extracted from the intercept and the slope, respectively.

Next, to determine VAA, it is required to first find the slope (Sl) of the expression $I_{DS}^{\frac{1}{1+\gamma}}$ vs. V_{GS}, and V_{AA} can be expressed as in 5.4 .

$$V_{AA} = \left[\frac{KV_{DS}}{Sl^{1+\gamma}}\right]^{1/\gamma} \tag{5.4}$$

To determine R, the the authors use 5.5 (re-arranged), where $\mathrm{IDS_{LIN}}$ represents the current in the linear region of the transfer characteristic, for the maximum available $\mathrm{V_{GS}}$ and small $\mathrm{V_{DS}}$.

$$R = \frac{\left[\frac{\frac{K}{V_{AA}^{\gamma}}(V_{GS}-V_T)^{1+\gamma}.V_{DS}}{IDS_{LIN}} - 1\right]}{\frac{K}{V_{AA}^{\gamma}}(V_{GS}-V_T)^{1+\gamma}.V_{DS}} \tag{5.5}$$

The parameter α_s is the next to be extracted, and to this end the output characteristic is used. Again a slope is necessary (Ss) and in this case it corresponds to the plot of $I_{Dssat}^{1/(2+\gamma)}$ vs. $(V_{GS}-V_T)$. The $\mathrm{I_{Dssat}}$ corresponds to the current, in each output curve, where $V_{GS}=V_{DS}$. The α_s is calculated as in 5.6.

$$\alpha_s = \frac{Ss^{2+\gamma}V_{AA}^{\gamma}}{K} \tag{5.6}$$

In order to determine the m parameter, the saturation voltage, defined here as $V_{DSsat} = \alpha_S(V_{GS}-V_T)$, is determined using one of the output curves. The m parameter is then calculated using 5.7.

$$m = \log 2 / \log\left[\frac{K\alpha_S(V_{GS}-V_T)^{2+\gamma}}{V_{AA}^{\gamma}I_{DSsat}(V_{DSsat)}}\right] \tag{5.7}$$

As the final parameter to be found, the channel length modulation parameter λ is determined evaluating the 5.2 in order to λ.

5.6.2 Bootstrap Inverter Calibration

The bootstrap inverter uses an additional OFET and a capacitor to extend the output voltage range. Its representation is shown in a) of Fig. 5.4.

The equations that can be used to set an appropriated working point for the device are derived by Jeon, J. et. al. [63] and the most relevant are shown in 5.8 and 5.9.

$$R_B = \frac{C_B + C_{gs\_TL}}{C_B + C_{gs\_TL} + C_{gd\_TL} + C_{gs\_TB}} \tag{5.8}$$

$$Vx, MIN = (V_{DD} - V_{TH}) + R_B(V_{DD} - V_{OH}) \tag{5.9}$$

The minimum voltage at the point "X" in a) of Fig. 5.4 is derived throughout the evaluation of 5.9, and is possible to set the voltage in the "X" node to smaller values than $V_{DD} - V_{TH}$[8]. Here, C_{gs_TL}, C_{gd_TL} and C_{gs_TB} are the load transistor (TL) gate-to-source parasitic capacitance, TL gate-to-drain parasitic capacitance and boost transistor (TB) gate-to-source parasitic capacitance respectively.

To optimize (close to zero) the maximum output value (V_{OH}) the ratio between the drive transistor (TD) and TL has to be properly adjusted ($V_{OH} = V_{DD}/R_W$). This ratio (R_W) is defined as in 5.10. The authors have simulated various parameter combinations and suggest the values 0.9 to R_B and 10 to R_W.

$$R_W = TD/TL = W_{TD}/W_{TL} = L_L/L_D \tag{5.10}$$

5.6.3 Zero-V_{GS}-Load Inverter Calibration

Although there are not many analytical models to aid in the design of this type of inverters - b) of Fig. 5.4 - Cui, Q. et. al. [64] present a possible approach to set design guidelines. Cui focused on developing a larger noise margin and thus grant a more stable device. The set from 5.11 to 5.14 can be used to define the V_{DD} and the relation between the geometrical dimensions of the load and drive transistors. Cui suggests 0.2 as the maximum limit for α, which demands a V_{DD} of, at least, five times V_{th}. To analyze the noise margin, as a normalized noise margin, 5.14 can be used with 0.586 as the upper limit.

$$N = TD/TL = (W_D/L_D)/(W_L/L_L) \tag{5.11}$$

[8]The "X" point has to be more negative than V_{DD} by, at least $|V_{th}|$ to allow the most negative part of the output signal to approach V_{DD}. It is possible for the voltage at the "X" point approach $2 \times VDD$

$$\alpha = \frac{Vth}{V_{DD}} \tag{5.12}$$

$$N_{opt} = [1/(2\alpha) + 1/2]^2 \tag{5.13}$$

$$NNM(N_{opt}) = \sqrt{2}(\sqrt{2} - 1 - \alpha) \tag{5.14}$$

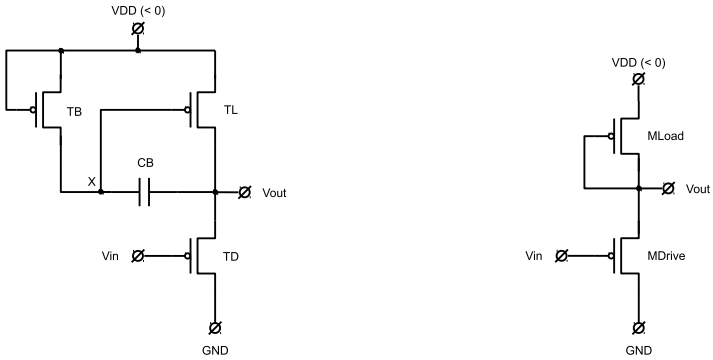


Figure 5.4: Schematic representation of a) bootstrap inverter; b) zero-V_{GS}-load inverter

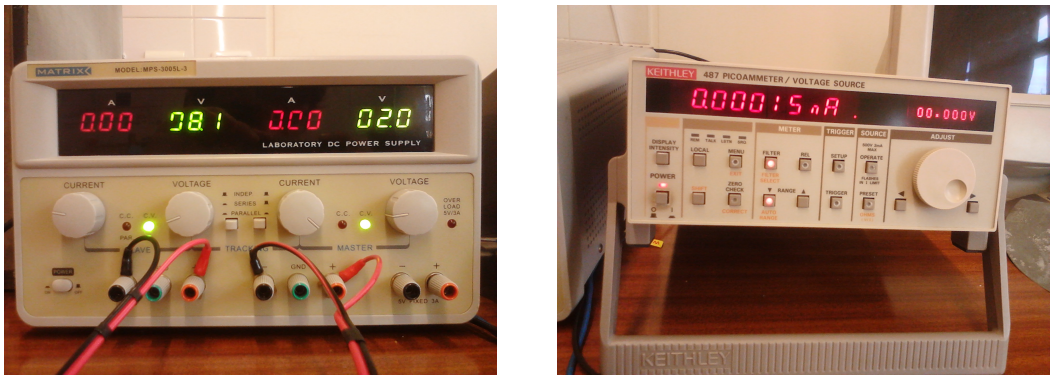
5.6.4 Model for the thickness of PMMA/Toluene and PMMA/Chloroform films

In these three works [65], [66] and [67], it is used the same model that can estimate the final thickness of PMMA in chloroform or toluene. In these works, it is recommended to keep the concentrations of PMMA not much higher than 5/95 wt.% to avoid deviations from the model, but these seem not be be significant (from the

analyzed material) until 10/90 wt.% - 15/85 wt.%. The models consider that the PMMA spreading is almost null after 30 seconds and does not consider longer time periods. The reference speed is 1000rpm. The system is presented in 5.15. Here, h is the height, C the concentration of PMMA in the solvent and W the rotations per minute.

$$\begin{cases} h = 0,92.C^{1,56}.W^{-0,51} & Toluene/PMMA \\ h = 4,3E^{1,33}.W^{-0,5} & Chloroform/PMMA \end{cases} \tag{5.15}$$

5.7 Used Sources and Meters



(a) **(b)**

Figure 5.5: Used source and meters: a) Matrix MPS - 3005L-3; b) Keithley 487 Picoammeter/Voltage Source

In this work, the different source/meters have been used. For each one, a small resume will be given.

5.7.1 Matrix MPS - 3005L-3

This is a common laboratory power supply source that can be used either as a voltage or current source. It has two adjustable outputs, ranging between 0 and 30 V each. These can be combined to attain a maximum of 60V (5A).

5.7.2 Keithley 487 Picoammeter/Voltage Source

Capable of being interfaced with a computer (either by rs-232 or using the IEEE-4888 interface), this voltage source and picoammeter is designed to provide 10fA sensitivity, up to 180 readings per second and ±500V (source). It can provide a minimum step of 1mV with and accuracy of 0.1mV.

5.7.3 Automatic Quadtech 1929 Precision LCR meter

This LRC can be used to extract from a capacitor the real (ε) part of the permittivity and the dielectric losses (tan δ), in the frequency range 100 Hz to 1 MHz at room temperature.

5.8 Used Software

5.8.1 Rhinoceros®

Rhinoceros® is a CAD system intended for multipurpose uses [68]. It can be used (but not limited to) in the microelectronics field in the conception of multilayer design of masks as an example.

5.8.2 Organic Transistor Model 0.2.9.7

As a third party simulation software [4], this online simulation tool has been developed for research purposes. It can approximately recreate what would be the transfer and output curves (among others) of the organic transistor.

5.8.3 Advanced Design System 2011®

This software from Agilent Technologies [69] has SPICE simulation capabilities and is specially intended for radio frequency (RF), microwave and high speed digital applications. In addition to a vast set of transistor models, it also allows to customize their parameters, given a series of parameters.

5.9 Capacitor

In the construction of the capacitor (a stack capacitor), two different substrates were used, a PET and an aluminum foil sec. 5.5.1.

Depending on the substrate, the sequence of layers that were deposited varied. In the case of PET, a first layer of gold was deposited using a sputtering process sec. 5.2 followed by a PMMA layer (sec. 5.3 or Fig. 5.3) and finally another gold layer. For the aluminum substrate, only two layers were used. PMMA was the first layer to be directly deposited using either the spin coating process or the paint-gun, and the last gold layer was deposited using the sputtering system. A last capacitor topology has been implemented using the PET foil as the inter-layer, with and without adjacent additional PMMA layers, and sandwiched between two gold layers sputter-deposited. All the capacitors were constructed using a mask with an aperture of 2cm*1,4cm, and a consequent area of $280\mu m$.

The processes, materials and parameter variations are represented in Tab. 5.2.

The various weight percentage (wt.%) of the PMMA solute in chloroform solvent were calculated using the relations in 5.16.

$$\begin{aligned} wt.\% &= 100 \times \frac{M_{Solute}}{M_{Solvent}+M_{Solute}} \\ M_{Solute} &= \rho \times V \end{aligned} \tag{5.16}$$

Here, ρ is the density [kg/m^3], V the volume [m^3], $M_{solvent}$ [kg], M_{solute}[kg] are the solvent and solute mass, respectively. The chloroform properties are highlighted in sec. 5.5.3.

After the PMMA has been deposited, it was cured at 100^{o}C for 10min.

The characterization process was carried out using an Automatic Quadtech 1929 Precision LCR meter sec. 5.7.3.

5.10 Schottky

The schottky components were prepared using a metal-semiconductor rectifying junction and a metal terminal that provided an ohmic contact . For the first component 5.6a, the chosen organic material used was - PEDOT:PSS sec. 5.5.4 - and for the rectifying and ohmic contacts aluminum and gold were respectively selected. This schottky component was constructed in a stacked topology. The used substrate

		Dielectric Deposition Method		
		Spin coating	**Paint-gun**	**None**
PMMA Percentage	**0 wt.%**			(1x) Au/PET/Au
	2/98 wt.%		(1x) Au/PMMA/Au (1x) Al/PMMA/Al	
	5/95 wt.%	(1x) Al/PMMA/A	(2x) Au/PMMA/Au (2x) Al/PMMA/Al	
	8/92 wt.%	(1x) Au/PET/PMMA/Au (1x) Au/PET/2xPMMA/Au		
	10/90 wt.%	(3x) Au/PMMA/Au (2x) Al/PMMA/Al		

Table 5.2: Processes, materials and parameter variations for the stack capacitor

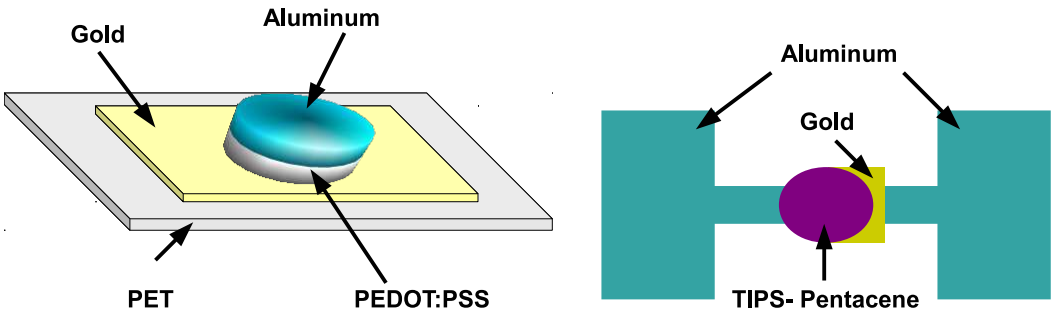


Figure 5.6: Used topologies for the schottky diode implementation - Stack and Planar - are shown in 5.6a and 5.6b respectively.

was PET with a sputtered gold layer - on top of which - two drop-cast layers of PEDOT:PSS followed. The first layer of PEDOT:PSS was allowed to dry at ambient temperature. After, another layer was applied and - while it was still at the liquid state - an aluminum circle with a diameter of 5mm was placed atop of this layer, thus granting a contact area rounding $19,6\mu m^2$.

To the second component 5.6b, consisted of a planar structure with two parallel (not atop of one another) deposited layers. The first layer was of aluminum and the second of gold. In between these two contacts, a drop-cast layer of Tips-Pentacene was deposited.

These devices were characterized using a Keithley 487 Picoammeter/Voltage Source sec. 5.7.2 alone, which interfaced with a third-party Labview^{TM}software.

5.11 OFET

In this section, the processes used to prepare the materials, deposition, curing, characterization, simulations, parameter extraction, model building and logic circuit implementation are presented from the point of view of the used materials and methods. The associated and relevant results will be discussed in sec. 6.3.

5.11.1 Device implementation

Two different transistor philosophies have been tested, and one of them was not fully implemented, namely the interdigitated OFET, a) from Fig. 5.7. This figure also shows the implemented masks. The left one a) was made out of aluminum and b) has been hand made in PET. Both have been designed with Rhinoceros®. The mask size has been kept relatively small, with 5cm×3,5cm as stated in sec. 5.1. For the interdigitated FET, three masks were created whereas two of them were intended to pattern each arm of the interdigitated structure and the remaining one the gate. For the parallel arms OFET, only two masks were made. One for the gate, and the other for source and drain electrodes. These masks were intended to be used with a sputtering system (sec. 5.2).

The implemented OFET topology is known as "bottom gate, bottom contact". A schematic representation of the most common possibilities can be seen in Tab. 5.3.

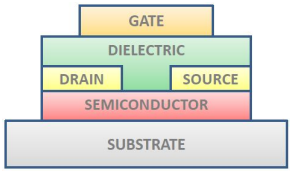
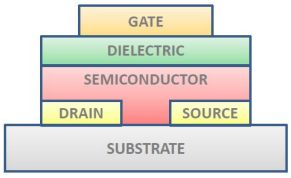
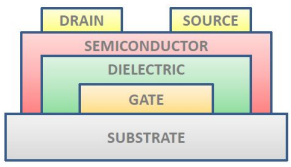
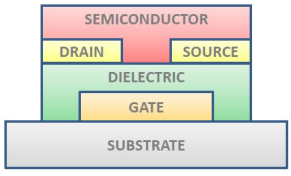
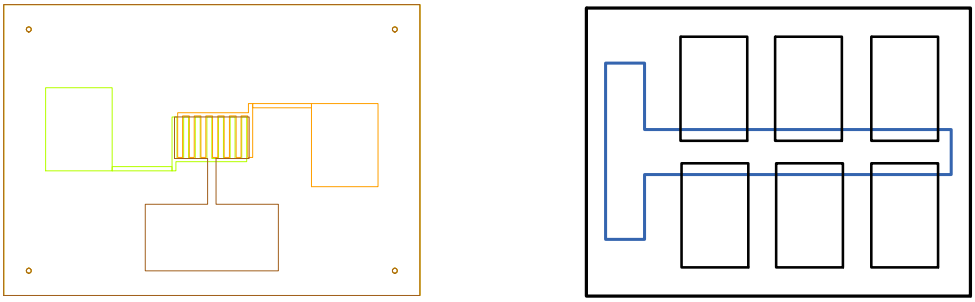
	Top-Contact	Bottom-Contact
Top-Gate		
Bottom-Gate		

Table 5.3: Most common OFET topologies

In the "bottom gate, bottom contact" topology, the first layer to be patterned in the sputtering system is the gate. Above this first layer, a dielectric layer is pre-

pared with PMMA/Toluene and deposited by spin-coating (sec. 5.3) and afterwards the sample is cured in an oven. The next layer to be deposited is the one which defines the source and drain electrodes, again using the sputtering system. Finally, the semiconductor in solution is deposited by spin-coating and cured in the oven. The prepared semiconductor solution consisted of a dissolution of Tips-Pentacene/1,2 Dichlorobenzene with a weight percentage (wt.%) of 13,3 (see 5.16, sec. 5.9). The previously prepared PMMA/Toluene solution was 8% wt.



(a) **(b)**

Figure 5.7: a) Interdigitated OFET; b) Parallel arms OFET

5.11.2 OFET Characterization

After the device has been constructed, it was placed inside a protective box. Its terminals were connected to the terminals in the box to an overall robustness. In the OFET - as both contacts with pentacene are made of gold - the source and drain could be used interchangeably. To prevent confusion, one terminal was chosen to be the drain and the other the source. The characterization scheme of the device is presented in Fig. 5.8.

Using both the Matrix source and the Keithley (source/meter) - which was controlled by a third-party Labview^{TM} software - the transfer and output curves were acquired for the multilayer OFET (b) from Fig. 5.7).

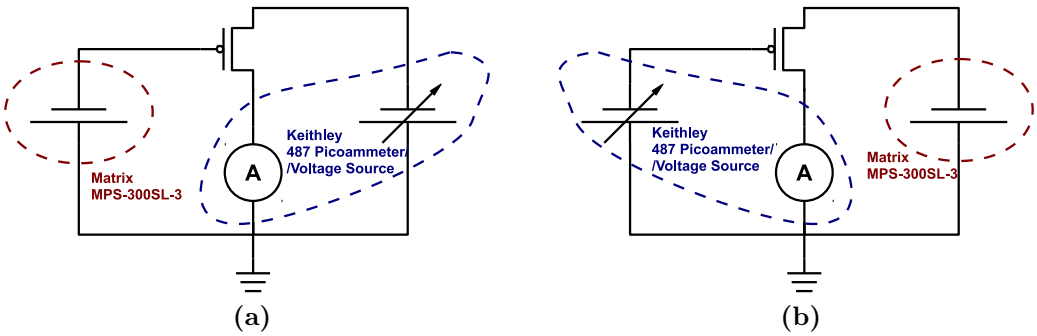


Figure 5.8: OFET Characterization Scheme - a) Output Curve; b) Transfer Curve

5.11.3 Physical Simulation of the OFET Behavior

Some particular characteristics and limitations of the deposition processes led to an OFET device that lacked some important features, among them:

- Low gate current (Ig) leakage;
- Uniform insulating and semiconductor layers;
- High organic semiconductor crystallinity;
- Highly oriented organic semiconductor crystals;
- Closely packed source and drain electrodes;
- Small variations of the distance along the transistor channel;

Although the created device was fabricated and characterized, it was decided to find which would be its approximated characteristic curves – had it been perfectly assembled. As the final intention was to observe how the device would perform in digital electronics, and the analyzed device displayed significant leakages and parasitic, it was used a simulation software that recreated the device behavior based on its materials, topologies and geometries. The intention was to use the characteristic curves of this simulated device - which is based on the originally created - and extract its parameters to model it. The simulated curves would have been very similar to those of the physically implemented device if a greater control over the assembly steps and the morphology of the layers have been possible.

A set of parameters is necessary to define the OFET device to be simulated according to [4]. Fig. 5.9 presents the main parameters to be found. For those

parameters whose value is not available or clear how to determine, the field has been kept with the default suggested value.

	Parameters	**Information**
	Topology	Bottom/Top gate? Bottom/top contacts?
Geometry	W	Width (Source/Drain extension)
	L	Length (Source/Drain separation)
	W_m	Gate Workfunction
OSC Constants	d_s	OSC thickness
	OSC_{type}	Doped? Intrinsic?
	μ	
	Density of states (DOS)	Gaussian DOS- amorphous, or 3D DOS - crystalline material.
	ε_s	Relative dielectric constant
	x_s	Electron Affinity
	E_{Gi}	Bandgap
Insulator	d_i	Insulator thickness
	ε_i	Relative dielectric constant
	x_i	Electron Affinity
	E_{GS}	Bandgap
	Interface Layer Traps	Adds interface trap information
Transport	Diffusion	Diffusion current can be allowed
	Mobile Charge Types	P-type (holes) or N-type (electrons)
	Mobility Model	Simplified Model; Crystalline Material; Hopping Transport;
Source/ /Drain Contacts	Rs	Source contact resistance
	RD	Drain contact resistance
	ϕ_B	Barrier height at source/OSC interface
Temperature	T	in Kelvin (K)

Figure 5.9: Main required parameters from [4] to simulate an OFET device

5.11.4 OFET Model - Parameter extraction

To allow the simulation of a single OFET as well as multiple interconnected OFETs - creating simple digital logic circuits - a SPICE compatible program (ADS) was used. For simulation, various transistor models can be used - they are grouped in levels, e.g. Level 0, Level1, etc. where a higher level can potentially provide better results in expense of more needed parameters and increased simulation time. These models require both geometrical, electrical and model specific parameters. Geometrical parameters can be obtained directly, contrary to electrical and model

specific parameters, which demand additional effort. An a-Si model, namely "Shur-RPI Amorphous (ASIA2) TFT" was used. This is a Level 15 model. The extracted procedure from Cerdeira, A. et. al. [61] was used to obtain the needed parameters for simulation as depicted in sec. 5.6.1.

5.11.5 Forward in Advanced Design System

After the needed parameters have been determined, two instances of the a-Si model were created. For each one of them, the parameters have been set equal with the exception of those defining their dimensions (W and L). This software allows for a modular approach in which modules can be created using previously constructed models (or defined components). Apart from the OFET, in this software the following simple systems have been created:

- An inverter (cascade);
- A bootstrap inverter (cascade);
- A nand gate;

To encounter an approximate working point in which both inverters present best performances, two different algorithms were used sec. 5.6.2, sec. 5.6.3.

Finally, the nand gate was built appending an additional drive OFET in parallel to the previously existent one.

6 Results and Discussion

6.1 Capacitor

Before the results and discussions on the created capacitors, a short contextualization will be given.

The Quadtech 1929 (sec. 5.7.3) can provide the real (ε) part, which is associated with the real value of the capacitor dielectric and the dielectric losses (tan δ). Considering the simplified diagram of the equivalent capacitor, alongside with a graphical representation of the same, these relations can be better understood (Fig. 6.1). Assuming a non-ideal capacitor, more phenomena could happen. The PMMA is a dipolar dielectric and, in principle, it can experience variations to its "ε", which usually rounds 3. From now on, ε will be denoted as ε_{diel}. As the parallel plate capacitor can be calculated evaluating the relation $c = (\varepsilon_{diel} \times \varepsilon_0 \times A)/d$, where ε_0 and A are the permittivity in the vacuum and the area of one of the plates, respectively. It is perceptible that, if a dielectric can have its ε_{diel} changed with the subjected frequency, its capacitance will also change. Here, different situations are possible. It can be observed that the parasitic resistance is constant and, as the capacitor changes its value, the relative importance of this parasitic also changes or, on the other hand, it can be perceived that with an increased frequency, not only the capacitor varies but also the resistance. This may imply that other parasitic besides the resistance start to play a role. This last point of view would demand equivalent circuits that are more complex. This topic will be (briefly) referred later.

Fifteen capacitors have been made and, as an attempt to show some tendencies, they will be divided into graphical groups. Before the graphical presentation, a brief reference to their specificity is made in Tab. 6.1.

In Fig. 6.2, it is possible to see that, except for c1 ads c5 that have a capacitance between $1pF$ and $10pF$ (or $3,6nF/m^2$ to $36nF/m^2$), the remaining agglomerate with capacitance values between $70pF$ and $2nF$ (or $250nF/m^2$ to $7,1\mu F/m^2$) in the interval [20Hz to 1Mhz].

(a) (b)

Figure 6.1: The basic capacitor equivalent circuit 6.1a, and the correspondent diagram 6.1b

Name	Concentration [wt.%]	Stack type	R.p.m.
c1	2/98	Au/PMMA/Au	—
c2	2/98	Au/PMMA/Al	—
c3	5/95	Au/PMMA/Al	—
c4	5/95	Au/PMMA/Au	—
c5	5/95	Au/PMMA/Au	—
c6	5/95	Au/PMMA/Al	—
c7	5/95	Au/PMMA/Al	1000 (30 s)
c8	10/90	Au/PMMA/Au	
c9	10/90	Au/PMMA/Al	
c10	10/90	Au/PMMA/Al	
c11	10/90	Au/PMMA/Au	500 (5s) + 1000 (30 s)
c12	10/90	Au/PMMA/Au	
c13	—	Au/PET/AU	—
c14	8/92	Au/PET/PMMA/Au	1000 (30 s)
c15	8/92	Au/PET/PMMA/Au	

Table 6.1: List of the created capacitors

With the intention to visualize the spam of variations regarding the losses of the capacitors, Fig. 6.3 presents the variation that $\tan\delta$ displays for each capacitor (1 to 12) when subjected to test frequencies from 20 hz to 1 Mhz. C8 is the capacitor that displays the most severe losses ($\delta = 0,74$) for low frequencies.

One interesting set of results, is related to those capacitors displaying the lower losses and the most constant behavior Fig. 6.4. Interestingly here, only c4 has both layers made of gold, all the remaining have one aluminum layer, which is the substrate. This behavior can be happening due to many factors. It can be related to the fact that the aluminum was not deposited but rather used as a foil (common kitchen aluminum foil); the PMMA can have some major affinity with aluminum

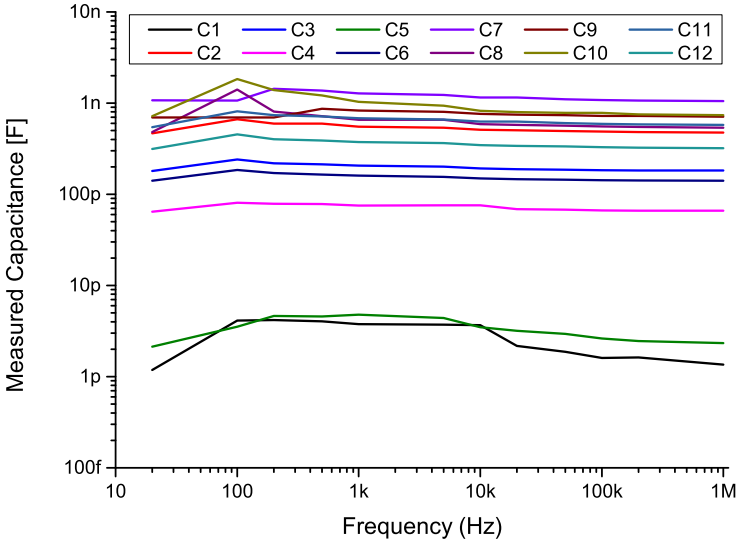


Figure 6.2: Capacitance of devices 1 to 12

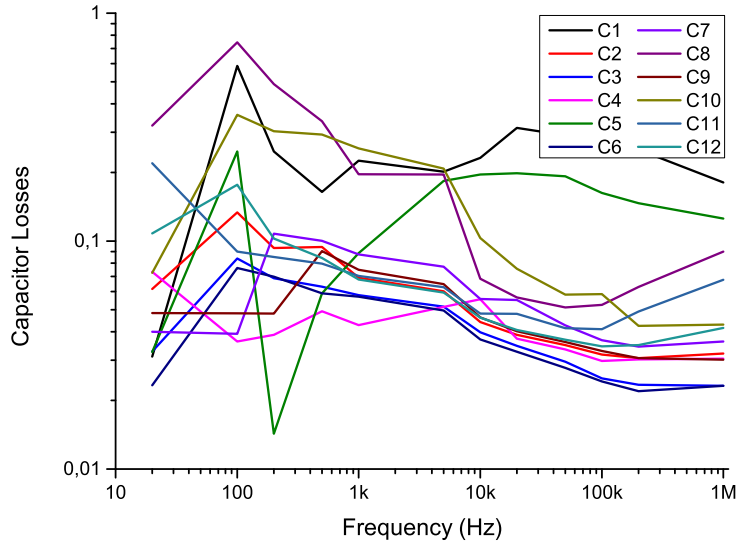


Figure 6.3: Losses in the capacitors 1 to 12 - $\tan\delta$

than with gold; the PMMA/Chloroform may be leading to better wetting in case of the aluminum; the aluminum surface may be contributing to a more homogeneous distribution of the heat in the curing process, among other possible factors. An important conclusion to append here, is that further research - either theoretical

and/or practical - should be made regarding this behavior.

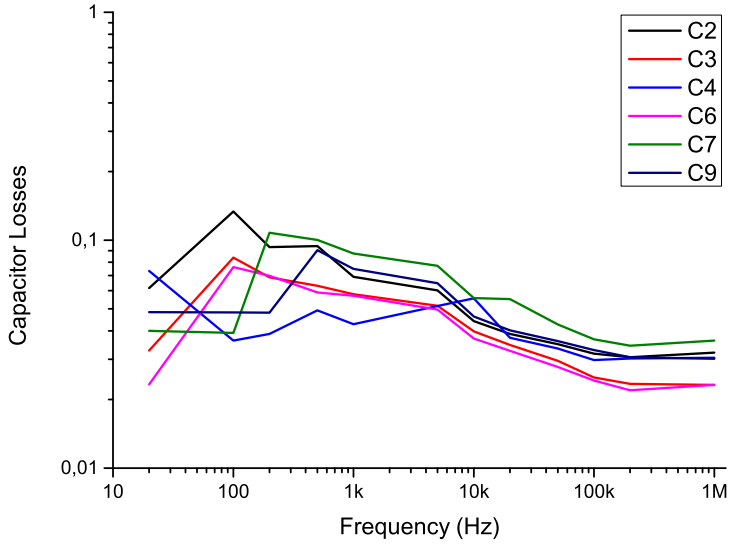


Figure 6.4: Set of capacitors displaying lower losses than the average

As can be observed, c5 and c1 are among the capacitors that show greater variation in their losses for increasing frequencies. They however, do not follow a tendency, they have losses that present rapid variations. This seems to suggest that the above mentioned capacitor model may not be the most indicated and that further studies in this area are necessary. More complex models may be a possible solution - these may consider additional parallel branches as well as series resistances to the capacitor. Parallel branches (e.g. inductance in series with a resistances), that for a given frequency star or stop to contribute to the overall losses may be a possible strategy.

Finally, is possible to observe in Fig. 6.5 that the capacitance from PET alone visibly decreases with frequency at 2khz. The addition of PMMA films can counter this effect and oddly even boost it for higher frequencies as noticeable in “PET + 2PMMA”.

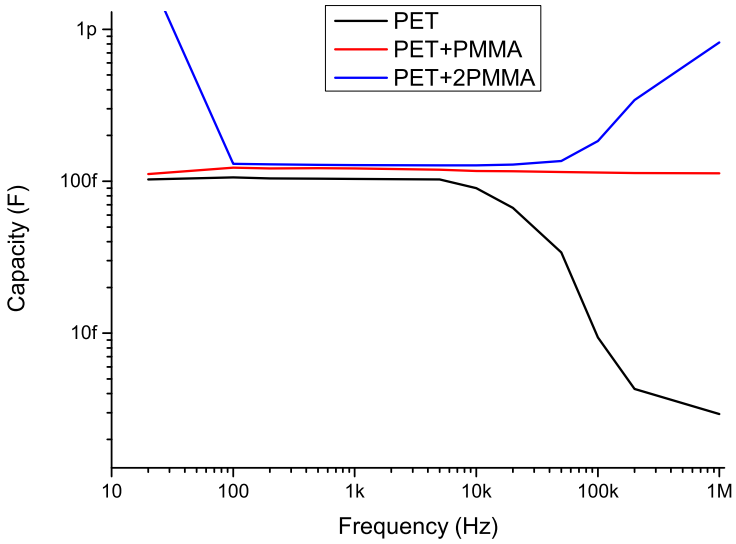


Figure 6.5: PET and additions of PMMA films

6.2 Schottky

In this section, a brief contextualization to the main propellers to the implementation of the schottky device will be underlined, some studies that show some relevant results will be indicated and, when possible and justifiable, compared to this present work. Finally, the results will be given and discussed as well as some possible interpretation.

As previously referred in sec. 5.10, two topologies have been implemented in the construction of the schottky device, namely the stack 5.6a, and the planar 5.6b. As argued by Dzugan, T. et. al. in [70], it may be expected to observe the formation of a schottky contact with some metals and PEDOT. They found, however - and contrarily to their theoretical assessment - that PEDOT/titanium did not displayed a schottky junction behavior. Another three studies from Kang, K. S. and coworkers, on three different journals ([71], [72] and [73]), report on various findings what seems to be a similar experiment. In all the three presented works, PEDOT:PSS is doped with pentacene, which according to the authors can lead to a forward current 440 times that of the undoped PEDOT:PSS. These unexpected findings reinforce the idea that organic conductors and semiconductors still need of deeper research.

Three of the characteristic curves extracted from the created schottky diodes with Au/PEDOT:PSS/Al stack (5.6a) are shown in Fig. 6.6. It is perceptible that

no evident rectification seems to be occurring for the tested voltage interval. Additionally, for negative and positive voltages, the magnitude of the current is roughly the same for all three devices, with a small exception of 6.6a. It is interesting to note that, the hysteresis test performed in 6.6b and 6.6c shows abrupt variations as the first voltage steps exhibit no current. This may have been due to an equipment error, contact problem, or other phenomena related to the physical behavior of the charges.

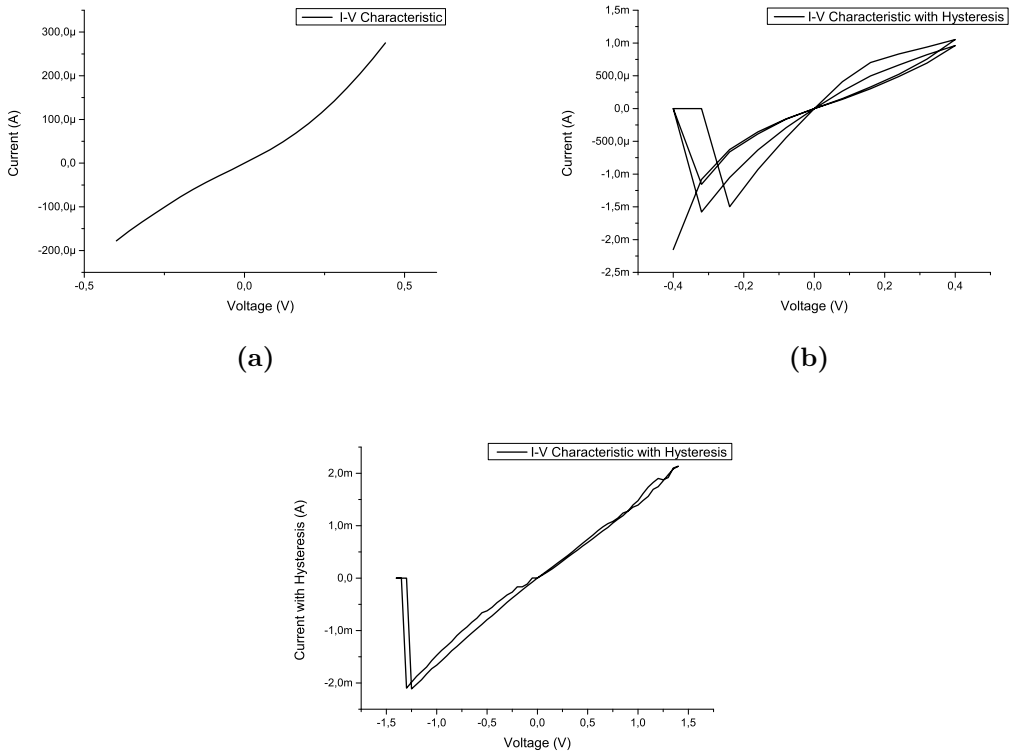


Figure 6.6: I-V Characteristic of three different PEDOT:PSS stack-devices of Au/PEDOT:PSS/AL. 6.6b and 6.6c show the characterization including the hysteresis effect. 6.6a, for clarity, only displays the characteristic curve

As previously mentioned, a single device with a planar structure and with contacts of gold and aluminum has also been created (5.6b). Its I-V characteristic is presented in Fig. 6.7 with four voltage sweeps, creating the observable hysteresis effect. The second forward voltage sweep gave origin to a maximum current of 3,6E-6A while the first had given origin to a current of 1,25E-5A - that is 3,4 times more. When a reverse voltage is applied, a negative hump (1º left) appears. This may

be due to parasitic accumulated charges that are then released, as for both reverse humps, the relation between their minimum currents (-2,67E-6A and -8,02E-7A) is of 3,33, which is very close to the previous relation. Dzugan [70] attributes the hysteresis effect observed in PEDOT devices to the degradation of the material and to ion migration, and for devices using PEDOT:PSS that fail after long periods of time, Kang [71] attributes the failure to the acid properties of PSS on metal contacts. In this present work, as the device uses TIPS-Pentacene as the semiconductor, only the "ion migration" possibility may be a valid candidate explanation.

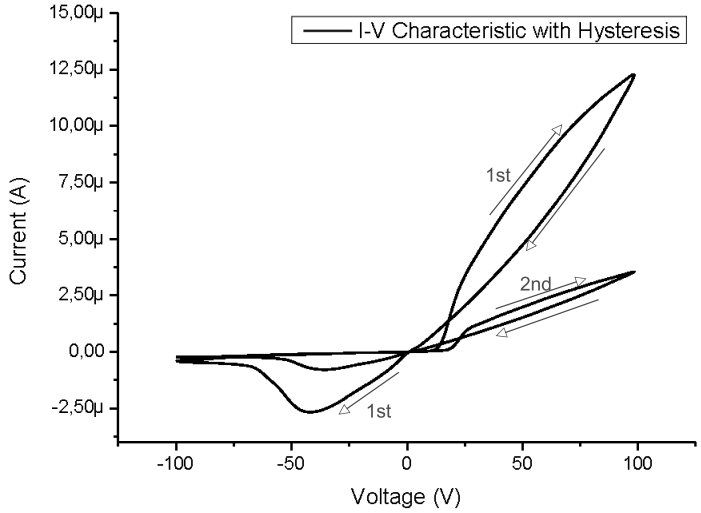
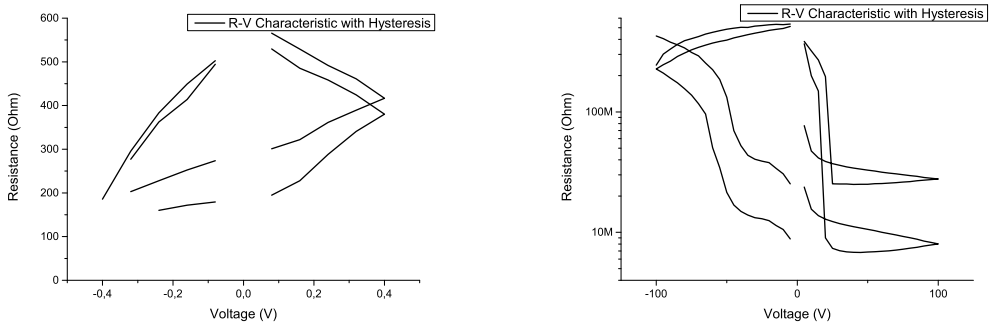


Figure 6.7: I-V and R-V characteristic curves of a planar Au/TIPS-Pentacene/Al schottky diode

Another interesting data set, relates to the calculated equivalent resistance of these devices. In 6.8a, it can be seen that the resistance in the device has a stable value rounding 200Ω except for values close to zero volt. The magnitude of the voltage value that is closer to zero - from the acquired data - rounds 10^{-17}V. This value is much lower than the smallest value above or below zero that the keithley (sec. 5.7.2) can generate. Accounting to this fact, this may be attributed to several causes, as parasitics, "ion migration", some imprecision linked to the keithley system, among others. As the interval between samples was less than half a second, the two first possibilities might be of consideration. For 6.8b, the hysteresis observed and the variations to it round the interval of 6,73E5Ω to 7,31E7Ω (with a variation of 7,24E7Ω) for a voltage excursion of 100V.



(a) **(b)**

Figure 6.8: R-V characteristic from two devices. 6.8a corresponds to the device appearing in 6.6b, and 6.8b to the device in Fig. 6.7

6.3 OFET

As previously pointed, one of the implementation philosophies for the OFET (5.7a) has failed to be achieved. This fact does not mean it cannot be done, rather, a more careful planning might be needed. Upon analyzing this device it was perceptible that, the deposited gold was occupying larger areas than those of the mask apertures. The excess gold was blurred. Apart from the registration between masks that should have been carefully planned - thus avoiding overlaps - the heating of the polymeric substrate during deposition, along with other factors, may have created spaces, or air gaps between the mask and the substrate. Fig. 6.9 is an empirical model illustrating how such an effect can be negative to the final deposited specimen. Here, "h1" is the separation between a mask entrance/aperture and the substrate, "h2" the separation between the target (gold) and the mask, "d1" is the desired area to be patterned and "d2" the real patterned area. The scenario was conceived only considering the outermost sputtered gold so that the worst effects could be clearly perceptible. Assuming for the analysis that all the surfaces are parallel, it can be seen that triangles $\Delta[dfe]$ and $\Delta[igh]$ are rectangular and proportional, as the segment $[dg]$ intercepts parallel lines. This also implies that $d\hat{f}e = i\hat{g}h = \alpha$. The relation $h_2/\overline{bd} = h1/\overline{gh}$ can thus be used to write $\overline{gh} = (\overline{bd}.h_1)/h_2$. As the additional left segment length $\overline{gh}$ was determined by this procedure, so the right segment can be. The final deposition area would be the sum of the left segment, d_1, and the right segment. As can be perceived from the left segment formula, to reduce the blurred area, there are three immediate hypothesis: augment h_2, reduce

the segment length $\overline{bc}$ (or equivalently the length of the gold target) or reduce h_1.

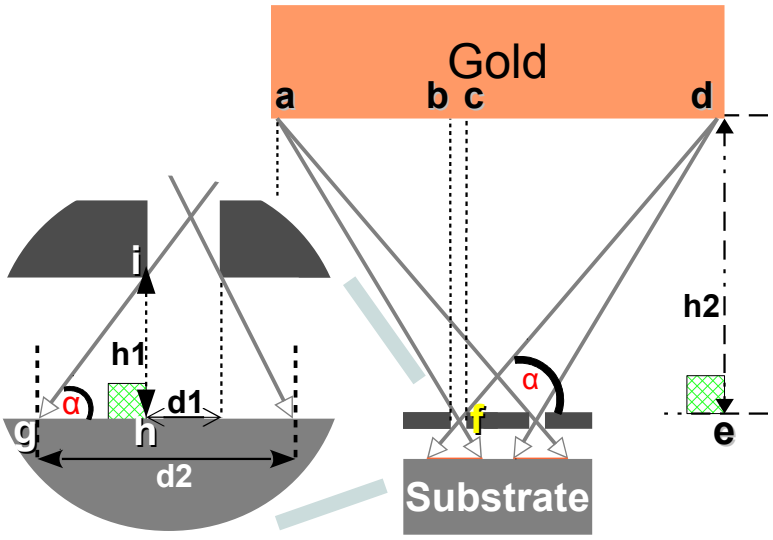
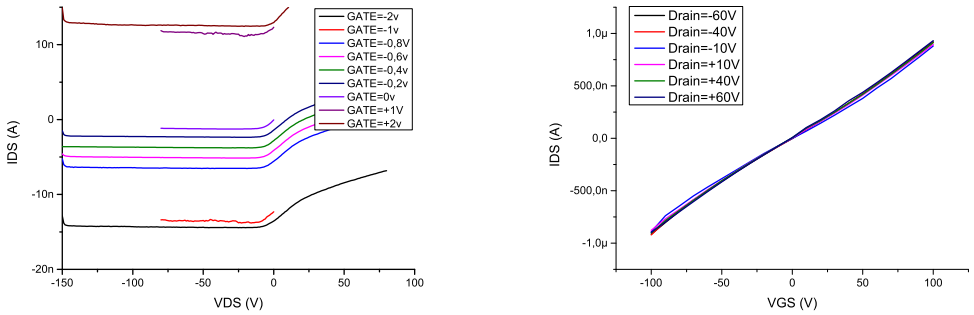


Figure 6.9: Sputtering problems - Substrate/mask separation

The other OFET implementation philosophy, whose layers can be seen in 5.7a was constructed using a "bottom gate top contact" topology, as depicted in Tab. 5.3. This OFET exhibited a current modulation of the channel dependent on the gate voltage, although, due to significant current leakage of the gate when compared to the current that flew between the source and the drain of the device, a careful analysis was not possible. The obtained output and transfer characteristic curves are shown in Fig. 6.10. As can be seen, the output characteristic does not present any significant variation for each of the different VDS inputs. Additionally, the output curves display positive and negative offset, depending on the gate voltage. For cases in which a positive VGS is applied, the correspondent output curve is shifted upwards and the opposite happens for negative values. This may be due to various causes, but one of the most probable relates with defects in the semiconductor/dielectric interface. As the conduction layer forms with extreme proximity to this interface, even small defects can became highly important in the charge carrier process. Even if small height changes along the channel dielectric became frequent, as an example, considerable implications to the charge carriers can happen. As a charge experiences a force that confines it to a region closer to the dielectric, its interactions with neighbor charges will be easier if done at the same height. A charge will thus experience difficulties in a “valley like terrain” in which the lower the charge is,

the stronger is the pulling force. This can inclusively lead to charge trapping and, assuming the terrain analogy, the charge may become enclosed in the bottom of a valley. If many "valleys" exist, many charges will start to become trapped and, to allocate new charge carriers, an increased threshold voltage will be needed to attract charges that are further away from the interface. As these "valleys" affect the threshold voltage, is the author's believe, that they can further degrade the output and transfer characteristics. As the gate depends on the PMMA to block the charges from the gate to the channel, the thicker the PMMA, the less probable a charge will pass through. These "valleys" may present thinner zones than the average channel thickness, thus leading to an overall degradation in the capacity to block current.



(a) **(b)**

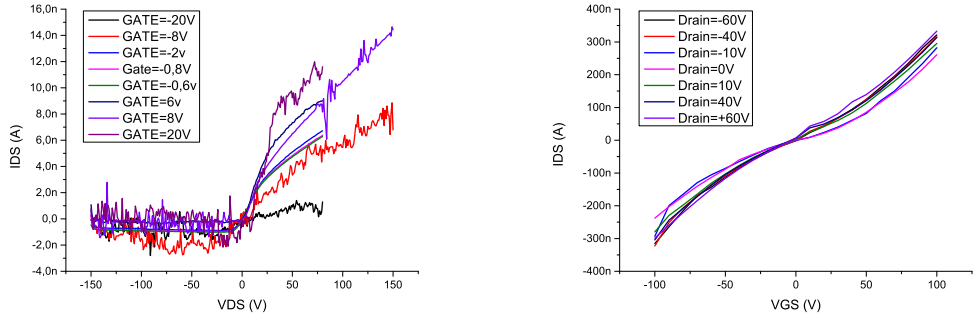
Figure 6.10: The I-V OFET characteristics: In 6.10a, the output curves for low VGS; In 6.10b, the transfer curves for a wide VDS input

It was attempted to compensate the offset, finding the average gate resistance, and for each VGS compensate the current. The results are shown in Fig. 6.11. Still, the results did not display the most convenient characteristics for the parameter extraction procedure.

To overcome this situation, as already has been described in sec. 5.11.3, the device was simulated using a third party software. Further details are given in the following subsection.

6.3.1 Simulation with Organic Transistor Model 0.2.9.7

Using this online tool, the parallel arms transistor implementation philosophy was simulated. Fig. 6.12 exhibits the used parameters.



(a) **(b)**

Figure 6.11: Offset compensation - output 6.11a and 6.11b curves with offset compensation

The only parameters that have been iterated were the organic semiconductor thickness and mobility. These were tuned until an approximate current compromise, for both original transfer and output curves were found. The resulting transfer and output curves are shown in Fig. 6.13.

6.3.2 Parameter extraction

Using the OFET parameter extraction method sec. 5.6.1 with the curves generated from the physical simulation of the device Fig. 6.13 a series of parameters were obtained. In Tab. 6.2 these parameters as well as additional geometric and physical parameters - which are needed by the simulation program - are equally presented.

6.3.3 Device and logic Simulations

Using the ADS, the drain and gate of the OFET were connected with independent variable voltage sources. The OFET source terminal was grounded. These two voltage sources were made to vary in such a way that, for each step of one, the other executed several other steps, thus contemplating the excursion needed for the output and transfer curves.

For the OFET with the presented characteristics in Tab. 6.2, the simulations result are presented in Fig. 6.14.

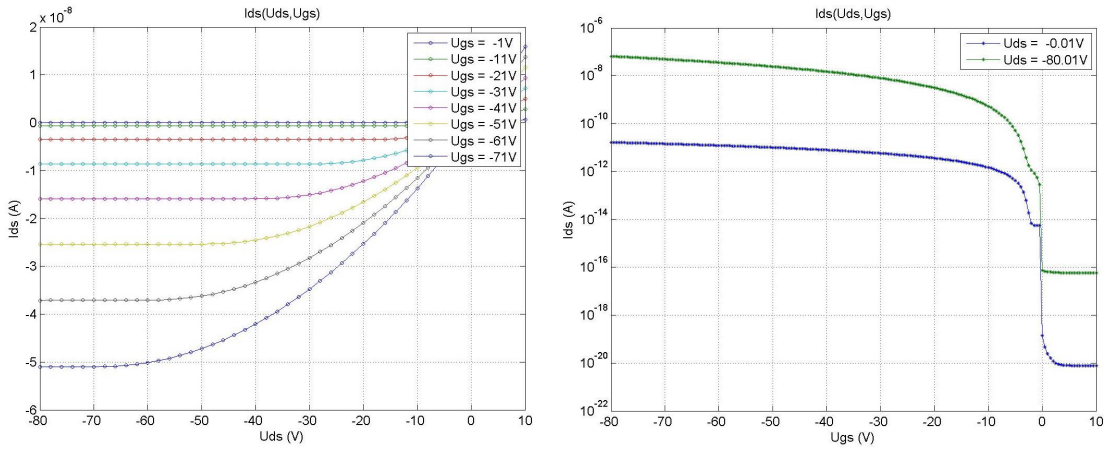
For the inverter, two implementations were made. The first one used a simple zero-vgs load inverter topology, and for the suggested algorithm of calibration in sec. 5.6.3, V_{DD} was chosen to -20V, and consequently α 0.15. The variable that has

	Parameters	Value	Ref.
Geometry Interdigitated	Topology	Bottom Gate, Bottom Contact	Not simulated
	W	70,9 mm	
	L	0,1 mm	
Geometry parallel arms	Topology	Bottom Gate, Bottom Contact	–
	W	11,5 mm	–
	L	3,5 mm	–
	W_m	5,1 eV	–
OSC Constants	d_s	$0,4\mu$m	Iteration
	OSC_{type}	Intrinsic	–
	μ	0,005 cm^2/V.s	Iteration
	DOS	Gaussian DOS - amorphous	–
	ε_s	4	[74]
	x_s	2,9 eV	[74]
	E_{Gi}	1,8 eV	[74]
Insulator	d_i	2×10^{-6}m	sec. 5.6.4
	ε_i	3	–
	x_i	1,9 eV	Default
	E_{GS}	5,0 eV	[75]
	Interface Layer Traps	No	Default
Transport	Diffusion	Yes	Default
	Mobile Charge Types	P-type (holes)	–
	Mobility	Simplified Model	Default
	Model	Hopping Transport	Default
Source/ /Drain Contacts	Rs	0Ω	Default
	RD	0Ω	Default
	ϕ_B	0 eV	Default
Temperature	T	300 K	Default

Figure 6.12: Used parameters from [4] to simulate an OFET device

been chosen to be shifted was L_D. L_L was kept at 3500 μm and L_D reduced to 233 μm. In order to improve the performance of this inverter, five stages were connected in series, thus leading to a sharper switch between states as can be seen in Fig. 6.15.

It is possible to observe that, although the upper limits of the output get very close to zero, the inferior outputs does not. To highlight the fact that this is not related to the magnitude of V_{DD}, the simulation was repeated for -40V, and the results are shown in Fig. 6.16. It can be seen though, that the lower part (or "logic zero") of the output continues to be spaced from -40 V, although in fact the output



(a) **(b)**

Figure 6.13: Output (6.13a) and Transfer (6.13b) characteristics of the physically simulated device

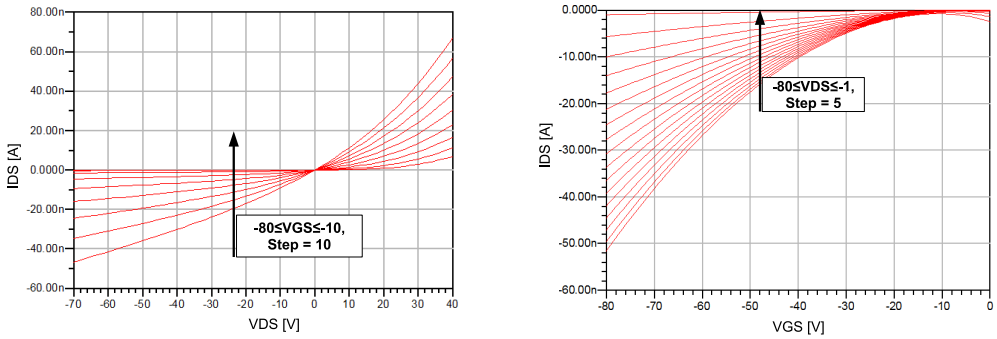
Parameter	Spice name	Symbol used	Value
Gate lenght	L	L	$3500\mu m$
Gate withth	W	W	$11500\mu m$
Saturation modulation parameter	ALPHASAT	α_{sat}	0,608
Rel. dielectric gate constant	EPSI	EPSI	3
Power law mobility parameter	GAMMA	γ	0,49
Output conductance parameter	LAMBDA	λ	0,0087 V^{-1}
Knee shape parameter	M	m	1,09
Conduction band mobility	MUDAND	μ_0	5E-7 $m^2/V.s$
Dielectric thickness	TOX	TOX	2E-6 m
Characteristic voltage for field effect mobility	VAA	V_{AA}	226,255 V
Zero-bias threshold voltage	VTO	V_T	2,98 V

Table 6.2: Parameters used for SPICE simulation of the OFET

is now sharper.

Theoretically, this inverter was supposed to be faster, but this was not the case. The frequency of the input wave - as will be possible to compare - was higher for the bootstrap inverter without causing distortions or gain losses.

The algorithm for the sizing of the parameters in the bootstrap inverter can be found in sec. 5.6.2. This algorithm considers the parasitic capacitance of both "Load" and "Drive" OFETs. The most important contribution for these capacitance is the overlap of the gate over the drain and the source contacts. It was assumed



(a) (b)

Figure 6.14: Results from the OFET simulation in the ADS software - 6.14a represents the output and 6.14b the transfer characteristic

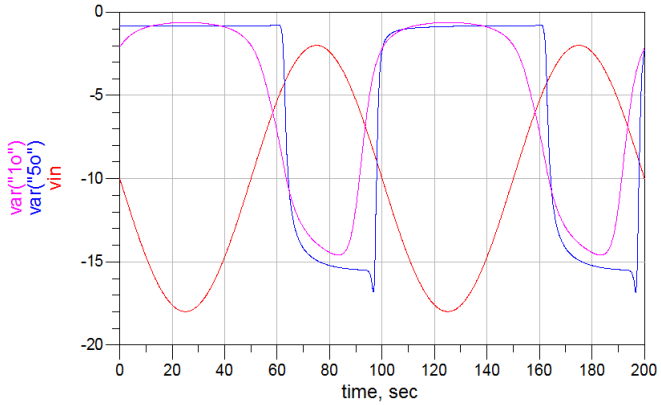


Figure 6.15: Zero-VGS load inverter with VDD=-20V - input, first stage and fifth (last) output

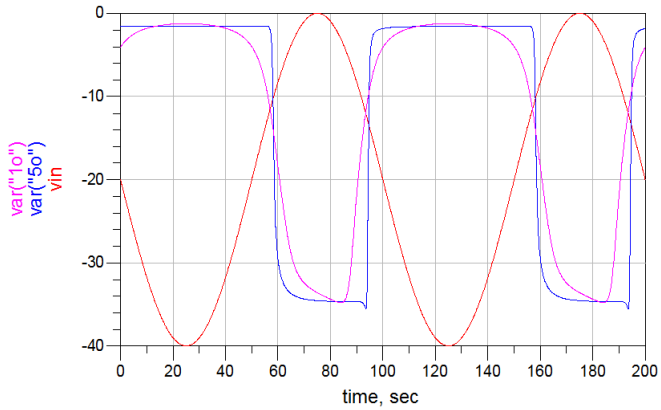


Figure 6.16: Zero-VGS load inverter with VDD=-40V - input, first stage and fifth (last) output

that an overlap of 0,1mm could be achieved. Considering W to be 11,5mm, the area equals $1,15E-6m^2$. As the dielectric relative permittivity is 3, the vacuum permittivity is $8,854E-12$ and the dielectric thickness $2E-6m$, the parasitic capacitance (from the gate to the drain or to the channel) is $c = (3 \times 8,854E-12 \times 1,15E-6)/2E-6 = 15,3pF$. This is a high value when compared to homologous in inorganic semiconductor industry, but as the objective is to make the calculus a possible reality to non-specialized implementation, this value has been kept. It should also be noted that for the zero-VGS configuration, these values have also been used. The bootstrap algorithm presents the steps to find R_B and, as recommended, it has been kept equal to 0,9. The equation can be simplified having in consideration that all the capacitance are equal for all devices (as the geometrical parameter to be changed is L and not W). If this capacitance is called β and knowing that CB is the compensating capacitor, it can be written: $CB = 17 \times \beta$. In the present case, CB rounds 250pF. The relation between the "Drive" and the "Load" was again of 15 ($L_L/L_D = 3500/233 \approxeq 15$).

The "X" point has a minimum boost voltage of $V_X = (-80+2,98)+0,9[-80+(233/2300) \times 80]$, and it rounds -142V.

In Fig. 6.17, is possible to see the simulation of the bootstrap inverter with the previous defined parameters. If compared with the zero-VGS load inverter, the differences are obvious but, among them, the signal excursion it is the most notorious. An enormous problem when implementing unipolar logic is precisely the excursion of the signal, alongside with other variables. This inverter is capable of almost rail-to-rail its output, which is worth to note.

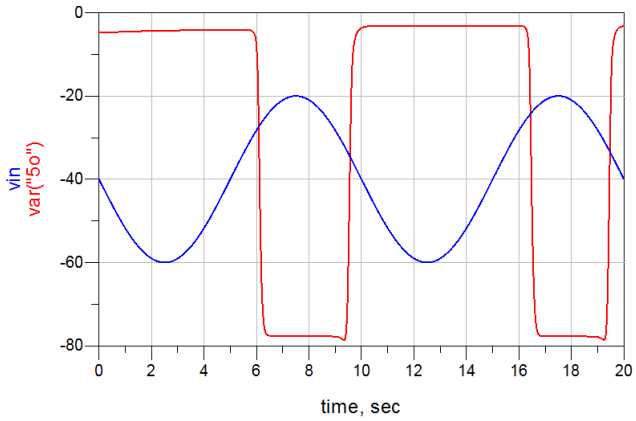


Figure 6.17: Bootstrap Inverter - VDD = -80V

The high voltages are also an inconvenient, but this inverter can still have

its voltage supply cut in half without significant signal degradation, as shown in Fig. 6.18.

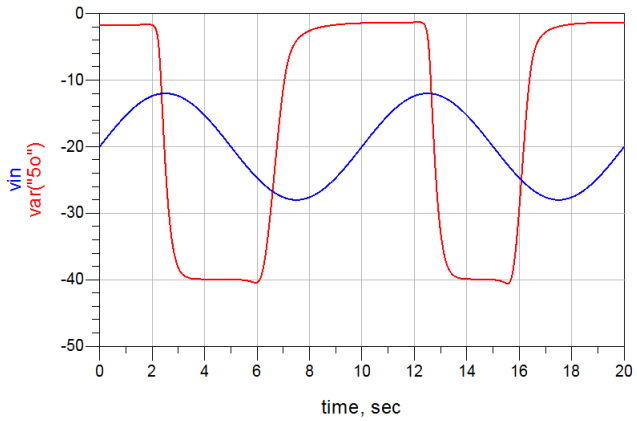


Figure 6.18: Bootstrap Inverter - VDD = -40V

Finally, using the bootstrap inverter and adding a parallel input "Drive" transistor to the circuit shown in 5.4a, a nand gate was made. This component is one of the most fundamental building blocks in digital logic and all logic functions can be derived using it alongside with Boolean algebra[1]. One of the inputs was coupled with a 1Hz frequency source and the other with a 0.5Hz. The results can be seen in Fig. 6.19. It is worth to mention that when both inputs go to "1", the output slightly decreases as, in practice, this is changing the relation between the Load and the Drive, slightly unbalancing the device. The settling time is perceptible between 1,5s and 2s. The positive and negative spikes are related to the logical input, which have abrupt transitions and are capable of rapidly charge and discharge the gate capacitance of the "TD" OFET, affecting the boost capacitor. Organic digital logic is associated with considerable high impedance and this spike/glitch phenomena is unlikely to appear in real implementations.

[1]This property is also known as "functional completness"

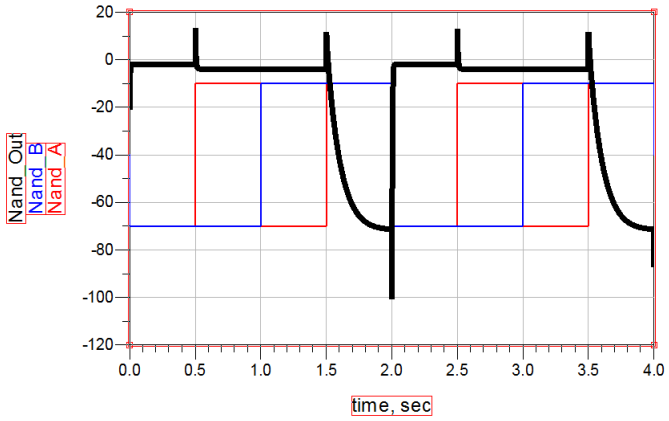


Figure 6.19: Bootstrap Nand - red and blue - inputs; black - output

7 Conclusions and Future Work

The presence of organic and printed electronics in our lives are becoming notorious. The knowledge initially developed by the academy and then passed to the industry, alongside with promising market forecasts are pushing forward the development of new products based on these technologies. Promising technologies as OLED displays and illumination, organic solar cells and large area electronics in general are among the major market players.

This work attempted to present an overview of organic and printed electronics showing its strong connections and simultaneously the aspects that distinguish them.

One of the purposes of this work was to test the versatility of this technology, which presents potentially advantageous characteristics such as low temperature processability, compatibility with a wide range of materials, deformability and - probably the most important - the fact that it does not require expensive clean rooms.

The main deposition techniques and processes have been referenced and explained, alongside with the most commonly used material. For most of the presented materials, its advantages and disadvantages have been emphasized, as well as its characteristics.

Apart from the materials used, three electronic components have been made and characterized using common laboratory tools, and some digital blocks have been implemented according to the objectives initially defined. Additionally, and in an attempt to further gain insight into possible variations in the behavior of these components, 14 more capacitors and 3 more schottky diodes have been created and characterized. In the case of the capacitor, two different substrates have been used and, for the schottky two different materials.

The created capacitors displayed a capacitance ranging from 1pF to 2nF for various deposition conditions, using the same mask aperture. In the case of the schottky devices, only the one with a planar structure - with gold and aluminum contacts using TIPS-Pentacene - displayed a rectifying behavior, with a best mea-

sured $I_{ON}/I_{OFF} = 30$. Although the OFET device has presented a IDS controlled behavior with respect to VGS, the current leakages from the gate to the channel have degraded its output and transfer characteristics. Furthermore, to allow possible inferences, a simulation of the physical characteristics of this device has been further performed.

Acknowledging the fast evolution of organic semiconductors and observing how rapidly new materials are constantly appearing, the problems that may come up in the short and long run have been highlighted - with focus in charge carrier trapping and deterioration.

Another promising area which is getting greater attention is the Internet of Things (IoT). As a matter of fact, a new IEEE publication, exclusively dedicated to this field, is scheduled to start in the beginning of 2014.

Its basis are connectivity and data mining. It is expected that, in a near future, all objects will be able to communicate and an enormous amount of data is expected to be generated.

Foreseen applications, ranging from heath care to social interaction, are expected to be developed in the coming years. For example, doctors will be able to access (with secure protocols) the patient information in real time; patterns may become evident thus allowing sociological insights into human behavior; smart objects may store and retrieve information based on predefined security levels, among many others.

We concluded that both areas have complementary characteristics. Printed and organic electronics cannot compete with conventional inorganic electronics in terms of performance, but they have the advantage of enabling rather inexpensive devices to be made. And the internet of things foresees the intercommunication between common objects, which may require affordable electronic solutions.

In the author's point of view, there are reasonable possibilities that both areas will be coordinated in the future, as the performance requirements for the IoT may be satisfied by the future performance of organic and printed electronics.

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Appendix

Here, some images from the microscope, where the micro-crystalline structure of the tips-pentacene (used in the OFET) can be seen.