Characterization of High-Resistivity Polycrystalline Silicon Substrates for Wafer-Level Packaging and Integration of RF Passives

M. Bartek, A. Polyakov, S.M. Sinaga, P.M. Mendes*, J.H. Correia*, and J.N. Burghartz

Delft University of Technology, Lab. of High-Frequency Technology and Components,
Mekelweg 4, 2628 CD Delft, the Netherlands, e-mail: m.bartek@ewi.tudelft.nl
*University of Minho, Dept. of Industrial Electronics, Guimarães, Portugal

High-resistivity polycrystalline silicon (HRPS) wafers are explored as a novel low-cost and low-loss substrate for radio-frequency (RF) passive components in wafer-level packaging (WLP) and integrated passive networks. A record quality factor (Q=11; 1 GHz; 34 nH) and very low loss (0.65 dB/cm; 17 GHz) are demonstrated for inductors and coplanar wave guides, respectively. The wafer-level packaging solution is based on an adhesive bonding of a passive HRPS wafer to an active silicon IC wafer, where the HRPS wafer serves as a mechanical carrier and vertical spacer. This enables integration of large RF passives with a vertical spacing of >150 µm to the conductive silicon substrate containing the circuitry, while providing mechanical stability, reducing form factor and avoiding any additional RF loss. The HRPS substrates have high dielectric constant, low RF loss, high thermal conductivity, perfect thermal matching, and processing similar to the single-crystalline silicon.

1. Introduction

Radio-frequency (RF) passive components, such as spiral inductors, transmission lines, or antennas, are often the limiting factor in the performance and cost of integrated silicon rf systems. The most important reason behind those limitations are the substantial substrate losses due to the conductivity of the silicon. This unwanted effect can only be reduced by increasing the silicon substrate resistivity or by spacing the component away from the lossy silicon substrate.

Other important issue when monolithic integration of rf components such as inductors is considered, is the fact that such components occupy a large fraction of the costly chip area. This makes any spiral inductor a rather costly component.

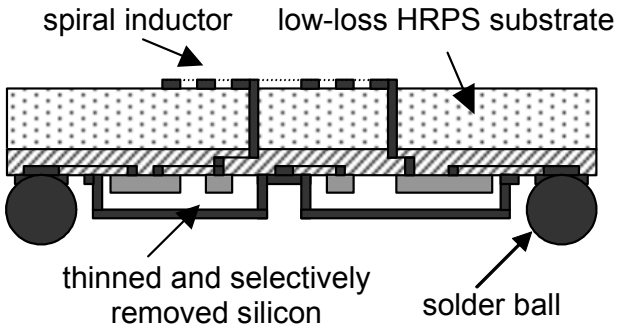

Fig. 1: Schematic view of the proposed wafer-level packaging concept based on a low-loss high-resistivity polycrystalline silicon substrate enabling vertical spacing of RF passive components (e.g. large spiral inductors).

A solution to those problems can be found in integration of the passive components over or under the active circuitry [1]. This can be accomplished by using a spacer substrate, having low RF losses, and if possible high permittivity, and good thermal conductivity. This spacer substrate is bonded to the silicon substrate with active circuitry and carries the rf passive components. This can be achieved using wafer-level packaging (WLP) technology, as shown in Fig. 1.

Glass substrates have been proposed for passive component integration could be considered for that purpose. Glass has, however, a low dielectric constant, a poor thermal conductivity and is difficult to process (e.g. high aspect ratio vias). Silicon is superior in both aspects and can provide low loss figures if high-resistivity silicon (HRS; 1-10 kΩ-cm) is used [2]. Single-crystalline float-zone HRS wafers, however, are expensive and prone to surface-channel effects unless an additional surface-passivation step is added [3]. A cheaper option is using of high-resistivity polycrystalline silicon (HRPS) wafers that can be obtained from the polycrystalline silicon rods for float-zone wafer preparation.

In this paper, HRPS substrates are proposed and characterised as a novel cost-effective alternative to glass and high-resistivity float-zone silicon RF substrates.

2. Characterization of High-Resistivity Polycrystalline Silicon (HRPS) substrates

HRPS wafers having diameter of 4 inch used in our experiments, were obtained from high-resistivity (~4kOhm-cm) polysilicon rods which are normally used as the source material for float-zone single-crystalline Si wafers. By avoiding the expensive float-zone crystallization step, the cost of HRPS wafers is significantly reduced, while the favourable material properties of single crystalline silicon (high thermal conductivity, comparably high dielectric constant, matched thermal expansion coefficient, easy processing) are still present.

2.1 Test structures

The substrate electrical properties were extracted from S-parameter measurements on coplanar waveguides (CPWs), CPW T-resonators and large spiral inductors (34 nH) fabricated using a 2 μm Al metallization with and without 1 μm thick PECVD-oxide insulation layer. The CPW test structures were designed with different signal-ground spacings in order to achieve impedances close to 50 Ω in all cases and to allow for meaningful comparisons. CPW length of 0.5 mm, 1 mm, 3 mm, and 5 mm were used.

For comparison, the same CPW structures were also fabricated on a commercially available glass substrate AF-45 and high-resistivity monocrystalline silicon wafers with and without surface passivation [3].

2.2 Results and discussion

The dielectric constant and the loss tangent were obtained from S-parameter measurements up to 30 GHz. Good agreement of the measured data and simulations in ADS-Momentum were obtained for all CPW structures and substrates shown in Fig. 2. In comparison to the glass substrate Schott AF-45 (α=0.38 dB/cm), a comparably low loss figure was measured for HRPS with (α=0.44 dB/cm) and without (α=0.89 dB/cm) an insulation oxide layer at 6 GHz. In comparison to high-resistivity monocrystalline silicon, no additional surface passivation steps are required for HRPS. That is, because the material has an inherently high defect density (see Fig. 3), suppressing any surface channel formation similarly to the surface amorphization to passivate the monocrystalline silicon. A high Q of 11 and 7.5 was measured for the 34-nH spiral inductor with and without an insulating oxide

layer, respectively, providing further evidence of the excellent RF quality of the HRPS substrate.

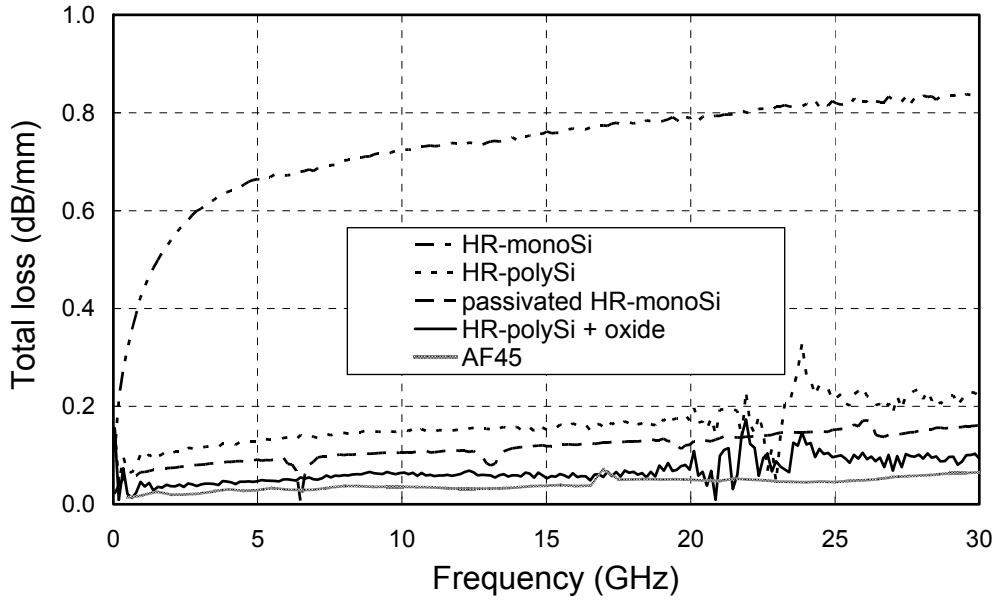

Fig. 2: Frequency dependence of the total loss of coplanar wave guides on high-resistivity polysilicon (HRPS) with and without 1 µm PECVD insulation oxide in comparison to high-resistivity mono-crystalline silicon (HRS) with and without surface passivation and to a Schott AF-45 glass substrate.

The crystallographic structure was analyzed using TEM. Fig. 3 shows as an example a bright-field TEM micrograph indicating presence and typical size of various crystallographic features.

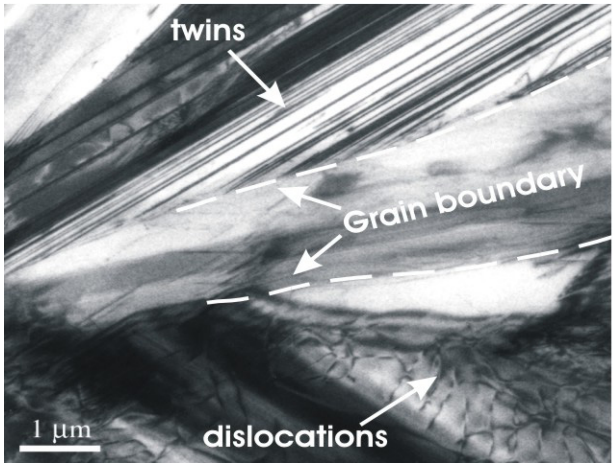

Fig. 3: A bright-field Transmission Electron Microscope (TEM) micrograph illustrating polycrystalline structure of HRPS substrates.

HRPS offers several advantages in comparison to glass, such as the higher and nearly frequency independent dielectric constant (11.7 vs. 4.8-6.2) allowing for a 30%-35% more compact component integration, the >10-times higher thermal conductivity, the perfect matching of the thermal expansion coefficient to that of the integrated circuit (IC) wafer, and the full compatibility with silicon processing.

3. Wafer-level packaging using HRPS substrate

The HRPS wafers can be used as an rf substrate in wafer-level packaging of silicon rf ICs. The same processing steps that are used to achieve the WLP technology basic packaging goal, can be adopted for implementation of an additional functionality at no or very limited additional cost. As indicated in Fig. 1, the HRPS-based WLP concept presented allows packaging of RF silicon ICs with simultaneous integration of high-quality spiral inductors, antennas [4] or cross-talk suppression structures [5].

The proposed WLP concept is based on silicon IC substrate transfer to a low-loss HRPS carrier using wafer-level adhesive bonding and subsequent 3-D metallization for realization of RF passives. The key fabrication steps required are: adhesive wafer bonding, forming of through-substrate vias, metallization within vias, substrate thinning and selective substrate removal.

4. Conclusions

High-resistivity polycrystalline silicon is presented and characterised as a low-cost material for wafer-level packaging of silicon RF ICs. HRPS provides a low RF loss, a high dielectric constant, a high thermal conductivity, good mechanical properties, and a perfect match to the integrated circuit silicon substrate in thermal expansion coefficient. Last but not least, the fabrication technology know-how available for standard single-crystalline Si substrates is directly applicable to processing of HRPS. The HRPS-based WLP concept proposed in this study enables implementation of 3-D passive structures potentially enhancing package performance.

Acknowledgement

The authors wish to acknowledge the support by Philips Semiconductors and Philips Research in the context of the Philips Associate Centre at DIMES (PACD); the Portuguese Foundation for Science and Technology (SFRH/BD/4717/ 2001, POCTI / ESE / 38468 / 2001, FEDER), and the European Commission (project Blue Whale IST-2000-3006). Dr. Manfred Grundner and Wacker Siltronic are acknowledged for supplying polysilicon rod material. Bernd Lux from the Institute of Crystal Growth (IKZ), Berlin, Germany is acknowledged for arranging the wafer dicing and polishing.

References

[1] N.P. Pham, K.T. Ng, M. Bartek, P.M. Sarro, B. Rejaei, J.N. Burghartz, A Micromachining Post-Process Module for RF Silicon Technology, *Techn. Digest IEDM 2000,* San Francisco, USA, Dec. 10-13, 2000, pp. 481-484.

[2] E. Valletta et al., Design and characterization of integrated passive elements on high ohmic silicon, *Proc. 2003 IEEE MTT-S,* pp. 1235 -1238.

[3] B. Rong, J.N. Burghartz, L.K. Nanver, B. Rejaei, M. van der Zwan; Surface-Passivated High-Resistivity Silicon Substrates for RF-IC's, *IEEE Electron Device Letters,* Vol. 25, No. 4, April 2004, pp. 176-178.

[4] P.M. Mendes, A. Polyakov, M. Bartek, J.N. Burghartz, J.H. Correia; An Integrated Folded-Patch Chip-Size Antenna Using High-Resistivity Polycrystalline Silicon Substrate, *Proc. ASDAM 2004,* October'17-21, 2004, Smolenice Castle, Slovakia.

[5] S.M. Sinaga, A. Polyakov, M.Bartek, J.N. Burghartz, Substrate Thinning and Trenching as Crosstalk Suppression Techniques, *Proc. 3rd EMPS,* 2004, Prague, pp. 131-136.